Project

Objectives:

- How to generate netlist file using Design Compiler (DC).
- Synthesis your SV module in Design Compiler with timing constraints.

Stage 1: Read the attached package and follow the tutorial and example step by step to generate netlist file and timing constraint spec file. Tcl scripts are suggested to use in DC, Tcl templates are provided in the packages.

- You will need to connect to the RedHat system remotely: **mo.ece.pdx.edu**. If you are on campus, you can remote access through Ubuntu PC in the Intel lab. If you are off-campus, check: https://cat.pdx.edu/services/network/vpn-services/ to install PSU VPN on your system. Then install a remote access software support x-server such as MobaXterm.
- Remote Login to mo.ece.pdx.edu with your ECE username and password.
- Read the tutorial in dc_task1 to set up DC. Please read the tutorial first and install DC in your UNIX account. If you have any questions about the installation process, please email your problems to the CAT team: support@cat.pdx.edu.

Stage 2:

Task. 1 Following the tutorial of dc_task1. Generate the netlist file of your 8-bit Wallace tree multiplier, simulate and comparing the result of netlist and your original sv file.

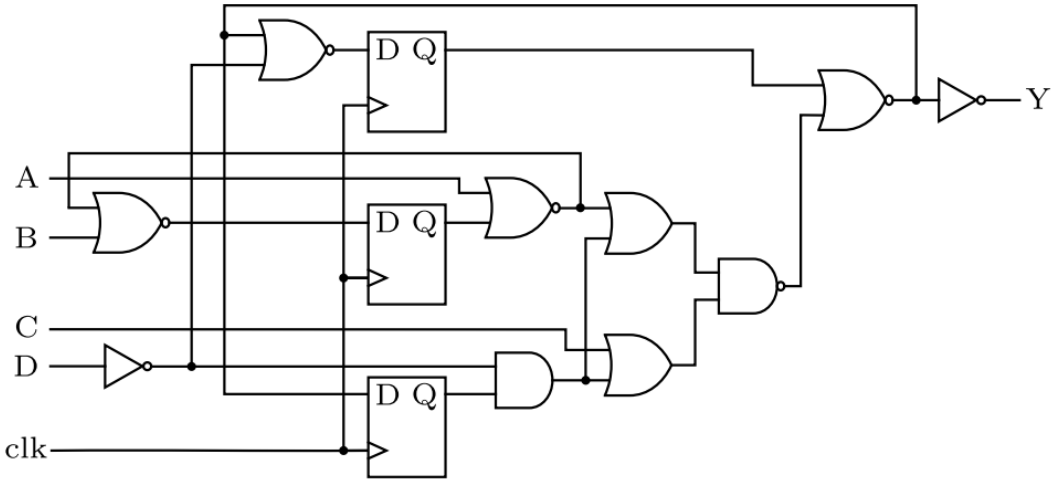

Fig. 1.

Task. 2: Following the tutorial of dc_task2. Create timing constraints for this circuit in Fig.1.

1) Write a gate-level synthesizable SystemVerilog module for the circuit in the figure.1
2) Compile your code in DC with following timing constraints:

Clock:	clock period to 10ns, with maximum clock latency 500ps
Input delay	Port A has a maximum input delay with 180 ps. Port B has a maximum input delay with 50 ps. Port C has a maximum input delay with 100 ps. Port D has a maximum input delay with 80 ps.
Output delay:	Port Y gate has a max output delay with 10ps.

3) Saving and export timing constraints spec file in .wsrc file.

Report requirements

1 Turn in your report and all results to D2L by the deadline.

2 Your report should contain:
- The systemverilog code for your designs.
- Netlist file of dc_task1 in Stage 1.
- Waveform of dc_task1 in Stage 1 to show the comparing result of your design and netlist.
- Reports (Area, Cell, Power) from DC in Stage 1 and task1 of Stage 2.
- Timing constraints spec file (*.wsrc) of dc_task2 Stage 1.
- DDC file of dc_task2 Stage 1.
- Timing constraints spec file (*.wsrc) of Stage 2.

3 Pack your code and DC reports (zip/tar) with the related task name.

4 Only one report is needed for a group. Please indicate your email and name on the first page.