(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

THIRD SEMESTER [B.TECH] JANUARY-FEBRUARY 2023

Paper Code: ICT-205 **Subject: Digital Logic and Computer Design**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q. No.1 which is compulsory. Select one question from each unit.

Q1 Answer the following:-

(a) State principle of duality. (2)
(b) What are the applications of a Multiplexer? (2)
(c) What is a shift register? (2)
(d) Differentiate between a latch and a Flip Flop. (2)
(e) Differentiate between a hardwired and micro programmed control unit. (2)
(f) What do you understand by interrupt driven data transfer? (2)
(g) What do you understand by virtual memory? (2)
(h) What is immediate addressing mode? (1)

UNIT-I

Q2 (a) Design a 4-input priority encoder. (5)
(b) Implement the following Boolean Function with an 8 X 1 Multiplexer $F(A,B,C,D)=\sum(0,3,5,6,8,9,14,15)$. (2)
(c) Implement a Full subtractor using two 4 x 1 MUX and one inverter. (4)
(d) Design a BCD to Excess-3 code converter using a 4-bit adder. (4)

OR

Q3 (a) Determine the essential prime implicants and reduce the following Boolean Function using Tabulation (Quinne – Mckluskey) method $F(A,B,C,D)=\sum(0,1,2,4,5,7,11,15)$. (12)
(b) A logic circuit implements the following Boolean Function $F=A'C+AC'D'$. It is found that the circuit input combinations A=C=1 can never occur. Find a simpler expression for F using proper don't care conditions. (3)

UNIT-II

Q4 (a) Design a BCD synchronous counter using T-Flip Flops. Show the state table, Flip-Flop input functions and circuit diagram. (10)
(b) Draw the internal logic diagram of a 1-bit RAM cell with select, read/write, input and output control lines. (5)

OR

Q5 (a) Design a Serial adder using sequential logic procedure. (7)
(b) The content of a 4-bit registeris initially 1101. The register is shifted six times to the right with serial input being 101101. Show the contents of the register after each shift. (3)
(c) Draw the logic diagram of a 4- bit asynchronous down counter. (5)

P.T.O.

UNIT-III

Q6 (a) What you understand by instruction set completeness? **(2)**

(b) A basic computer has the following registers Program Counter (PC), Instruction Register (IR), Accumulator(AC),Data Register(DR), Address Register (AR), Temporary Register (TR), Input Register (INP), Output Register (OUTP). The size of memory unit is 4096 X 16. The basic computer supports both direct and indirect addressing modes. The control unit is a hardwired control unit. **(10)**

(i) Draw the instruction format of this basic computer. What should be the size of the Common Bus?

(ii) Draw the block diagram showing all significant components of the control unit.

(iii) Write micro-operations for Fetch and decode phases of instruction cycle.

(c) A computer has a memory unit with a capacity of 16,384 words, 40-bits per word. The instruction code format consists of six bits for the operation part and 14-bits fot the address part. There is no indirect mode bit. Two instructions are packed in one memory word and a 40-bit instruction register is available in the control unit. Formulate a procedure for fetching and executing instructions.(Main steps only). **(3)**

OR

Q7 (a) Define Microinstruction, microprogram, control memory, control address register and instruction mapping with respect to a micro-programmed control unit. **(5)**

(b) Draw block diagram of a Micro-program sequencer. **(5)**

(c) Discuss major characteristics of Reduced Instruction Set Computers (RISC). **(5)**

UNIT-IV

Q8 (a) Show step by step multiplication process using Booth multiplication algorithm when (+15) is multiplied with (-13) . Assume 5-bit registers that hold signed numbers in 2's complement format. **(5)**

(b) What do you understand by Direct Memory Access (DMA)? With suitable block diagrams explain working of a DMA controller. **(10)**

OR

Q9 (a) Define the following terms–Virtual address, logical address, physical address, page table, page fault. **(5)**

(b) With suitable block diagrams explain the working of an associative memory. **(5)**

(c) A digital computer has a memory unit of 64K X 16 and cache memory of 1K words. The cache uses a direct mapping with a block size of four words. How many bits are there in tag, index, block and word field of the address format? How many blocks can the cache accommodate? **(5)**

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