(Please write your Exam Roll No.) **Exam Roll No.** 02755102721

END TERM EXAMINATION

THIRD SEMESTER [B.TECH]] FEBRUARY 2023

Paper Code: ECC-207 ***Subject: Digital Logic And Computer Design***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt five questions Q.No. 1 which is compulsory. Select one question from each Unit. Internal choice is indicated. Assume missing data, if any.

Q1. Attempt all questions: **(3x5=15)**

(a) Write the base of the following number systems: Decimal, Binary, Octal, and Hexadecimal.

(b) Draw symbol and write the truth table of JK flip flop.

(c) State the necessity of multiplexer.

(d) Write about parallel priority interrupts.

(e) List out the typical characteristic of multiprocessors.

UNIT-I

Q2. (a) State and prove De Morgan's Theorems. **(5)**

(b) Design 1: 16 demultiplexer using 1: 4 demultiplexers. **(10)**

Q3. (a) Draw the circuit diagram of BCD to 7 segment decoder and write its truth table. **(7)**

(b) Simplify the following Boolean function, $f(W,X,Y,Z)=\sum m(2,6,8,9,10,11,14,15)$ UsingQuine-McClukey tabular method. **(8)**

UNIT-II

Q4. (a) Describe the working of Master-Slave JK Flip-Flop with Truth Table and Logic diagram. **(7)**

(b) Describe the operation of 4 bit SISO shift register with the help of block diagram, truth table and timing diagram. **(8)**

Q5. (a) Draw the block diagram of Programmable Logic Array. **(7)**

(b) Define modulus of a counter? Write down the number of flip flops required for mod-5 counter? **(8)**

UNIT-III

Q6. (a) Explain the organizations of micro programmed control unit with neat sketch. **(8)**

(b) What are the different phases of a basic computer instruction cycle? Explain instruction cycle with flowchart. **(7)**

Q7. (a) Explain with a neat diagram, system configuration incorporating an I/O processor. **(8)**

(b) Discuss the following: Computer configuration for micro program, Symbolic micro program and binary micro program. **(7)**

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UNIT-IV

Q8. (a) Show internal configuration of a DMA controller diagrammatically and explain how it's working. **(8)**

(b) Explain Types of Interrupts with an example for each. **(7)**

Q9. (a) Explain how memory management unit provides memory protection. **(7)**

(b) Explain Cache with Set-Associative and direct mapping. Assume your own example address and explain. **(8)**

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