DELHI TECHNOLOGICAL UNIVERSITY

Shahbad Daulatpur, Main Bawana Road, DL - 42

Two Stage Opamp Design

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Submitted by:

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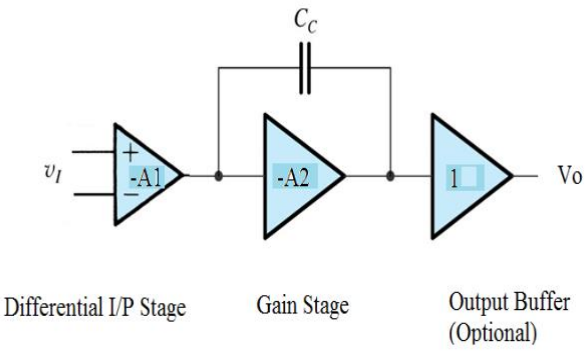
Introduction

An operation amplifier, also known as Op-Amp, is a high-gain electronic voltage amplifier with a differential input and usually a single-ended output. An op-amp only responds to the difference between the two voltages irrespective of the individual values at the inputs.

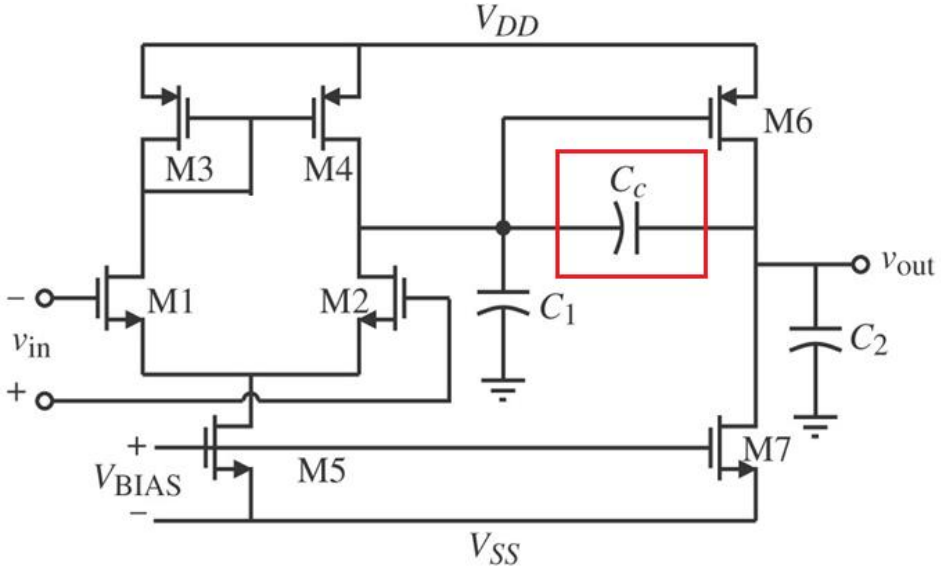
Two stage Op-Amp:



The biggest limitation in the frequency response of the two op-amp lies in the fact that its poles lie very close to each other thereby reducing the phase margin available. For this reason, a compensation capacitor of high value is introduced in order to move the poles apart and to allow for dominant pole approximation and calculation.

However, the addition of compensation capacitor leads to the decrease in phase margin as it behaves as a pole for the phase angle. For this reason, there is a coupling resistor used along with the coupling capacitor. The task in compensating amplifiers for closed loop applications is to move all poles and zeros away from origin except the dominant pole.

Basic configuration for two-stage op-amp:



Design Statement: An Opamp with minimum Phase margin of 50 Degrees with following specifications is to be designed:

1. Av >= 4000
2. Load Capacitance C_L = 15pF
3. V_{DD} = -V_{SS} = 2.5V
4. Unity Gain Bandwidth = 4MHz
5. Slew Rate = 5V/uS
6. ICMR: -1.5 to 2V
7. Output Voltage Swing: -2 to 2V
8. Min. Power Dissipation = 2mW

Simulation Results:

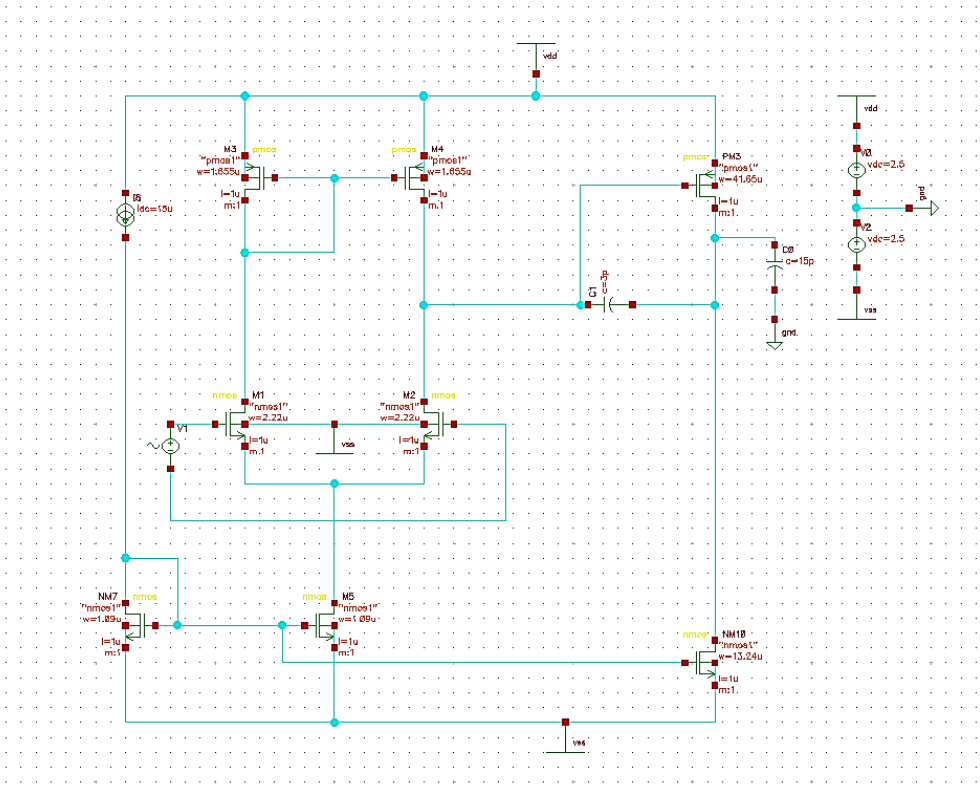


Fig: Schematic

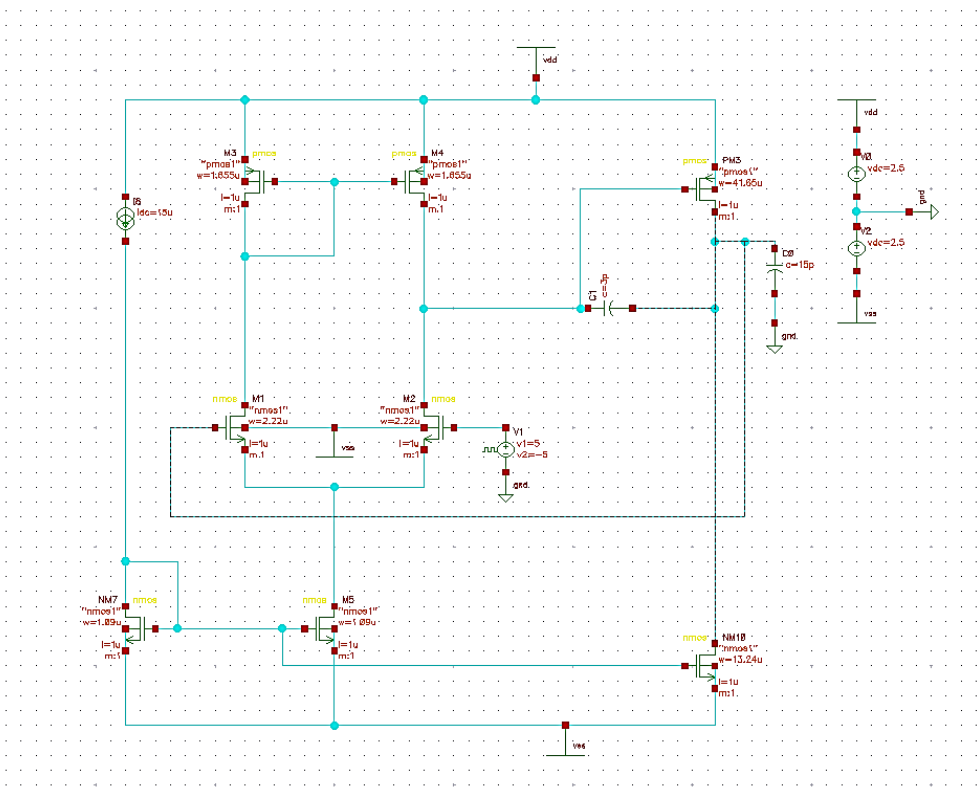


Fig: Schematic for slew rate measurement

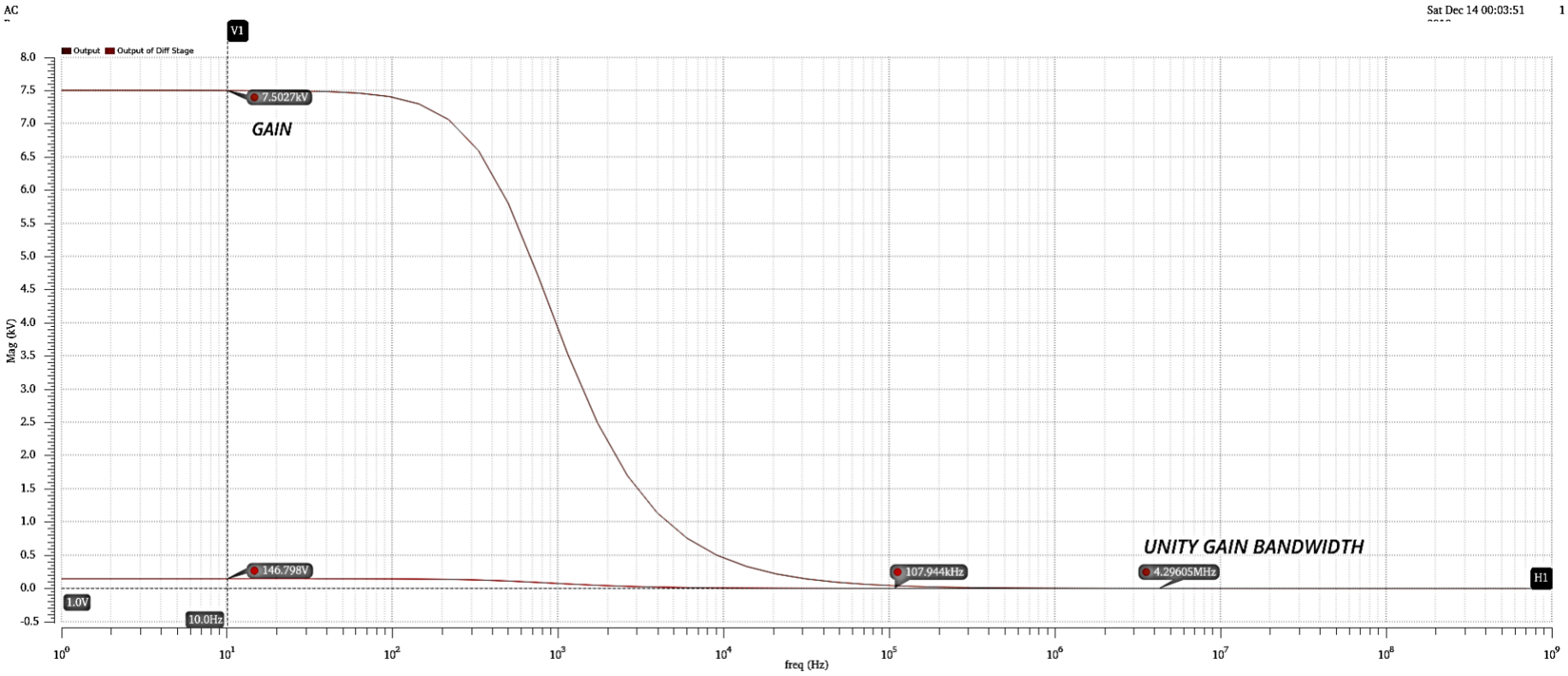


Fig: Input Common Mode Range

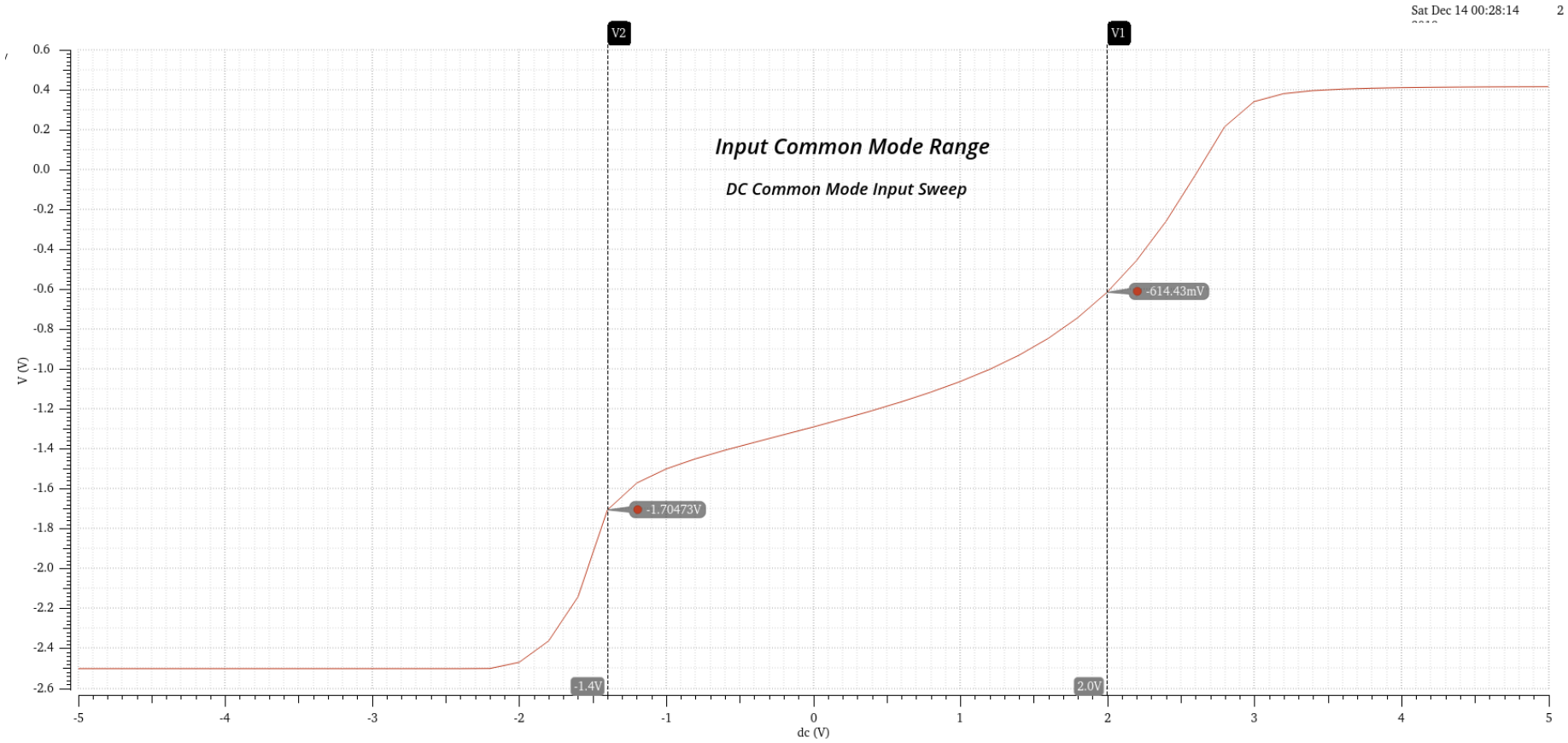


Fig: Gain & Unity Gain Bandwidth

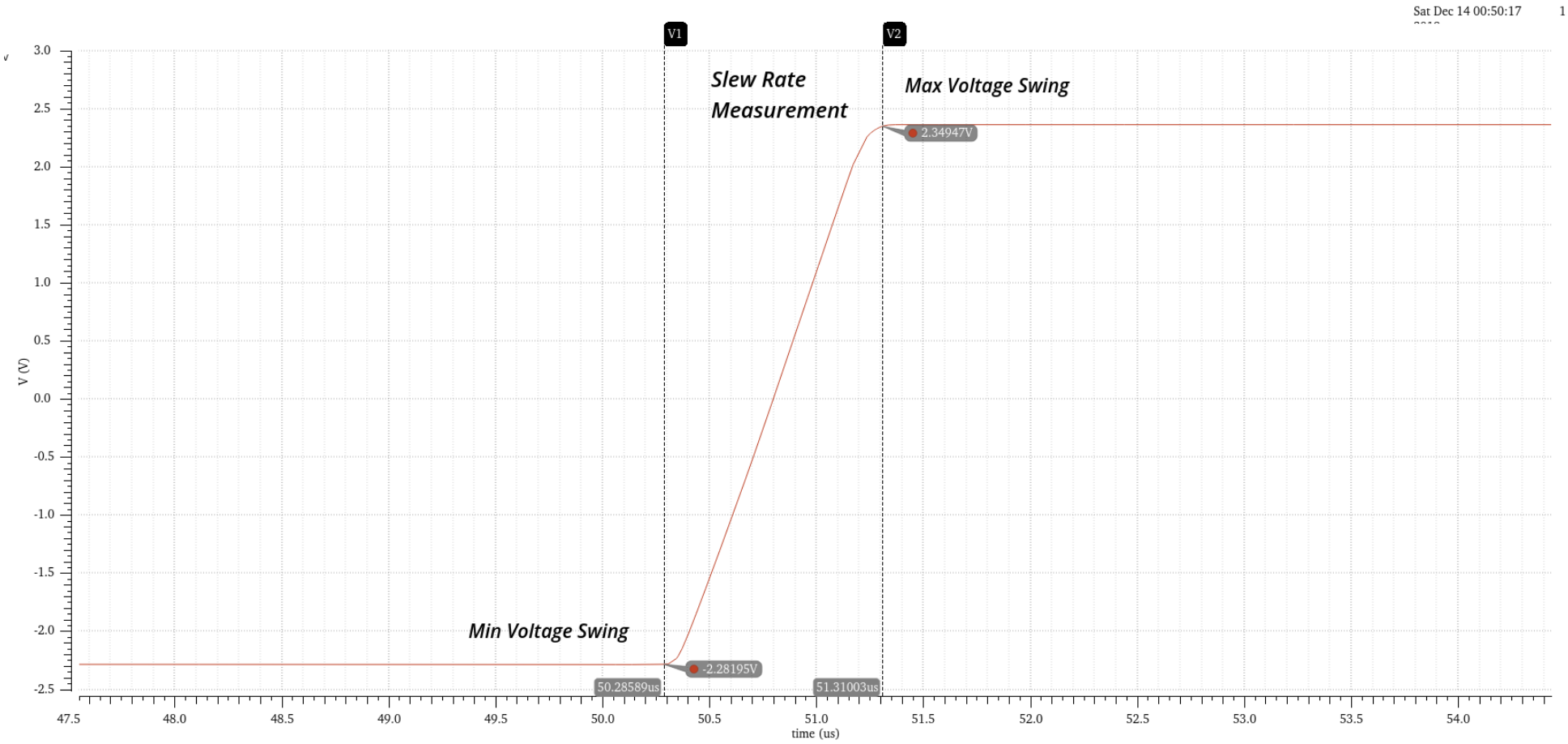


Fig: Slew Rate and Output Voltage Swing

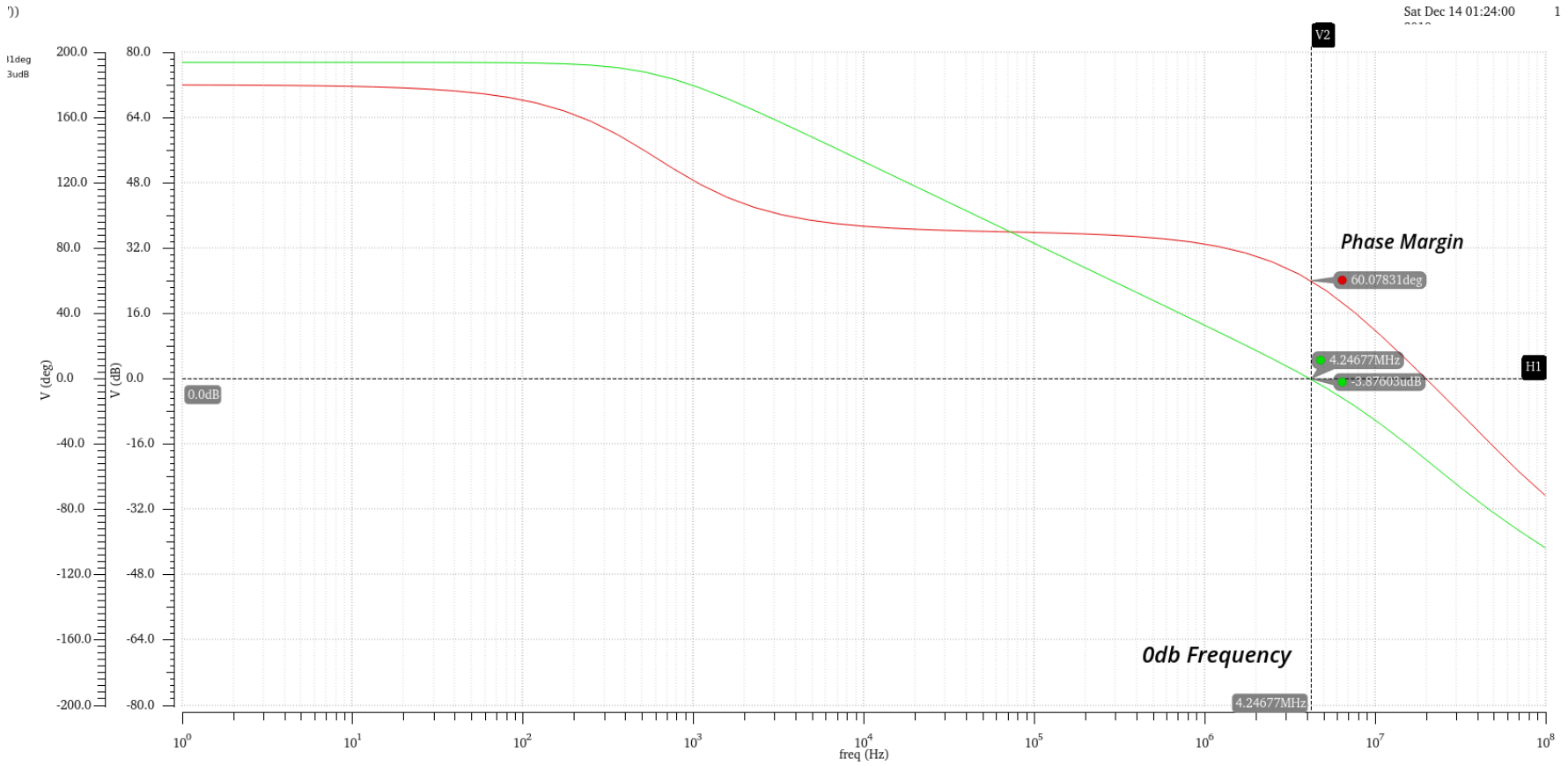


Fig: Phase Margin

Observations:

1. **Gain of Two Stage Opamp**: 7502.7 for design of greater than 4000
2. **Phase Margin**: 60.0783 Degrees for design of greater than 50 Degrees
3. **0db Frequency (Unity Gain Bandwidth):** 4.246MHz for designed 4MHz
4. **ICMR**: -1.4 to +2V for design of -1.5 to 2V
5. **Output Voltage Swing**: -2.28 to 2.34V for design of -2 to 2V
6. **Measured Slew Rate**: (2.349-(-2.281))/(51.31-50.285) V/uS = 4.516V/us for design of 5V/uS
7. **Power Dissipation**: 0.983mW for max power budget of 2mW

Result:

Therefore, a two stage Opamp was designed with the design specifications mentioned above.