DELHI

TECHNOLOGICAL

UNIVERSITY

Subject: ECE208 Computer Architecture(CA)

Submitted To: Prof. Dinesh Kumar

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Objective –

To write the VHDL code for the ***MIPS****(Microprocessor without interlocked pipelined stages)* ***Processor*** and perform simulation.

Work Plan –

Firstly, we will use the instruction set and architecture design for the MIPS processor(MIPS is a RISC processor) provided on the internet. Based on the provided instruction set, we will design and implement the data path and control unit. After completing the design for the MIPS processor, we will write the code for the whole design of the MIPS processor. After that we will verify the code by doing simulations in order to see how the MIPS processor works.

Software required-

ModelSim or Xilinx ISE

Applications -

*TheMicroprocessorwithoutInterlockedPipelineStage (MIPS) microprocessorisoneoftheworld'smostpopular processors for embedded*applications.

MIPS microprocessor can be found in applications ranging from hard disk controllers to laser-jet printers to gaming consoles and audio applications in consumer devices.