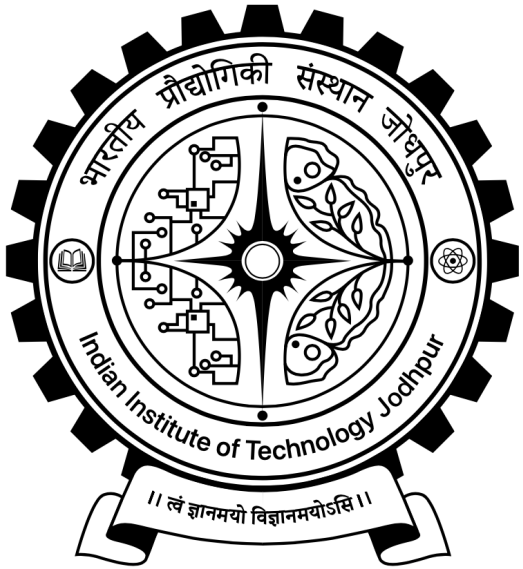

Computer Architecture
CSL3020

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Overview of Memory System

Story so far –

Memory is a one large chunk of bytes.

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All our programs take less than 4 GB of space.

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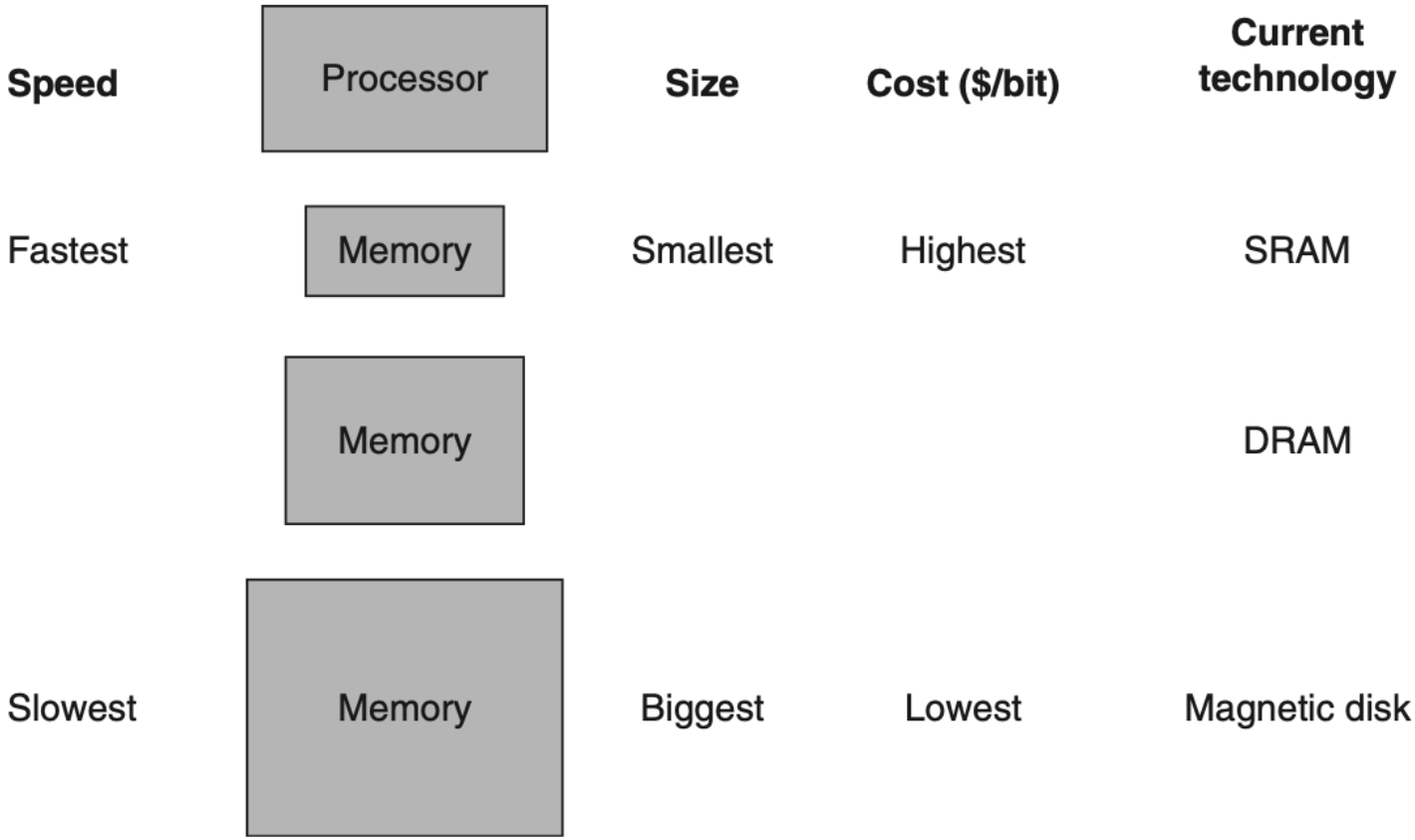

Area, power, latency trade-off

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Temporal locality: The principle stating that if a data location is referenced then it will tend to be referenced again soon.

Spatial locality: The principle stating that if a data location is referenced, data locations with nearby addresses will tend to be referenced soon.

Overview of Memory System

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- Hit rate: The fraction of memory accesses found in the upper level.
- Miss rate = 1 - hit rate
- Miss penalty: It is the time taken to transfer data from lower level to upper level, plus the hit time.

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How to take the advantage of spatial locality?

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How to take the advantage of spatial locality?

Group memory addresses into blocks and transfer blocks between the levels in memory hierarchy instead of transferring single byte.

- Block: The minimum unit of information that can be either present or not present in the two-level hierarchy is called a block or a line.

Basics of Cache

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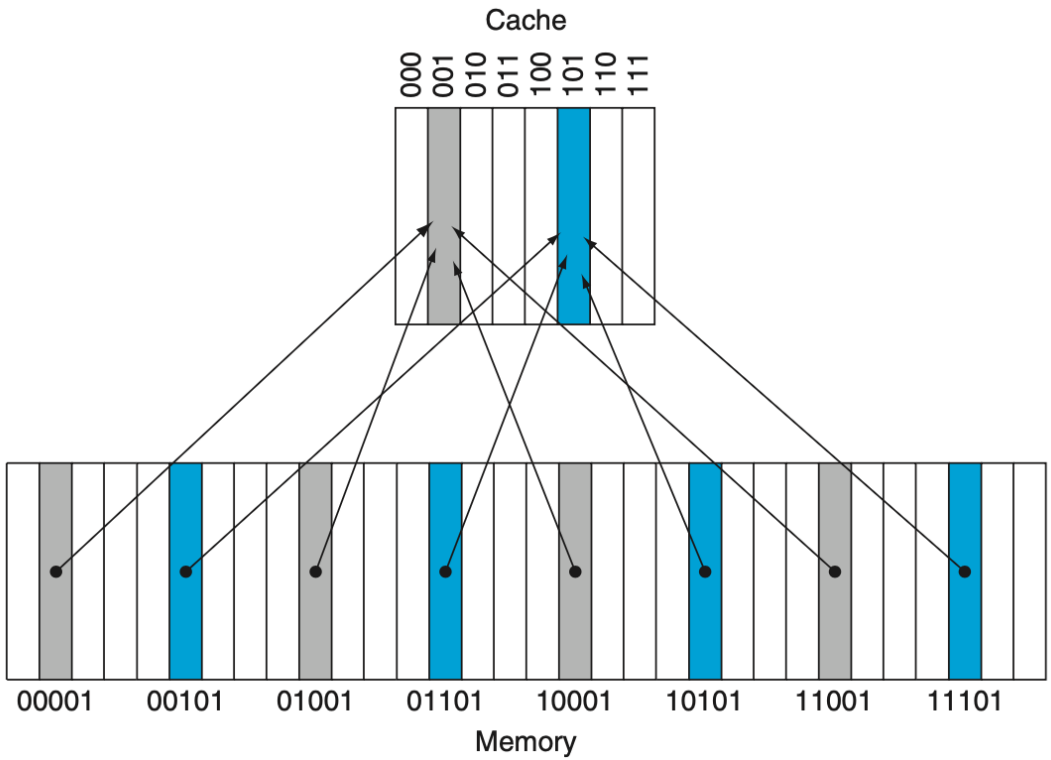
We need a mapping scheme to answer these questions.

Basics of Cache

Direct mapping: Each (main) memory location is mapped to exactly one location in the cache.

Cache location = (Block address) modulo (Number of blocks in the cache)



Basics of Cache

As multiple addresses are mapped to a single cache location, the referenced address is divided into two fields:

- *Tag:* contains the address information required to identify associated block
- *Cache index:* used to select the block

The index of a cache block, together with the tag, uniquely specifies the corresponding memory address.

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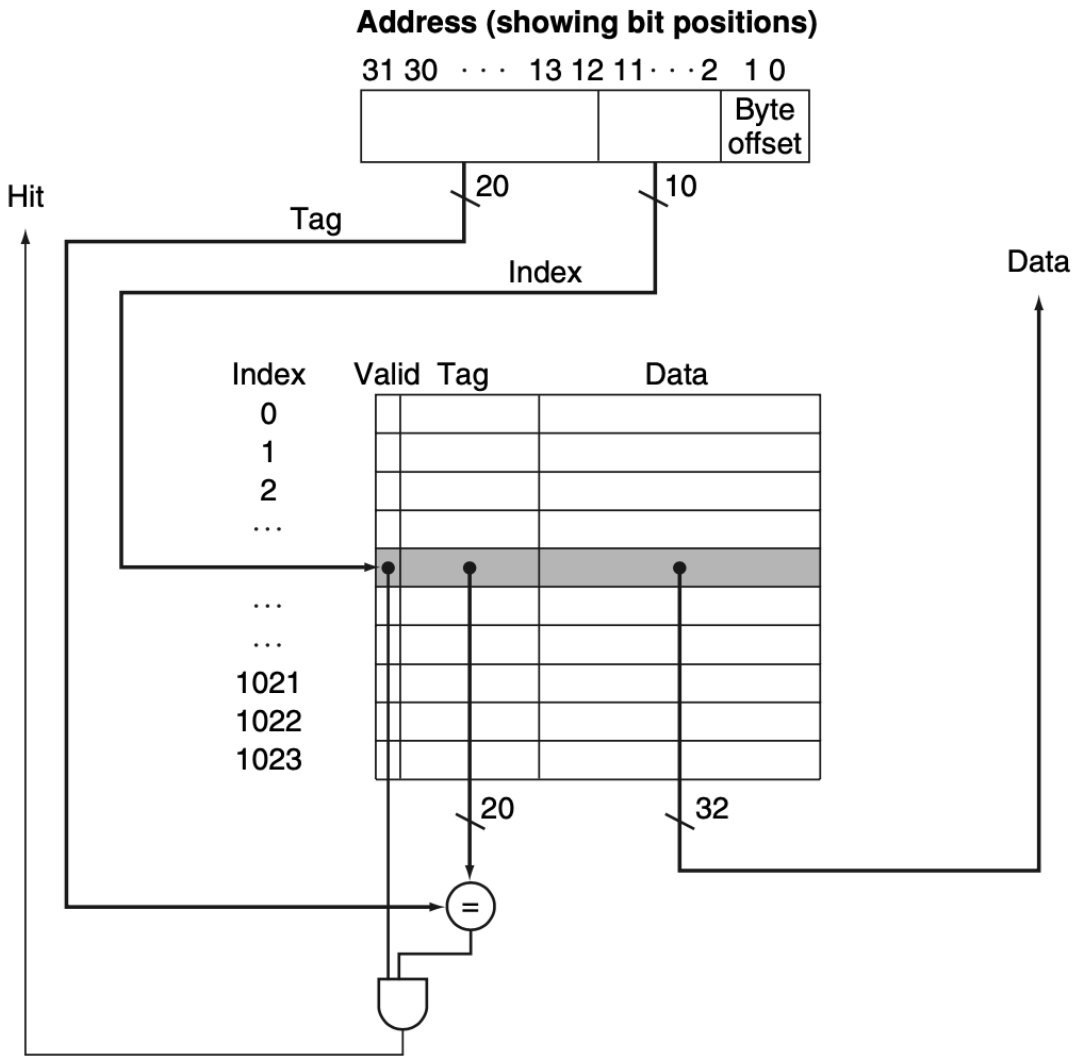
Valid bit: A field in the tables of a memory hierarchy that indicates that the associated block in the hierarchy contains valid data.

Example:

Binary address of reference	Hit or miss in cache	Assigned cache block (where found or placed)
10110_{two}	miss (5.6b)	$(10110_{two} \bmod 8) = 110_{two}$
11010_{two}	miss (5.6c)	$(11010_{two} \bmod 8) = 010_{two}$
10110_{two}	hit	$(10110_{two} \bmod 8) = 110_{two}$
11010_{two}	hit	$(11010_{two} \bmod 8) = 010_{two}$
10000_{two}	miss (5.6d)	$(10000_{two} \bmod 8) = 000_{two}$
00011_{two}	miss (5.6e)	$(00011_{two} \bmod 8) = 011_{two}$
10000_{two}	hit	$(10000_{two} \bmod 8) = 000_{two}$
10010_{two}	miss (5.6f)	$(10010_{two} \bmod 8) = 010_{two}$
10000_{two}	hit	$(10000_{two} \bmod 8) = 000_{two}$

Index	V	Tag	Data
000	N		
001	N		
010	N		
011	N		
100	N		
101	N		
110	N		
111	N		

Cache Misses



Assuming that the block size is one word and address is 32 bit long

Cache Misses

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Ans: 147 Kbits

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4. Restart the instruction execution at the first step.

Cache Misses

The control of the cache on a data access is essentially identical: on a miss, we simply stall the processor until the memory responds with the data.

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- *Write-through:* A scheme in which writes always update both the cache and the next lower level of the memory hierarchy.
- *Write buffer:* A queue that holds data while the data is waiting to be written to memory.
- *Write-back:* Updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.

Cache Performance Analysis

How to evaluate cache performance

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$$\text{Memory-stall clock cycles} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Misses}}{\text{Instructions}} \times \text{Miss penalty}$$

Cache Performance Analysis

Example: Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%.

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Ans: 2.72 times

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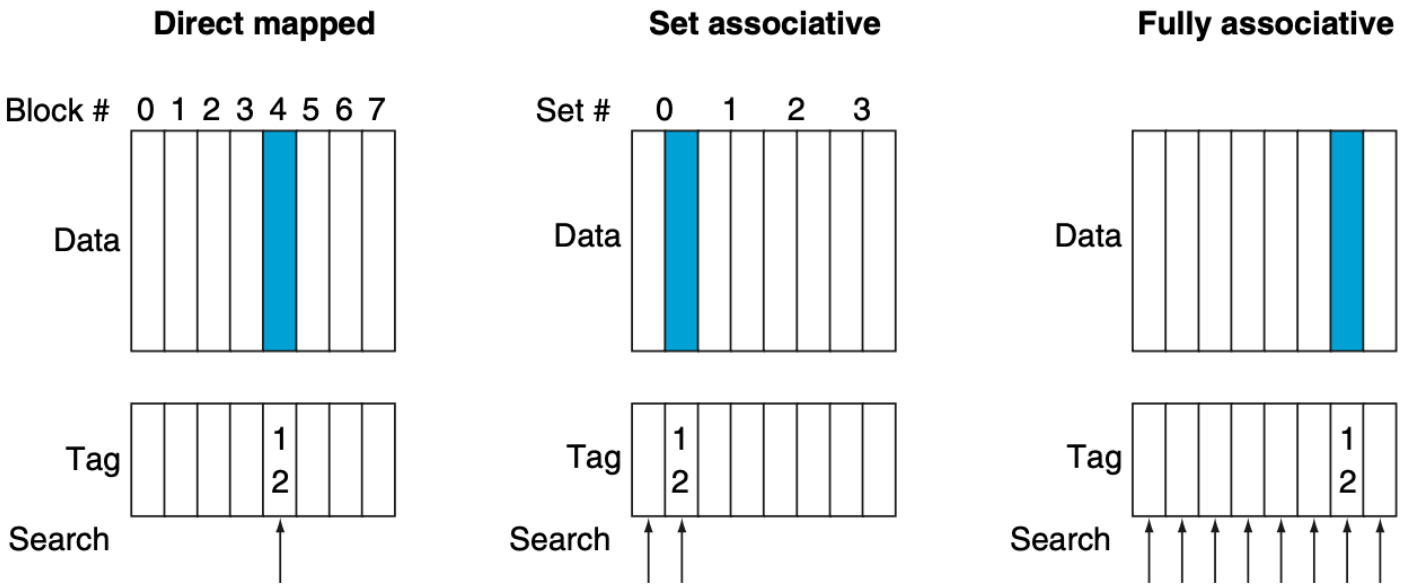

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Example: Assume there is a small cache consisting of eight one-word blocks. Given the following sequence of block addresses: 0, 8, 0, 5, 12, 9, 1, 5, and 8, find the number of misses for 2-way, 4-way, and 8-way set-associative mapping with LRU replacement scheme.

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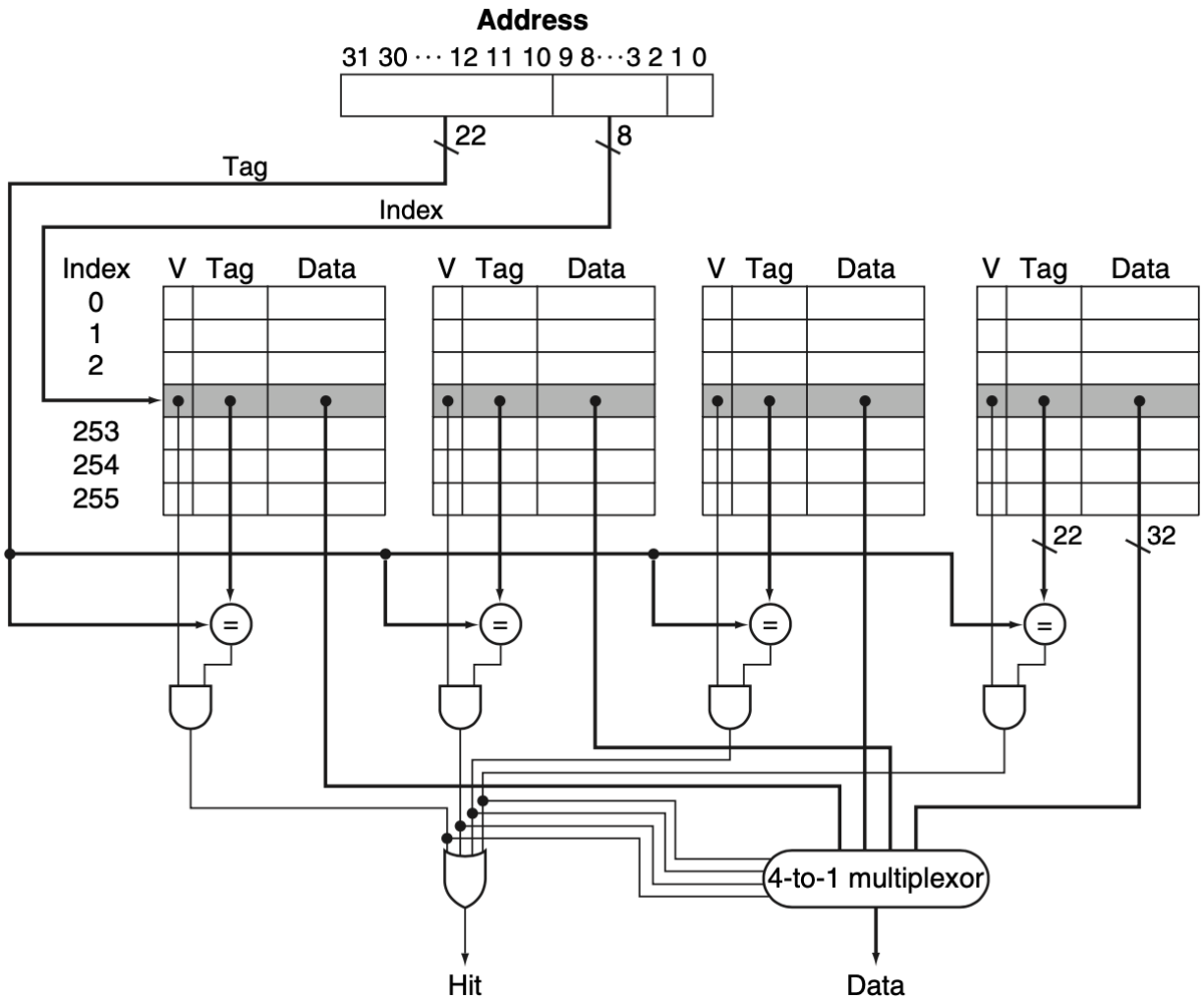
Ans: 8, 6, 6

Reducing Cache Misses



Implementation of a 4-way set-associative cache requires four comparators and a 4-to-1 multiplexor.

Reducing Cache Misses - Multilevel Cavhe