MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

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I SEMESTER M.TECH (CSE) MIDTERM EXAMINATIONS OCT 2024

MIDTERM EXAMINATION

HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5116]

Date: 11-10-2024 Time: 10 – 11:30 AM Max. Marks: **30**

Instructions to Candidates:

- Answer ALL the questions

Q1. What are the Directives in OpenMP and summarize their roles. **3M**

Q2. Interpret and explain the role of *for* and *section* directives in OpenMP. Give the structure in usage of them in OpenMP. **3M**

Q3. Write and explain a MPI routine with its arguments that combines data from all processes in the communicator using a specified operation to store the result in the root and this result is distributed to all processes in the communicator. **2M**

Q4. A MPI program consists of 2 processes. Process 0 sends a number and a text message to the receiver. Receiver in turn must receive this number and the text message and then sleeps for 1 sec. After this, now the receiver sends this text message back to the sender. Measure the time taken by the receiver to send the text message back to the sender. Implement this in your MPI program using standard mode send and receive. Use the user-friendly statements where ever required in your program. **3M**

Q5. Implement to carry out an efficient MPI program to meet the following specifications:
It is required for the root process to send a word to all its slaves. All processes (including the root) will have to reverse this word. Display the time taken by each of the slaves. Also let every process display the reversed word. Use the user-friendly statements wherever required in your program. Do not write any user defined function(s). **4M**

Q6. Interpret the use of threads, blocks, and grids in the context of CUDA? **3M**

Q7. Construct an efficient CUDA kernel to generate an output matrix of size N X N from given input matrix of size N X N.

For Eg:

Output matrix =

A	B	C
D	E	F
G	H	I

from the following input matrix

Input matrix =	1	2	3
	4	5	6
	7	8	9

4M

Q8. Construct the CUDA code of main( ) function required to use the kernel you wrote in question number Q7. 4M

Q9. Sketch a specific block diagram and explain its architectural class scheme based on the multiplicity of instruction streams and data streams in which a parallel computer may execute distinct instructions operating over the same data stream and its derivatives. 2M

Q10. Differentiate the role of hardware and software in programmatic levels of parallel processing in parallel computer systems. 2M