arm

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1. What is true about below statemets,
I. Von Neumann Architecture shares common address space for Data and Instructions.
II. Harvard Architecture has separate physical address space for Data and Instructions.

Answers

1. Only I is true

2. Only II is true

3. Both I and II are true

4. None of them is true

2. What are the significant designing issues/factors taken into consideration for RISC Processors?

Answers

1. Simplicity in Instruction Set

2. Pipeline Instruction Optimization

3. Register Usage Optimization

4. All of the above

3. Which among the following data processing instructions doesnot use the barrel shifter?

Answers

1. ADD R2,R5, R4

2. MOV R5, R4, LSL #2

3. MOV r5, R4, LSR #2

4. MOV r5, R4, ROR #2

4. In CPU structure, what kind of instruction to be executed is held by an instruction Register (IR)?

Answers

1. Current (present)

2. Previous

3. Next

4. All of the above

5. Which type of non-privileged processor mode is entered due to raising of high priority of an interrupt?

Answers

1. User mode

2. Fast Interrupt Mode (FIQ)

3. Interrupt Mode (IRQ

4. Supervisor Mode (SVC)

6. What is the size of the bit-band alias region(s) in the memory map of a Cortex-M3 or Cortex-M4?

Answers

6. What is the size of the bit-band alias region(s) in the memory map of a Cortex-M3 or Cortex-M4?

Answers

1. 1 MB

2. 8 MB

3. 16 MB

4. 32 MB

7. Abort mode generally occurs when _____

Answers

1. an attempt to access memory fails

2. low priority interrupt is raised

3. ARM processor is on rest

4. undefined instructions are to be handled

8. Assunming, integer is 2 byte, What will be the output of the program?

```
#include<stdio.h>
int main()
{     printf( "%x\n" , -1>>1);
   return 0;
 }
```

Answers

1. ffff

2. 0fff

3. 0000

4. fff0

9. When a global variable may be modified by an exception handler, it should be declared as

Answers

1. Const

2. Static

3. dynamic

4. Volatile

10. If r0=4 , r1=0 , r2=3 and r3=4, what is the result of r0 after executing the following operation?

```
UMLAL r0 , r1 , r2,  r3
```

Answers

1. r0 == 0xC

2. r0 == 0x10

3. r0 == 0x12

4. r0 == 0x14

11. Which of the following is correct sequence of execption priorities from highest to lowest priorities?

Answers

1. Reset -> Data Abort -> IRQ -> FIQ -> Prefetch abort -> Software Interrupt

2. Reset -> Data Abort -> FIQ -> IRQ -> Prefetch abort -> Software Interrupt

3. Reset -> Data Abort -> Prefetch abort -> IRQ -> FIQ -> Software Interrupt

4. Reset -> Data Abort -> Prefetch abort -> FIQ -> IRQ -> Software Interrupt

12. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____ .

Answers

1. EA = [Rn]

2. EA = [Rn + Rm]

3. EA = [Rn] + Rm

4. EA = [Rm] + Rn

13. By which method SVC software exception is triggered ?

Answers

1. SVC instruction

2. By writing To NVIC

3. Both A and B

14. Which of the following stack is used in ARM cortex m3?

Answers

1. Full Descending

2. Full Ascending

3. Both of the above

4. None of the above

15. On a Cortex-M processor with an MPU present,which exception will be generated by an invalid EXC_RETURN code?

Answers

1. Reset

2. Busfault

3. MemManage

4. UsageFault

16. Which of the following is not the part of PSR(Program status register)?

Answers

1. APSR(Application program status register)
2. IPSR(Interrupt program status register)
3. EPSR(Exception program status register)
4. EPSR(Execution program status register)

17. Consider a four bit ALU which does four bit arithmetic. When R0 = 1101 and R1 = 1011, what is the status of NZCV flags, when R0 and R1 added?

Answers

1. NZCV = 0111
2. NZCV = 1000
3. NZCV = 1001
4. NZCV = 1010

18. Which of the default exception handler as defined in CMSIS-core is..

Answers

1. MemManage fault
2. Bus fault
3. Hard fault
4. Usage fault

19. Which TWO of the following memory-mapped regions for the Cortex-M3 allow for bit-banding operation

Answers

1. SRAM
2. CODE
3. PERIPHERAL
4. Both A and C

20. RS232 is not TTL compatible

Answers

1. True
2. False

21. Which out of the following is the main function of a Watchdog timer?

Answers

1. control the compare mode
2. protection from failures to the system
3. control the capture mode
4. All of the above

22. In the ARM Nomenclature ARMxTDMI, D and M stand for _____ and _____.

Answers

1. Debugger and Multiplier units are not present

2. Division and Multiplier units are present

3. Debug and Fast Multiplier units are present

4. Division and Multiplier units are not present

23. LDMIA Rd!,<reg list> what does this instrcution ?

Answers

1. Read mulitiple words from memory spicified by Rd,address increment after(IA) each transfer

2. Read mulitiple words from memory spicified by Rd,address increment after(IA) each read

3. Read mulitiple words from memory spicified by Rd,address increment before(IB) each transfer

4. Read mulitiple words from memory spicified by Rd,address increment before(IB) each read

24. ____ register is used to store the return address of subroutine also known as _____.

Answers

1. R13, Link register

2. R14, Link register

3. R13, Stack pointer

4. R14, Stack pointer

5. R15, Program counter

25. Which of the following will generate the maximum time delay?

Answers

1. f/2

2. f/4

3. f/16

4. f/32

26. The technique of assigning a memory address to each I/O device in the computer system is called

Answers

1. Memory-mapped I/O

2. ported I/O

3. dedicated I/O

4. wired I/O

27. In Cortex M processors Exceptions like NMI , Hard FAULT etc have fixed priority levels. The priority levels are represented in

Answers

1. Range from (0-255)

2. negative numbers

3. positive numbers

4. None of the above

28. What is the use of the prescalar in the operation of the timer?

Answers

1. For fast calculation

2. for increasing the time delay given by the timer by decreasing its frequency of operation

3. for removing the concept the reloading of count

4. for easy counter operations

29. Largest value that can be loaded in an 8 bit register is ?

Answers

1. 11111111H

2. FH

3. FFH

4. 00H

30. The Thumb instruction set allows for

Answers

1. Smaller instructions, Larger code size, larger number of instructions.

2. Larger instructions, Smaller code size, smaller number of instructions

3. Smaller instructions, Smaller code size, smaller number of instructions

4. Smaller instructions, Smaller code size, larger number of instructions

31. UART stands for

Answers

1. Universal asynchronization receiver/transmitter

2. Universal asynchronous receiver/transmitter

3. United asynchronous receiver/transmitter

4. Universal automatic receiver/transmitter

32. Which out of the following is not a directive

Answers

1. .EQU

2. .DEVICE

3. .ORG

4. .LDI

33. In SPI bus, which signal line carries data from master to slave device & hence regarded as Slave Input/Slave Data In (SI/SDI)?

Answers

1. Master Out Slave In (MOSI)

2. Master In Slave Out (MISO)

3. Serial Clock (SCLK)

4. Slave Select (SS)

34. Which of the following is true about SysTick timer?

Answers

1. it is used to generate interrupts periodically

2. it is used to generate execptions periodically

3. it is used to generate interrupts, but not periodically

4. Both A and B

35. What is the step size for 8 bit ADC, when max voltage is 2.56V?

Answers

1. 100mV

2. 10mV

3. 1mV

4. 0.1mV

36. What is the START condition of I2C?

Answers

1. SCL line low,SDA line from high to low

2. SCL line high,SDA line from low to high

3. SCL line high,SDA line from high to low

4. SCL line low,SDA line from low to high

37. Dominant bit in CAN Protocol means--?

Answers

1. logical 1

2. logical 0

3. None of this

4. Both A and B

38. What is the START condition of I2C?

Answers

1. SCL line low,SDA line from high to low

2. SCL line high,SDA line from low to high

3. SCL line high,SDA line from high to low

4. SCL line low,SDA line from low to high

39. CPOL = 0 , CPHA = 0 in spi means ?

Answers

1. Read on falling edge , changed on a rising edge

2. Read on Rising edge , changed on a falling edge

40. Which of the following is/are Main advantage of the PWM?

Answers

1. Power loss in the switching devices is very high

2. Power loss in the switching devices is very low

3. No power loss in switching devices

4. Both A and B