MCPI MCQ

1. **What is true about below statements,**
   i. **Von Neumann Architecture shares common address space for Data and Instructions.**
   ii. **Harvard Architecture has separate physical address space for Data and Instructions.**
   a) Only I is true
   b) Only II is true
   c) Both I and II are true
   d) None of them is True

2. **What are the significant designing issues/factors taken into consideration for RISC Processors ?**
   a. Simplicity in Instruction Set
   b. Pipeline Instruction Optimization
   c. Register Usage Optimization
   d. All of the above

3. **Which among the following data processing instructions does not use the barrel shifter?**
   a) ADD R2, R5, R4
   b) MOV R5, R4, LSL #2
   c) MOV R5, R4, LSR #2
   d) MOV R5, R4, ROR #2

4. **In CPU structure, what kind of instruction to be executed is held by an instruction Register (IR)?**
   a) Current (present)
   b) Previous
   c) Next
   d) All of the above

5. **Which type of non-privileged processor mode is entered due to raising of high priority of an interrupt?**
   a) User mode
   b) Fast Interrupt Mode (FIQ)
   c) Interrupt Mode (IRQ)
   d) Supervisor Mode (SVC)

6. **What is the size of the bit-band alias region(s) in the memory map of a Cortex-M3 or Cortex-M4?**
   a) 1MB
   b) 8MB
   c) 16MB
   d) **32MB**

7. **Abort mode generally enters when _____**
   a. an attempt access memory fails
   b. low priority interrupt is raised
   c. ARM processor is on rest
   d. undefined instructions are to be handled

8. **Assuming, integer is 2 byte, What will be the output of the program?**

```c
#include<stdio.h>

int main()
{
    printf("%x\n", -1>>1);
    return 0;
}
```

   a) ffff
   b) 0fff
   c) 0000
   d) fff0

9. **When a global variable may be modified by an exception handler, it should be declared as**
   a) Const
   b) Static
   c) dynamic
   d) Volatile

10. **If r0=4 , r1=0 , r2=3 and r3=4, what is the result of r0 after executing the following operation?**
    UMLAL r0 , n1, r2, r3
    a) r0 == 0xC
    b) r0 == 0x10
    c) r0 == 0x12
    d) r0 == 0x14

11. **Which of the following is correct sequence of exception priorities from highest to lowest priorities?**
    a) Reset -› Data Abort -> IRQ -> FIQ -> Prefetch abort -> Software Interrupt
    b) Reset -› Data Abort -> FIQ -> IRQ ->Prefetch abort -> Software Interrupt
    c) Reset -› Data Abort -> Prefetch abort -> IRQ -> FIQ -> Software Interrupt
    d) Reset -› Data Abort -> Prefetch abort -> FIQ -› IRQ -> Software Interrupt

12. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____

a) EA = [Rn]

b) EA = [Rn + Rm]

c) EA = [Rn] + Rm

d) EA = [Rm] + Rn

13. By which method svc software exception is triggered?

a) SVC Instruction

b) By writing to NVIC

c) Both A and B

14. which of the following stack is used in ARM cortex M3?

a) Full Descending

b) Full Ascending

c) Both of the Above

d) None of the Above

15. On a Cortex-M processor with an MPU present, which exception will be generated by an invalid EXC_RETURN code

a) Reset

b) Busfault

c) MemManage

d) UsageFault

16. Which of the following is not the part of PSR(Program status register)?

a) APSR(Application program status register)

b) IPSR(Interrupt program status register)

c) EPSR(Exception program status register)

d) EPSR(Execution program status register)

17. Consider a four-bit ALU which does four bits arithmetic. When R0 = 1101 and R1 = 1011, what is the status of NZCV flags, when R0 and R1 added?

a) NZCV = 0111

b) NZCV = 1000

c) NZCV = 1001

d) NZCV = 1010

18. Which of the default exception handler as defined in CMSIS-core is_____?

a) MemManage fault

b) Bus fault

c) **Hard fault**

d) Usage fault

19. Which TWO of the following memory-mapped regions for the Cortex-M3 allow for bit-banding operation?

a) SRAM
b) CODE
c) PERIPHERAL
d) Both A and C

20. RS232 is not TTL compatible

a) True
b) False

21. Which out of the following is the main function of a Watchdog timer?

a) Control the compare mode
b) protection from failures to the system
c) control the capture mode
d) All of the above

22. In the ARM Nomenclature ARMxTDMI, D and M stand for _____ and _____.

a) Debugger and Multiplier units are not present
b) Division and Multiplier units are present
c) Debug and Fast Multiplier units are present
d) Division and Multiplier units are not present

23. LDMIA Rd!<reg list> what does this instruction ?

a) Read multiple words from memory specified by Rd, address increment after(IA) each transfer
b) Read multiple words from memory specified by Rd, address increment after(IA) each read
c) Read multiple words from memory specified by Rd, address increment before(IB) each transfer
d) Read multiple words from memory specified by Rd, address increment before(IB) each read

24. ____ register is used to store the return address of subroutine also known as _____.

a) R13, Link register
b) R14, Link register
c) R13, Stack pointer
d) R14, Stack pointer
e) R15, Program counter

25. Which of the following will generate the maximum time delay?

a) f/2
b) f/4
c) f/16
d) f/32

26. The technique of assigning a memory address to each I/O device in the computer system is called

a) Memory-mapped I/O
b) ported I/O
c) dedicated I/O
d) wired I/O

27. In Cortex M Processors Exceptions like NMI , Hard FAULT etc have fixed priority levels. The priority levels are represented in

a) Range from (0-255)
b) negative numbers
c) positive numbers
d) None of the above

28. What is the use of the prescalar in the operation of the timer?

a) For fast calculation
b) for increasing the time delay given by the timer by decreasing its frequency of operation
c) for removing the concept, the reloading of count
d) for easy counter operation

29. Largest value that can be loaded in an 8 bit register is ?

a) 11111111H
b) FH
c) FFH
d) 00H

30. The Thumb instruction set allows for

a) Smaller instructions, Larger code size, larger number of instructions.
b) Larger instructions, Smaller code size, smaller number of instructions
c) Smaller instructions, Smaller code size, smaller number of instructions
d) Smaller instructions, Smaller code size, larger number of instructions

31. UART stands for

a) Universal asynchronization receiver/transmitter
b) Universal asynchronous receiver/transmitter
c) United asynchronous receiver/transmitter
d) Universal automatic receiver/transmitter

32. Which out of the following is not a directive?

a) .EQU
b) .DEVICE
c) .ORG
d) .LDI

33. In SPI bus, which signal line carries data from master to slave device & hence regarded as Slave Input/Slave Data In (SI/SDI)?

a) Master Out Slave In (MOSI)
b) Master In Slave Out (MISO)
c) Serial Clock (SCLK)
d) Slave Select (SS)

34. Which of the following is true about SysTick timer?

a) it is used to generate interrupts periodically
b) it is used to generate execptions periodically
c) it is used to generate interrupts, but not periodically
d) Both A and B

35. What is the step size for 8 bit ADC, when max voltage is 2.56V?

a) 100mV
b) 10mV
c) 1mV
d) 0.1mV

36. What is the START condition of I2C?

a) SCL line low,SDA line from high to low
b) SCL line high,SDA line from low to high
c) SCL line high,SDA line from high to low
d) SCL line low,SDA line from low to high

37. Dominant bit in CAN Protocol means?

a) logical 1
b) logical 0
c) None of this
d) Both A and B

38. What is the START condition of I2C?

a) SCL line low, SDA line from high to low
b) SCL line high, SDA line from low to high
c) SCL line high, SDA line from high to low
d) SCL line low, SDA line from low to high

39. CPOL = 0 , CPHA = 0 in SPI means ?

a) Read on falling edge , changed on a rising edge
b) Read on Rising edge , changed on a falling edge

40. Which of the following is/are Main advantage of the PWM?

a) Power loss in the switching devices is very high
b) Power loss in the switching devices is very low
c) No power loss in switching devices
d) Both A and B

41. What is the processor used by ARM7?

a) 8-bit CISC
b) 8-bit RISC
c) 32-bit CISC
d) 32-bit RISC

42. What is the instruction set used by ARM7?

a) 16-bit instruction set
b) 32-bit instruction set
c) 64-bit instruction set
d) 8-bit instruction set

43. How many registers are there in ARM7?

a) 35 register(28 GPR and 7 SPR)
b) 37 registers(28 GPR and 9 SPR)
c) 37 registers(31 GPR and 6 SPR)
d) 35 register(30 GPR and 5 SPR)

44. ARM7 has an in-built debugging device?

a) True
b) False

45. What is the capability of ARM7 f instruction for a second?

a) 110 MIPS
b) 150 MIPS
c) 125 MIPS
d) 130 MIPS

46. We have no use of having silicon customization?

a) True
b) False

47. Which of the following has the same instruction set as ARM7?

a) ARM6
b) ARMv3
c) ARM71a0
d) ARMv4T

48. What are t, d, m, I stands for in ARM7TDMI?

a) Timer, Debug, Multiplex, ICE

b) Thumb, Debug, Multiplier, ICE

c) Timer, Debug, Modulation, IS

d) Thumb, Debug, Multiplier, ICE

49. ARM stands for _____

a) Advanced RISC Machine

b) Advanced RISC Methodology

c) Advanced Reduced Machine

d) Advanced Reduced Methodology

50. What are the profiles for ARM architecture?

a) A,R

b) A,M

c) A,R,M

d) R,M

51. ARM7DI operates in which mode?

a) Big Endian

b) Little Endian

c) Both big and little Endian

d) Neither big nor little Endian

52. In which of the following ARM processors virtual memory is present?

a) ARM7DI

b) ARM7TDMI-S

c) ARM7TDMI

d) ARM7EJ-S

53. How many instructions pipelining is used in ARM7EJ-S?

a) 3-Stage

b) 4-Stage

c) 5-Stage

d)2-stage

54. How many bit data bus is used in ARM7EJ-s?

a) 32-bit

b) 16-bit

c) 8-bit

d) Both 16 and 32 bit

55. What is the cache memory for ARM710T?

a) 12Kb
b) 16Kb
c) 32Kb
d) 8Kb

56. What are the pipelining stages include?

a) Fetch, Decode, Write
b) Fetch, Decode, Execute
c) Fetch, Execute, Write
d) Fetch, Decode, Execute, Write

57. What is pipe lining?

a) Non linear
b) Linear
c) Linear and Non linear
d) Sometimes both

58. What are the no of pins that are in the ARM7 processors?

a) 65 pin with QFP
b) 45 Pin with QFP
c) 45 pin with LLC
d) 65 pin with DIP

59. Using what the processor wake-up from power-down?

a) External Interrupts
b) Internal interrupts
c) Serial Programming
d) Program Counter

60. What is the flash memory for LPC2141?

a) 34kB
b) 32kB
c) 128kB
d) 256kB

61. What are the categories in the vectored interrupt controller?

a) Fast interrupt request
b) Non vectored interrupt request
c) Non-vectored IQR
d) Fast interrupt request, Non vectored interrupt request and Non-vectored IQR

62. Each peripheral has an interrupt line?

a) True

b) False

63. What is pin connect block?

a) All pins are having a function without reserved

b) Some pins are Reserved

c) Pins have more than one function

d) Multiplexing of some pins

64. How many processors are used in the Instruction pipelining?

a) One

b) Two

c) Three

d) Four

65. Which signal is used for pipelining on bis cycle in ARM710T?

a) BWAIT

b) BTRAN

c) BLOK

d) BCLK

66. _____ pin can be used to extend memory access in whole cycle increments.

a) BTRAN

b) BLOK

c) BWAIT

d) BCLK

67. How many DC-DC converters interfaces in ARM7100?

a) 5

b) 3

c) 4

d) 2

68. The ARM7TDMI-S uses which pipelining?

a) 2-Stage

b) 3-Stage

c) 4-Stage

d) 5-Stage

69. The ARM7TDMI-S processor has _____ types of memory cycle.

a) 5
b) 3
c) 4
d) 2

70. The main importance of ARM micro-processors is providing operation with _____

a) Low cost and low power consumption
b) Higher degree of multi-tasking
c) Lower error or glitches
d) Efficient memory management

71. ARM processors where basically designed for _____

a) Main frame systems
b) Distributed systems
c) Mobile systems
d) Super computers

72. The ARM processors don't support Byte addressability.

a) True
b) False

73. The address space in ARM is _____

a) 2^{24}
b) 2^{64}
c) 2^{16}
d) 2^{32}

74. Memory can be accessed in ARM systems by _____ instructions.

i) Store
ii) MOVE
iii) Load
iv) arithmetic
v) logical
a) i, ii, iii
b) i, ii
c) i, iv, v
d) iii, iv, v

75. In the ARM, PC is implemented using _____

a) Caches
b) Heaps
c) General purpose register
d) Stack

76. The additional duplicate register used in ARM machines are called as _____

a) Copied-registers

b) Banked registers

c) EXtra registers

d) Extential registers

77. The banked registers are used for _____

a) Switching between supervisor and interrupt mode

b) Extended storing

c) Same as other general purpose registers

d) None of the mentioned

78. Each instruction in ARM machines is encoded into _____ Word.

a) 2 byte

b) 3 byte

c) 4 byte

d) 8 byte

79. All instructions in ARM are conditionally executed.

a) True

b) False

80. The addressing mode where the EA of the operand is the contents of Rn is _____

a) Pre-indexed mode

b) Pre-indexed with write back mode

c) Post-indexed mode

d) None of the mentioned

81. _____ symbol is used to signify write back mode.

a) #

b) ^

c) &

d) !

82. The instructions which are used to load or store multiple operands are called as _____

a) Banked instructions

b) Lump transfer instructions

c) Block transfer instructions

d) DMA instructions

83. The Instruction, LDM R10!, {R0,R1,R6,R7} _____

a) Loads the contents of R10 into R1, R0, R6 and R7

b) Creates a copy of the contents of R10 in the other registers except for the above mentioned ones

c) Loads the contents of the registers R1, R0, R6 and R7 to R10

d) Writes the contents of R10 into the above mentioned registers and clears R10

84. The instruction, MLA R0,R1,R2,R3 performs _____

a) R0<-[R1]+[R2]+[R3]

b) R3<-[R0]+[R1]+[R2]

c) R0<-[R1]*[R2]+[R3]

d) R3<-[R0]*[R1]+[R2]

85. The ability to shift or rotate in the same instruction along with other operation is performed with the help of _____

a) Switching circuit

b) Barrel switcher circuit

c) Integrated Switching circuit

d) Multiplexer circuit

86. _____ instruction is used to get the 1's complement of the operand.

a) COMP

b) BIC

c) ~CMP

d) MVN

87. The offset used in the conditional branching is _____ bit.

a) 24

b) 32

c) 16

d) 8

88. The BEQ instructions is used _____

a) To check the equality condition between the operands and then branch

b) To check if the Operand is greater than the condition value and then branch

c) To check if the flag Z is set to 1 and then causes branch

d) None of the mentioned

89. The condition to check whether the branch should happen or not is given by _____

a) The lower order 8 bits of the instruction

b) The higher order 4 bits of the instruction

c) The lower order 4 bits of the instruction

d) The higher order 8 bits of the instruction

90. Which of the two instructions sets the condition flag upon execution?

i) ADDS R0,R1,R2

ii) ADD R0,R1,R2

a) i

b) ii

c) Both i and ii

d) Insufficient data

91. _____ directive is used to indicate the beginning of the program instruction or data.

a) EQU

b) START

c) AREA

d) SPACE

92. _____ directive specifies the start of the execution.

a) START

b) ENTRY

c) MAIN

d) ORIGIN

93. _____ directives are used to initialize operands.

a) INT

b) DATAWORD

c) RESERVE

d) DCD

94. _____ directive is used to name the register used for execution of an instruction.

a) ASSIGN

b) RN

c) NAME

d) DECLARE

95. The pseudo instruction used to load an address into the register is _____

a) LOAD

b) ADR

c) ASSIGN

d) PSLOAD

96. Which of the following helps in the generation of waveforms?

a) timer

b) inputs

c) outputs

d) memory

97. Which bit size determines the slowest frequency?

a) counter size

b) pre-scalar value

c) counter

d) timer

98. Which bit size determines the maximum value of the counter-derived period?

a) counter size

b) pre-scalar value

c) bit size

d) byte size

99. Which of the following timer is suitable for IBM PC?

a) IA-32

b) Intel 8253

c) Intel 64

d) 8051 timer

100. Which of the following is mode 0 in 8253?

a) interrupt on start count

b) interrupt for wait statement

c) interrupt on terminal count

d) no interrupt

101. Which of the following is the pin efficient method of communicating between other devices?

a) serial port

b) parallel port

c) peripheral port

d) memory port

102. Which of the following depends the number of bits that are transferred?

a) wait statement

b) ready statement

c) time

d) counter

103. Which of the following is the most commonly used buffer in the serial porting?

a) LIFO

b) FIFO

c) FILO

d) LILO

104. What does SPI stand for?

a) serial parallel interface

b) serial peripheral interface

c) sequential peripheral interface

d) sequential port interface

105. Which allows the full duplex synchronous communication between the master and the slave?

a) SPI

b) serial port

c) I2C

d) parallel port

106. Which of the following processor uses SPI for interfacing?

a) 8086

b) 8253

c) 8254

d) MC68HC11

107. In which register does the data is written in the master device?

a) index register

b) accumulator

c) SPDR

d) status register

108. What happens when 8 bits are transferred in the SPI?

a) wait statement

b) ready statement

c) interrupt

d) remains unchanged

109. Which signal is used to select the slave in the serial peripheral interfacing?

a) slave select

b) master select

c) interrupt

d) clock signal

110. How much time period is necessary for the slave to receive the interrupt and transfer the data?

a) 4 clock time period
b) 8 clock time period
c) 16 clock time period
d) 24 clock time period

111. What does I2C stand for?

a) inter-IC
b) intra-IC
c) individual integrated chip
d) intel IC

112. Which company developed I2C?

a) Intel
b) Motorola
c) Phillips
d) IBM

113. Which of the following is the most known simple interface?

a) I2C
b) Serial port
c) Parallel port
d) SPI

114. Which are the two lines used in the I2C?

a) SDA and SPDR
b) SPDR and SCL
c) SDA and SCL
d) SCL and status line

115. Which of the following developed P82B715?

a) Philips
b) Intel
c) IBM
d) Motorola

116. Which pin provides the reference clock for the transfer of data?

a) SDA
b) SCL
c) SPDR
d) Interrupt pin

117. Which of the following are the three hardware signals?

a) START, STOP, ACKNOWLEDGE

b) STOP, TERMINATE, END

c) START, SCL, SDA

d) STOP, SCL, SDA

118. Which of the following performs the START signal?

a) master

b) slave

c) CPU

d) memory

119. Which of the following are handshake signals?

a) START

b) STOP

c) ACKNOWLEDGE

d) START and STOP

120. A packet is also referred to as

a) postcard

b) telegram

c) letter

d) data

121. Which of the following byte performs the slave selection?

a) first byte

b) second byte

c) terminal byte

d) eighth byte

122. Which of the following indicates the type of operation that the master requests?

a) address value

b) initial value

c) terminal count

d) first byte

123. How can both single byte and the double byte address slave use the same bus?

a) extended memory

b) extended address

c) peripheral count

d) slave bus

124. Which counter selects the next register in the I2C?

a) auto-incrementing counter

b) decrementing counter

c) auto-decrementing counter

d) terminal counter

125. Which is an efficient method for the EEPROM?

a) combined format

b) auto-incrementing counter

c) register set

d) single format

126. Which of the following uses two data transfers?

a) auto-incrementing counter

b) auto-decrementing counter

c) combined format

d) single format

127. Which of the following is efficient for the small number of registers?

a) auto-incrementing counter

b) auto-decrementing counter

c) combined format

d) single format

128. Which can determine the timeout value?

a) polling

b) timer

c) combined format

d) watchdog timer

129. How is bus lockup avoided?

a) timer and polling

b) combined format

c) terminal counter

d) counter

130. Which of the following can determine if two masters start to use the bus at the same time?

a) counter detect

b) collision detect

c) combined format

d) auto-incremental counter

131. Which ports are used in the multi-master system to avoid errors?

a) unidirectional port

b) bidirectional port

c) multi directional port

d) tridirectional port

132. Which of the following can be used for long distance communication?

a) I2C

b) Parallel port

c) SPI

d) RS232

133. Which of the following can affect the long distance communication?

a) clock

b) resistor

c) inductor

d) capacitor

134. Which are the serial ports of the IBM PC?

a) COM1

b) COM4 and COM1

c) COM1 and COM2

d) COM3

135. Which of the following can provide hardware handshaking?

a) RS232

b) Parallel port

c) Counter

d) Timer

136. Which of the following have an asynchronous data transmission?

a) SPI

b) RS232

c) Parallel port

d) I2C

137. How many areas does the serial interface have?

a) 1

b) 3

c) 2

d) 4

138. The RS232 is also known as

a) UART
b) SPI
c) Physical interface
d) Electrical interface

139. How much voltage does the MC1489 can take?

a) 12V
b) 5V
c) 3.3V
d) 2.2V

140. Which of the following is not a serial protocol?

a) SPI
b) I2C
c) Serial port
d) RS232

141. Which of the following is an ideal interface for LCD controllers?

a) SPI
b) parallel port
c) Serial port
d) M-Bus

142. How is data detected in a UART?

a) counter
b) timer
c) clock
d) first bit

143. Which of the signal is set to one, if no data is transmitted?

a) READY
b) START
c) STOP
d) TXD

144. What rate can define the timing in the UART?

a) bit rate
b) baud rate
c) speed rate
d) voltage rate

145. How is the baud rate supplied?

a) baud rate voltage
b) external timer
c) peripheral
d) internal timer

146. Which is the most commonly used UART?

a) 8253
b) 8254
c) 8259
d) 8250

147. Which company developed 16450?

a) Philips
b) Intel
c) National semiconductor
d) IBM

148. What does ADS indicate in 8250 UART?

a) address signal
b) address terminal signal
c) address strobe signal
d) address generating signal

149. Which of the following signals are active low in the 8250 UART?

a) BAUDOUT
b) DDIS
c) INTR
d) MR

150. Which of the signal can control bus arbitration logic in 8250?

a) MR
b) DDIS
c) INTR
d) RCLK

151. Which can prevent the terminal of data transmission?

a) flow control
b) increasing flow
c) increasing count
d) terminal count

152. Which of the following is the first flow control method?

a) software handshaking

b) hardware handshaking

c) UART

d) SPI

153. Which one of the following is the second method for flow controlling?

a) hardware

b) peripheral

c) software

d) memory

154. Which can restart the data transmission?

a) XON

b) XOFF

c) XRST

d) restart button

155. Which of the following is a common connector?

a) UART

b) SPI

c) I2C

d) DB-25

156. What does pin 22 in DB-25 indicate?

a) transmit data

b) receive data

c) ring indicator

d) signal ground

157. Which pin indicates the DSR in DB-25?

a) 1

b) 2

c) 4

d) 6

158. Which of the following connections are one to one?

a) Modem cables

b) SPI

c) UART

d) I2C

159. Which of the following are used to link PCs?

a) modem cable

b) null modem cable

c) serial port

d) parallel port

160. Which of the following method is used by Apple Macintosh?

a) hardware handshaking

b) software handshaking

c) no handshaking

d) null modem cable

161. Which of the following provides an efficient method for transferring data from a peripheral to memory?

a) dma controller

b) serial port

c) parallel port

d) dual port

162. Which of the following can be adopted for the systems which does not contain DMA controller for data transmission?

a) counter

b) timer

c) polling

d) memory

163. Which of the following have low-level buffer filling?

a) output

b) peripheral

c) dma controller

d) input

164. How many classifications of DMA controllers are made based on the addressing capability?

a) 2

b) 3

c) 4

d) 5

165. How many address register are there for the 1D type DMA controller?

a) 1

b) 2

c) 3

d) 4

166. Which of the following of a generic DMA controller contain a base address register and an auto-incrementing counter?

a) address bus
b) data bus
c) bus requester
d) address generator

167. Which of the following is used to transfer the data from the DMA controller to the destination?

a) data bus
b) address bus
c) request bus
d) interrupt signal

168. Which of the following is used to request the bus from the main CPU?

a) data bus
b) address bus
c) bus requester
d) interrupt signal

169. Which signal can identify the error?

a) data bus
b) address bus
c) bus requester
d) interrupt signal

170. Which signal allows the DMA controller to select the peripheral?

a) local peripheral control
b) global peripheral control
c) address bus
d) data bus

171. GPS module like SIM900/800 uses which protocol?

a) UART protocol
b) USART protocol
c) SPI protocol
d) I2C protocol

172. Finger print sensor uses which interface?

a) USART protocol
b) UART protocol
c) SPI protocol
d) I2C protocol

173. RS232 is used for long range wired communication.

a) True

b) False

174. UART is similar to _____

a) SPI protocol

b) I2C protocol

c) HTTP protocol

d) MQTT protocol

175. What does UART contain?

a) Parallel register

b) Shift register

c) Clock

d) Parallel shift register

176. Communication in UART is _____

a) Only simple

b) Only duplex

c) Only full duplex

d) Simplex, half duplex, full duplex

177. Start bit of UART is logic high.

a) True

b) False

178. Which error occurs when the receiver can't process the character?

a) Overrun error

b) Underrun error

c) Framing error

d) Break condition

179. What is WD1402A?

a) SPI

b) USART

c) SPIUART

d) I2C

180. What is the speed of the 8250 UART?

a) 4800bits/sec

b) 1200bits/sec

c) 12000bit/sec

d) 9600bits/sec

181. Which error occurs when UART transmitter has completed sending a character and the transmit buffer is empty?

a) Overrun error

b) Underrun error

c) Framing error

d) Break condition

182. Which error occurs when the designated start and stop bits are not found?

a) Overrun error

b) Underrun error

c) Framing error

d) Break condition

183. Which error occurs when the parity of the number of 1 bit disagrees with that specified by the parity bit?

a) Overrun error

b) Underrun error

c) Framing error

d) Parity error

184. A _____ occurs when the receiver input is at the space level.

a) Overrun error

b) Underrun error

c) Framing error

d) Break condition

185. The term break derives from _____ signaling.

a) Current loop

b) Voltage loop

c) Power loop

d) Current and Power loop

186. Two wire interface is also called as _____

a) UART

b) SPI

c) I2C

d) USART

187. I2c will address large number of slave devices.

a) True

b) False

188. SDA is having a _____transition when the clock line SCL is high.

a) high to low

b) low to high

c) low to low

d) high to high

189. Inter Integrated Circuit is a _____

a) Single master, single slave

b) Multi master, single slave

c) Single master, multi slave

d) Multi master, multi slave

190. Typical voltages used are _____

a) 5v

b) 3.3v

c) 5v or 3.3v

d) 2.5v

191. What is the speed of I2C bus?

a) 100 kbits/s

b) 10 kbits/s

c) 75 kbits/s

d) 100 kbits/s and 10 kbits/s

192. Master transmits means _____

a) Master node is sending data to a slave

b) Master node is receiving data from slave

c) Slave node is transmitting data to master

d) Slave node is sending data to master

193. Who sends the start bit?

a) Master receive

b) Master transmit

c) Slave transmit

d) Slave receive

194. Which is the I2C messaging example?

a) 24c32 EPROM

b) 24c32 EEPROM

c) 24c33 EEPROM

d) 24c33 EPROM

195. Are pull up registers required in I2C?

a) True

b) False

196. How many types of addressing structures are there in I2C?

a) 4 types

b) 3 types

c) 2 types

d) 5 types

197. All operating modes work under _____

a) 11 kbit/s

b) 100 kbit/s

c) 15 kbit/s

d) 150 kbit/s

198. Which mode is highly compatible and simply tightens?

a) Fast mode

b) High speed mode

c) Ultra fast mode

d) Both fast and high speed mode

199. What is the speed for fast mode?

a) 100 kbit/s

b) 400 kbit/s

c) 150 kbit/s

d) 200 kbit/s

200. What is the speed for High-Speed mode?

a) 100 kbit/s

b) 3.4 Mbit/s

c) 150 kbit/s

d) 200 kbit/s

201. Secure digital card application uses which protocol?

a) UART

b) SPI

c) I2C

d) USART

202. SPI device communicates in _____

a) Simplex
b) Half duplex
c) Full duplex
d) Both half and full duplex

203. Do SPI have/has a single master?

a) True
b) False

204. SPI is described as Asynchronous serial interface.

a) True
b) False

205. How many logic signals are there in SPI?

a) 5 signals
b) 6 signals
c) 4 signals
d) 7 signals

206. SPI uses how many lines?

a) 4 lines
b) 1 line
c) 3 lines
d) 2 lines

207. MOSI means _____

a) Line for master to send data to the slave
b) Line for the slave to send data to the master
c) Line for the clock signal
d) Line for the master to select which slave to send data to

208. MISO means _____

a) Line for master to send data to the slave
b) Line for the slave to send data to the master
c) Line for the clock signal
d) Line for the master to select which slave to send data to

209. Which of the following is an advantage of SPI?

a) No start and stop bits
b) Use 4 wires
c) Allows for single master
d) Error checking is not present

210. Which of the following is the disadvantage in SPI?

a) Full duplex communication
b) Push pull drivers
c) Unidirectional signals
d) More pins

211. Which of the following is the type of SPI controller?

a) Queued SPI
b) Microwire
c) Microwire/plus
d) Quad SPI

212. _____ is a predecessor of SPI.

a) Queued SPI
b) Microwire
c) Microwire/plus
d) Quad SPI

213. Which has a half duplex communication?

a) Queued SPI
b) Microwire
c) Microwire/plus
d) Quad SPI

214. Do SPI have internal flash?

a) True
b) False

215. SMBUS stands for _____

a) Serial Memory Bus
b) Serial Management Bus
c) System Management Bus
d) System Memory Bus

216.