RNSIT
Bengaluru

ESTD.: 2001
An Institute with a Difference

Dr. R N Shetty
Founder

VII Semester

VLSI Lab Manual

18ECL77

20 Years of Academic Excellence

Faculty-in-charge

Mrs. Sangeetha B G

Mrs. Ibrar Jahan

Mrs. Ohileshwari M S

Department of
Electronics & Communication Engineering

RNS INSTITUTE OF TECHNOLOGY
Dr. Vishnuvardhan Road, Channasandra, RR Nagar, Bengaluru - 560 098

RNS INSTITUTE OF TECHNOLOGY

Dr. VISHNUVARDHAN ROAD, CHANNASANDRA, BENGALURU -560 098

Department of Electronics and Communication Engineering

VISION of the College

Building RNSIT into a World - Class Institution

MISSION of the College

To impart high quality education in Engineering, Technology and Management with a difference, enabling students to excel in their career by

1. Attracting quality Students and preparing them with a strong foundation in fundamentals so as *to achieve distinctions in various walks of life* leading to outstanding contributions.
2. Imparting value based, need based, and choice based and skill based professional education to the aspiring youth and *carving them into disciplined, World class Professionals* with *social responsibility.*
3. Promoting excellence in Teaching, Research and Consultancy that galvanizes academic consciousness among Faculty and Students.
4. Exposing Students to emerging frontiers of knowledge in various domains and make them suitable for Industry, Entrepreneurship, Higher studies, and Research & Development.
5. Providing freedom of action and choice for all the Stake holders with better visibility.

VISION of the Department

Conquering technical frontiers in the field of Electronics and Communications

MISSION of the Department

1. To achieve and foster excellence in core Electronics and Communication engineering with focus on the hardware, simulation and design.
2. To pursue Research, development and consultancy to achieve self sustenance.
3. To create benchmark standards in electronics and communication engineering by active involvement of all stakeholders.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

ISE Graduates within three-four years of graduation will have

- **PEO1**: Acquired the fundamentals of computers and applied knowledge of Information Science & Engineering and continue to develop their technical competencies by problem solving using programming.
- **PEO2**: Ability to formulate problems attained the Proficiency to develop system/application software in a scalable and robust manner with various platforms, tools and frameworks to provide cost effective solutions.
- **PEO3**: Obtained the capacity to investigate the necessities of the software Product, adapt to technological advancement, promote collaboration and interdisciplinary activities, Protecting Environment and developing Comprehensive leadership.
- **PEO4**: Enabled to be employed and provide innovative solutions to real-world problems across different domains.
- **PEO5**: Possessed communication skills, ability to work in teams, professional ethics, social responsibility, entrepreneur and management, to achieve higher career goals, and pursue higher studies.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

- **PO1: Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems
- **PO2: Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
- **PO3: Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.
- **PO4: Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- **PO5: Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.
- **PO6: The engineer and society:** Apply reasoning informed by the contextual knowledge to assess Societal, health, safety, legal and cultural issues and the

consequent responsibilities relevant to the professional engineering practice.

- **PO7: Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- **PO8: Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- **PO9: Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- **PO10: Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- **PO11: Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- **PO12: Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

ECE Graduates will have

- **PSO1:** Apply fundamental knowledge of Electronics, Communications, Signal processing, VLSI, Embedded and Control systems etc., in the analysis, design, and development of various types of real-time integrated electronic systems and to synthesize and interpret the experimental data leading to valid conclusions.
- **PSO2:** Demonstrate competence in using Modern hardware languages and IT tools for the design and analysis of complex electronic systems as per industry standards along with analytical and managerial skills to arrive at appropriate solutions, either independently or in team.

RNS INSTITUTE OF TECHNOLOGY

Dr. VISHNUVARDHAN ROAD, CHANNASANDRA, BENGALURU -560 098

Department of Electronics and Communication Engineering

VLSI Laboratory

Subject Code: 18ECL77 **Total Hours: 40**
Hours/Week: 01I + 2P **Exam Hours: 03**

Subject Code	18ECL77
I.A. Marks (CIE)	40
Exam Marks (SEE)	60

Course objectives:

This course will enable students to:

- Design, model, simulate and verify digital circuits
- Design layouts and perform physical verification of CMOS digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the stages in ASIC

Course Outcomes

After studying this course, students will be able to:

CO1	Design and Simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
CO2	Functional verification of operational amplifier and analog/digital converters to meet desired parameters using basic amplifiers.
CO3	Interpret delay concepts using DC Analysis, AC Analysis and Transient Analysis in analog circuits.
CO4	Design and simulate combinational and sequential digital Verilog HDL.
CO5	Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list

CO mapping to PO/PSOs

CO / PO & PSO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
15ECL77.1	1				2					1			2	2
15ECL77.2	1	1		1	2					1			2	2
15ECL77.3	1			1	2					1			2	3
15ECL77.4	1				2					1			2	3
15ECL77.5	1			1	2					1			1	3

VLSI Laboratory

Subject Code: 18ECL77 **Total Hours: 40**
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Subject Code	18ECL77
I.A. Marks	40
Exam Marks	60

List of Programs

Sl. No	Name of Experiment	CO
	PART - A **ASIC-ANALOG DESIGN**	
1	.1 a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of Inverter with Wn = Wp, Wn=2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time,fall time of 1 ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter? 1.b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.	CO1, CO3
2	2.a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results. 2.b)Draw the layout of NAND with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.	CO1, CO3
3	3.a)Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. 3.b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.	CO1, CO3

4	4.a)Capture schematics of two-stage operational amplifier and measure the following: i. UGB ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. 4.b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), chose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.	CO2, CO3
	PART - B **ASIC-DIGITAL DESIGN**	
1	4 Bit UP/DOWN Counter Asynchronous Reset Counter • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the Gate Level Netlist by setting Area and Timing Constraints and also find the Critical Path and Maximum Frequency of Operation • Perform the above for 32Bit UP/DOWN Counter	CO4, CO5
2	4 Bit Adder • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the netlist. • From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required	CO4, CO5
3	UART • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing • constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, • Identify Critical path	CO4, CO5
4	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog Code • Verify functionality using Test-bench	CO4, CO5

	• Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path	
5	Latch and Flip-Flop • Synthesize the design and compare the synthesis report (D, SR. JK)	CO4, CO5
6	For synthesized netlist carry out the following: • Floor planning • Placement and Routing • Record the parameters such as no. of metal layers used for routing, flip method for placement of standard cells • Physical Verification and record the DRC and LVS reports • Generate GDSII	CO4, CO5

VLSI Laboratory
Evaluation Rubrics

Subject Code: 18ECL77 **I.A. Marks : 20**
Hours/Week: 01I+2P **Exam Hours: 03**
RBT Level: L1,L2,L3 **Exam Marks: 80**

Lab Write-up and Execution Rubrics (Max: 10 marks)

		Above Average	Average	Below Average
a.	**Understanding of design and approach to solve. (4 Marks)**	Able to analyze the given design and efficiently implement using Cadence tool. (4)	Able to analyze the design and moderate understanding of tool. (3-2)	Poor understanding of design or tool. (1-0)
b.	**Execution and Viva (5 questions) (2 Marks)**	Design executed for specified inputs with valid results and able to answer all five questions appropriately. (2)	Design is executed for some inputs and able to answer three-two questions. (1)	Design has errors or no Execution and not answered any questions. (0)
c.	**Results and Documentation (4 Marks)**	Obtained results for respective design are legibly written / documented. (4)	Obtained results for respective design is acceptably documented. (3-2)	No Proper results and poor documentation. (1-0)

LAB Internal Assessment rubrics (Max: 10 marks)

		Above Average	Average	Below Average
a.	**Write-up (3 Marks)**	Able to write the complete design. (3)	Able to write the design with few errors. (2-1)	Unable to write. (1-0)
b.	**Execution (5 Marks)**	Executed successfully for all the specification given. (5)	Obtained partially correct results. (3-2)	Program has compilation errors or No Execution. (1-0)
c.	**Viva (5 questions) (2 Marks)**	Able to answer all five questions correctly. (2)	Able to answer three-two questions. (1)	Not answered any. (0)

PART-A

INTRODUCTION TO VLSI LAB

VLSI lab allows the theoretical concepts studied as part of subjects CMOS VLSI Design, Microelectronics Circuits and HDL, to experience in practical with the help of Cadence tool framework. The lab introduces the complete custom IC design flow, ASIC design flow and AMS (Analog and Mixed Signal) flow for Analog circuits, Digital circuits and Analog and mixed signal circuits design respectively.

The analog design involves schematic (standard cell), test schematic capture and symbolic representation of circuit topologies using Virtuoso schematic editor/ Composer. Simulation of the test circuit to perform various analyses such as transient, DC and AC is facilitated by Multimode Simulator/Spectre. Once the simulation results are obtained as per the specifications the physical design is carried out using Virtuoso Layout suite followed by the physical verification using Assura DRC (Design Rule Check), LVS (Layout Versus Schematic) and Parasitic RC extraction. The floor planning, Power planning, placement and routing can be performed later using Encounter.

The digital design involves the realization of various digital circuit components using Register Transfer Logic (RTL) code, Compilation of the same using Native Compiler, elaboration using elaborator and simulation using Incisive. The synthesis of the verified RTL code to obtain the gate level netlist is performed thereon.

The AMS circuit design is performed by importing the digital modules as configuration files into the analog environment, followed by the steps of the analog design and simulating the same using AMS simulator instead of Spectre.

Introduction to Cadence Design Systems

Cadence is an Electronic Design Automation (EDA) environment which allows different applications and tools to integrate into a single framework thus allowing supporting all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the cadence environment. This set of files is commonly referred to as a design

kit. The Cadence Development System consists of a bundle of software packages such as schematic editors, simulators, and layout editors. This software manages the development process for analog, digital, and mixed-mode circuits. In this lab, we will strictly use the tools associated with analog circuit design and digital design. All the Cadence design tools are managed by a software package called the Design Framework II. This program supervises a common database which holds all circuit information including schematics, layouts, and simulation data.

LINUX Operating System

Using the LINUX operating system is similar to using other operating systems such as DOS. LINUX commands are issued to the system by typing them in a "shell". LINUX commands are case sensitive so be careful when issuing a command, usually they are given in lower-case.

The following list summarizes all the basic commands required to manage the data files you will be creating in this lab course. All LINUX commands are entered from the shell window (Terminal window).

Caution: Do not use LINUX commands for modifying, deleting, or moving any Cadence data files.

Table 1 Common LINUX commands

Commands	Description
ls [-la]	Lists files in the current directory. "l" lists with properties and "a" also lists hidden files (ones beginning with a ".")
cd XXXX	Changes the current directory to XXXX.
cd..	Changes the current directory back to one level.
cp XXXX YYYY	Copies the file XXXX to YYYY
mv XXXX YYYY	Moves file XXXX to YYYY. Also used for rename
rm XXXX	Deletes the file XXXX
mkdir XXXX	Creates the directory XXXX.
lp -dXXXX YYYY	Prints the textfile or postscript file YYYY to the printer named XXXX, where XXXX can be either "ipszac" or "hpszac"

Note: The command "&" tells LINUX to execute the command and return the prompt to the active shell.

ANALOG DESIGN
Custom IC Design Flow

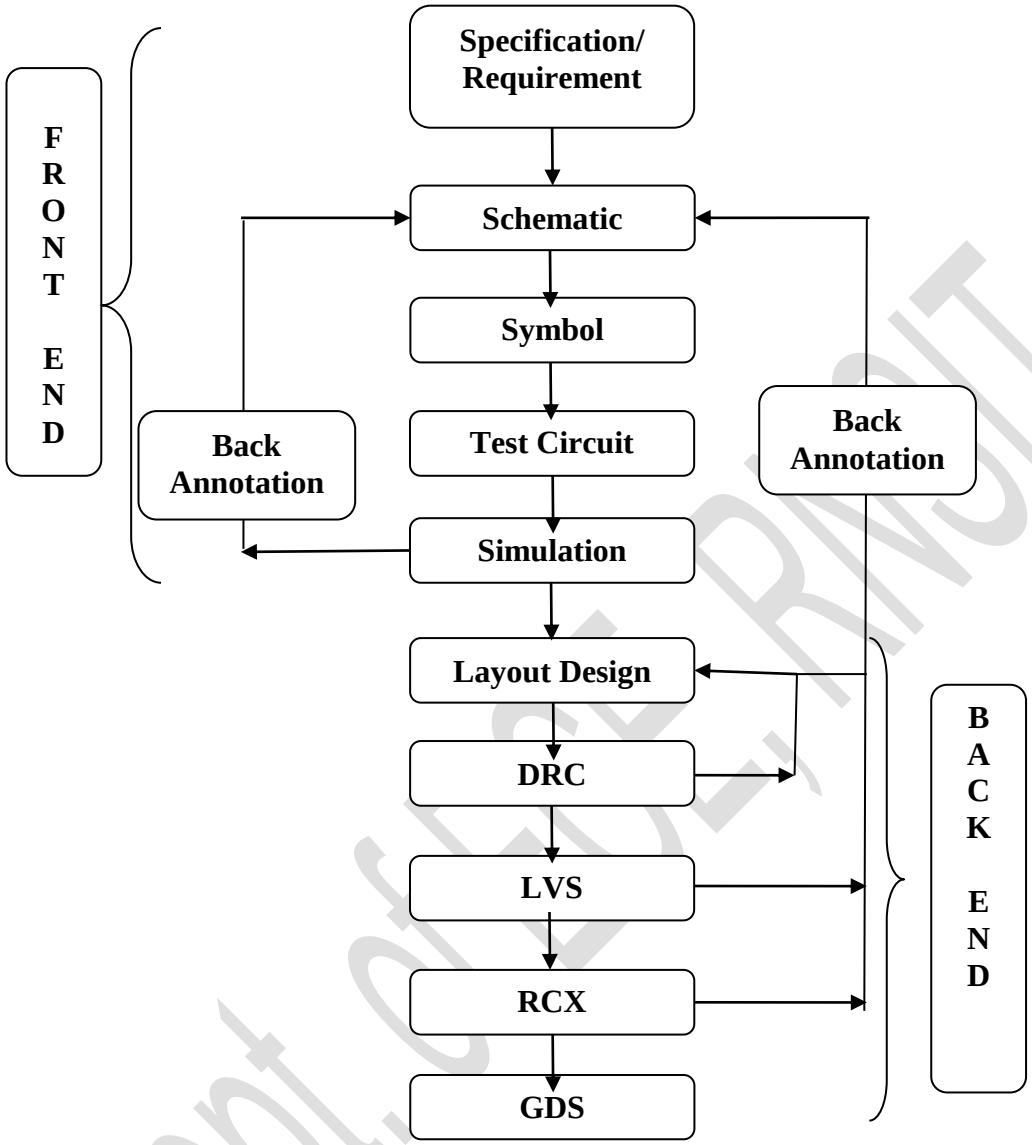


Fig.1 Flow Diagram of Analog Design flow

Procedure for analog design

1. Login to your workstation using the username and password. The home directory has a **csh** file with paths to the cadence installation.

2. In a terminal window, type **csh** at the command prompt to invoke C shell.
   > csh
   >source /home/installs/cshrc
   >ls
   In the terminal window, enter:
   >virtuoso &
   The virtuoso or **Command Interpreter Window (CIW)** appears at the bottom of the screen.

3. If the "What's New…" window appears, close it with the **File-Close** command.
4. Keep opened **CIW** window for the labs.

Creating a new Library:

1. In the **CIW** window click on **Tools-Library manager**. The library manager window will be opened.
2. Click **File-New-Library**. Specify the name for the new library. Click **ok.**
3. In the next "**Technology File for New Library**" form, select option **Attach an existing technology file** and click **ok.**
4. In the "**Attach Design Library to technology file**" form, select **gpdk180** from the cyclic field and click **ok**
5. After creating a new library you can verify it from the Library manager.

Creating a Schematic Cellview:

1. In the CIW or Library manager, select the library created and execute **File-New-Cellview**.
2. Setup the new file form.
3. Click **ok**. A blank schematic window for the design appears.

Adding Components to Schematics:

1. In the design window, click the **create instance,** fix menu icon to display add instance form.
2. Click on the **browse** button. This opens up a library browser from which you can select the components **(gpdk180)** and the symbol view **(library created you).**
3. After you complete the add instance form, move your cursor to the schematic window and click left to place a component. If you place a component with wrong parameter values, use the **Edit-Properties-Objects** command to change the parameter. Use **Edit-Move** command if you place components in the wrong location. You can rotate components using **Edit-Rotate** command.

4. After entering components, click **cancel** in the Add instance form or press **Esc**.

Adding Pins to Schematic:

1.Click the Pin fixed menu icon in the schematic window
2.Make sure that the direction field is set to **input/output/inout** when placing the pins respectively.
3.Select cancel from the **Add-Pin** form after placing the pins.

Adding Wires to a Schematic:

1.Click the **wire** (narrow) icon in the schematic window.
2.In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.
3.Follow the prompts at the bottom of the design window and click **left** on the destination point for your wire. A wire is routed between the source and destination points.
4.Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.
5.Click the **Check and Save** icon in the Schematic editor window.
6.Observe the CIW output area for any errors.

Symbol Creation:

1.In the schematic window, execute
Create -Cellview -From Cellview.
The **Cellview** form appears. With the Edit options function active, you can control the appearance of the symbol to generate.
2.Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **Schematic symbol.** Click **ok**.
3.Modify the **pin specification**.
4.Click **ok**.

Editing a Symbol:

1. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, click **left** to select it.
2. Click **Delete** icon in the symbol window, similarly select the red rectangle and delete that.
3. Execute **Create-Shape-Polygon.**
4. After creating the shape press **ESC** key.
5. You can move the pin names according to the location.
6. Execute **Create-Selection Box**. In the Add Selection Box form, click **Automatic**. A new red selection box is automatically added.

7. After creating symbol, click on the save icon in the symbol editor window to save the symbol. In the symbol editor, execute **File-Close** to close the symbol view window.

Test Circuit Creation:

1. In the CIW or Library manager, select the library created and execute **File-New-Cellview**.
2. Setup the new file form.
3. Click **ok**. A blank schematic window for the design appears.

Adding Components to Test circuit:

1. In the design window, click the **create instance,** fix menu icon to display add instance form.
2. Click on the **browse** button. This opens up a library browser from which you can select the symbol view **(library created you)** and the components **(gpdk180).**
3. Make the connection according to the test circuit.

Simulation with Spectre:

1. In the schematic window, execute **Launch-ADE L**
2. In **Analog Design Environment (ADEL)** window, Click the **Choose- Analysis** icon.
3. To setup for **transient analysis** select **tran** icon, click at the **moderate or enabled** button at the bottom, click **Apply**.
4. To setup for **DC analysis** select dc, turn on **Save DC Operating Point**.

Turn on the **Component Parameter**. Click the **select Component**, which takes you to the schematic window. Select input signal, **Vpulse** or DC analysis. Select **start and stop** voltages. Click **Apply** and **ok**.

Selecting outputs for plotting:

1. In **Analog Design Environment (ADEL)** window,
2. Execute **Outputs- To be plotted- Select** input and output line on Schematic in the simulation window.
3. Follow the prompt at the bottom of the schematic window, click on the **output net**, **input net** of the design. Press **ESC** with the cursor in the schematic after selecting it.
4. Execute **Simulation-Netlist and Run** to start the simulation.

Saving and Loading Simulator State:

1. In the simulation window, execute **Session- Save State**. Set the Save as field and click **ok.**
2. In the simulation window execute **Session- Load State**, set the state name and click **ok**.

Creating a Layout View:

1. From the schematic window menu execute **Launch- Layout XL**. A startup Option form appears.
2. Select **Create New** option.
3. Check the cell name, View name. Click **ok**.

Adding Components to Layout:

1. Execute **Connectivity-Generate-All from Source**. Generate Layout form appears. Click **ok**, which imports the schematic components into the layout window automatically.
2. Rearrange the components within **PR boundary.**
3. To rotate a component, select the component and execute **Edit-Properties**. Now select the degree of rotation.
4. To move a component, select the component and execute **Edit-Move** command.

Making Interconnection:

1. Execute **Connectivity-Nets-Show/Hide Selected incomplete nets**.
2. Move the mouse pointer over the device and click **LMB** to get the connectivity information, which shows the guidelines for the interconnections of the components.
3. From the layout window execute **Create-Shape-Path** or **Create-Shape-Rectangle** and select the appropriate layers from the **LSW** window and **Vias** for making interconnections.

Creating Contacts/Vias:

1. Execute **Create-Via** to place different contacts as given in the table below.

Connection	Contact Type
For Metal1- Poly	Metal1- Poly
For Metal1- P substrate	Metal1- Psub
For Metal1- N Well	Metal1- Nwell

2. Save the design by selecting **File-Save**.

Running DRC:

1. Select **Assura-Run DRC** from Layout window. The **DRC** form appears. The Library and cell name are taken from the current design window, but rule file may be missing. Select the technology as **gpdk180**. This automatically loads the rule file.

2. Click **ok** to start **DRC**. A progress form will appear. You can click on the watch clock file to see the Log file.
3. When DRC finishes, a dialog box appears, Click **Yes** to view the results.
4. If there are any DRC error exits in the design **View Layer Window (VLW)** and **Error Layer Window (ELW)** appears. Also the errors highlight in the design itself.
5. Click **View- Summary** in the **ELW** to find the details of errors.
6. You can refer to rule file also for more information, correct all DRC errors and **Re – run** the DRC.
7. If there are no errors in the layout then a dialog box appears with No DRC errors found written in it, Click on **close** to terminate the DRC run.

ASSURA LVS:

1. Select **Assura-Run LVS** from the layout window. The Assura Run LVS form appears, it will automatically load both the schematic and layout view of the cell.
2. Click **OK**. The LVS begins and a progress form appears.
3. If the schematic and layout matches completely, you will get the form displaying Schematic and Layout Match.
4. If the schematic and Layout do not matches, a form informs that the LS completed successfully and results form will appear, click **YES** in the form.
5. In the LVS debug form, find the details of mismatches and correct all those mismatches and **Re-Run** the LVS.

ASSURA RCX:

1. From the layout window execute **Assura-Run RCX**.
2. Change the **Assura Parasitic Extraction form**, select Output Type under Setup tab of the form.
3. In the **Extraction tab** of the form, choose **Extraction type (RC)**, **Cap coupled mode** (coupled) and specify the reference node for extraction.
4. In the **filtering tab** of the form, Enter **Power Nets** as **Vdd!, Vss!** and Enter **Ground Nets** as **gnd!**
5. Click **ok**. The **RCX** progress form appears, in the progress form click **Watch log file** to see the output log file.
6. When RCX completes, a dialog box appears, shows Assura RCX Run completed successfully.
7. Open the **av_extracted** view from the Library manager and view the parasitic.

Configuration View:

1. In the CIW or Library manager, execute **File-New-Cell view**.
2. Click **ok** in Create New File form. The **Hierarchy editor** form opens and a **New Configuration** form opens in front of it.
3. Click **Use template** at the bottom of the **New Configuration** form and select **Spectre** in the cyclic field and click **ok.**

4. Change the **Top Cell view** to **schematic** and remove the default entry from the Library List field.
5. Click **ok.** The Hierarchy editor displays the Hierarchy for the design using table format.
6. Click the **Tree View** tab. The Design hierarchy changes to Tree format. Save the current configuration.
7. Close the Hierarchy window, execute **File-Close window.**

To run the circuit without parasitics:

1. From the Library manager open **cell config** view.
2. In the form, turn on the both cyclic buttons to **Yes** and click **ok.**
3. Execute **Launch-ADE L** from the schematic window.
4. Follow the same procedure for running the simulation. Execute **Session-Load** state.
5. Click **Netlist and Run** icon to start the simulation.
6. In the CIW, note the netlisting statistics in the circuit inventory section. This list includes all nets, design devices, source and loads. There are no parasitic components.

Measuring the Propagation Delay without parasitics:

1. In the waveform window execute **Tools-Calculator.**
2. From the functions select **delay,** this will open the delay data panel.
3. Place the cursor in the text box for **signal1**, select the wave button and select the input waveform from the waveform window.
4. Repeat the same for **signal2**, select the output form.
5. Set the **Threshold value1 (vdd/2)** and **Threshold value2 (vdd/2)**.
6. **Edge Type:**
   For tpHL signal1- High and signal2 – Low
   For tpLH signal1 – Low and signal2 - High
7. Execute **ok** and observe the expression created in the calculator.
8. Click on **Evaluate the Buffer** icon to perform the calculation. Close calculator window.

To run the circuit with parasitics:

1. From the Library manager open **cell config** view.
2. In the form, turn on the both cyclic buttons to **Yes** and click **ok.**
3. Click the **Tree View** tab. The Design hierarchy changes to Tree format.
4. Right click on **Io, set instance view,** select **av_extracted,** and Click **Recompute the hierarchy** and Save the current configuration.
5. Close the Hierarchy window, execute **File-Close window.**
6. Execute **Launch-ADE L** from the schematic window.
7. Follow the same procedure for running the simulation. Execute **Session-Load** state.
8. Click **Netlist and Run** icon to start the simulation.
9. In the CIW, note the netlisting statistics in the circuit inventory section. This list includes all nets, design devices, source and loads. There are parasitic components.

Calculating the Propagation Delay:

1. In the waveform window execute **Tools-Calculator.**
2. From the functions select **delay,** this will open the delay data panel.
3. Place the cursor in the text box for **signal1**, select the wave button and select the input waveform from the waveform window.
4. Repeat the same for **signal2**, select the output form.
5. Set the **Threshold value1 (vdd/2)** and **Threshold value2 (vdd/2)**.
6. Set **Edge number** as 2; **Edge Type** as rising and falling
7. Execute **ok** and observe the expression created in the calculator.
8. Click on **Evaluate the Buffer** icon to perform the calculation. Close calculator window.

1. Goto ADEL window, right click on outputs,
2. Click on **Get expression**, name the expression as tpHL and tpLH (tpHL will have Edge Type1 as rising and Edge Type2 as falling, similarly, tpLH will have Edge Type1 as falling and Edge Type2 as rising) and tp expression as (tpHL +tpLH)/2
3. Press OK
4. Again run ADEL, it displays delay value on the screen

Calculating the Power:

1. In ADEL window, select **outputs**, from the tab select **save all.**
2. In pop-up window, select **all** block for first and second line. Apply **ok.**
3. Run the simulation once again.
4. In the waveform window, choose **browser** from classic panel, double click on **tran,** click on :**pwr.**
5. Power waveform appears on waveform window.
6. Execute **Tools-Calculator.**
7. Select the wave button on calculator and select the power waveform from the waveform window.
8. This will display **getdata** on calculator window.
9. From the functions select **average,** this will open the data panel.
10. Click on **Evaluate** and observe the expression created in the calculator.

Calculating the Gain:

1. Go to **ADEL** window.
2. Run **simulation**
3. In the waveform window, open a **new sub window**.
4. From the **ADEL** window go to **Results -> Direct Plot** ->Select **AC Gain and Phase**, and select Vo and Vin from test circuit.
5. **Gain waveform** appears on the simulation window.

Experiment – 1

Objectives:

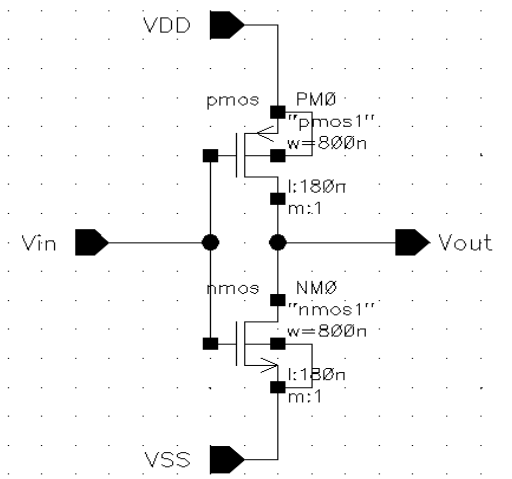
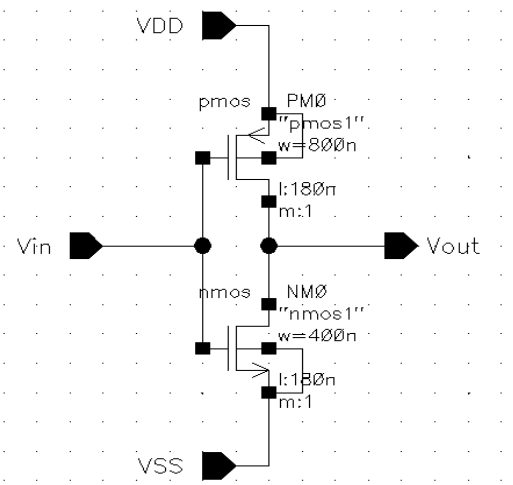
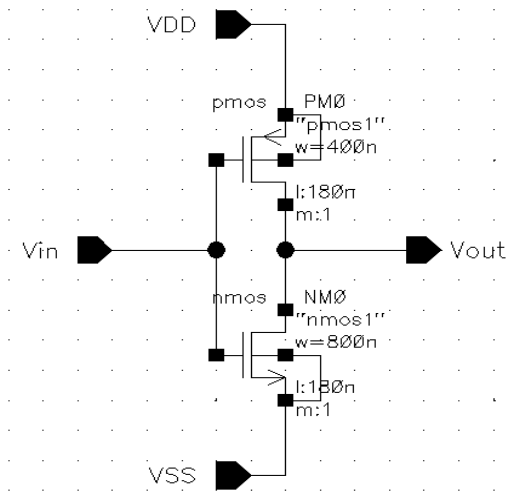
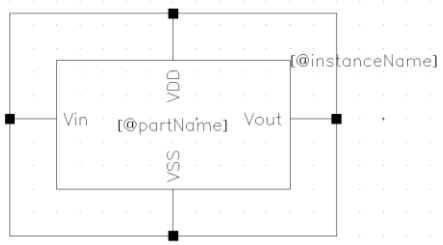
1 a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of Inverter with Wn = Wp, Wn=2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

i. Set the input signal to a pulse with rise time,fall time of 1 ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter?

ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width?

iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

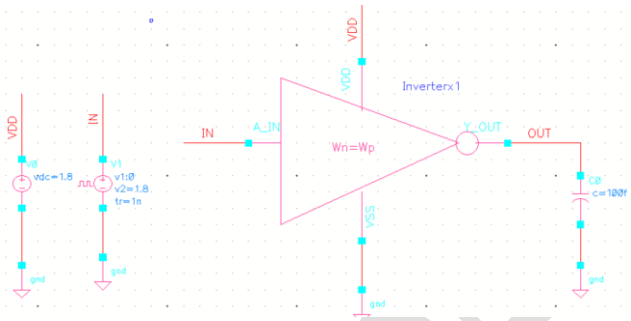
1.b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Schematic	Symbol
Wn=Wp 	**Wn=2Wp** 
Wn=Wp/2 	**Symbol** 

Length and Width of NMOS and PMOS Transistors for the condition

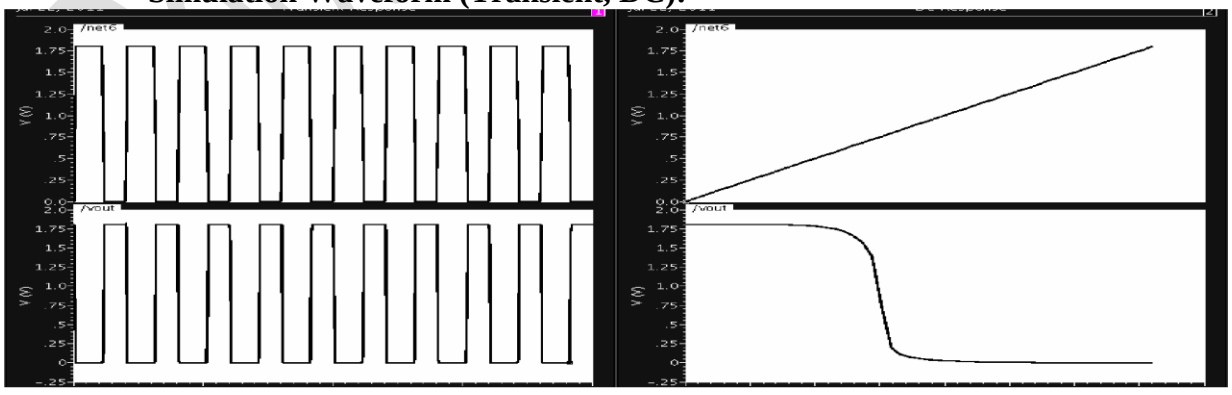
		Wn=Wp	**Wn=Wp/2**	**Wn=2Wp**
Library Name	**Cell Name**	**Properties/comments**	**Properties/comments**	**Properties/comments**
gpdk180	nmos	Model Name= nmos1 (NM0); W= 800n; L=180n	Model Name= nmos1 (NM0); W= 400n; L=180n	Model Name= nmos1 (NM0); W= 800n; L=180n
gpdk180	pmos	Model Name = pmos1 (PM0); W= 800n; L=180n	Model Name = pmos1 (PM0); W= 800n; L=180n	Model Name = pmos1 (PM0); W= 400n; L=180n

Test Circuit



Library Name	**Cell Name**	**Properties/comments**
USN	Inv	symbol
analoglib	Vpulse	V1 = 0V, V2 =1.8V, Delay = 0s, Rise time=1ns; fall time=1ns; Pulse Width = 10ns, Period = 20n s
analoglib	Vdc, gnd	DC Voltage=1.8V
analoglib	Cap	100fF
analoglib	Gnd	

Simulation Waveform (Transient, DC):

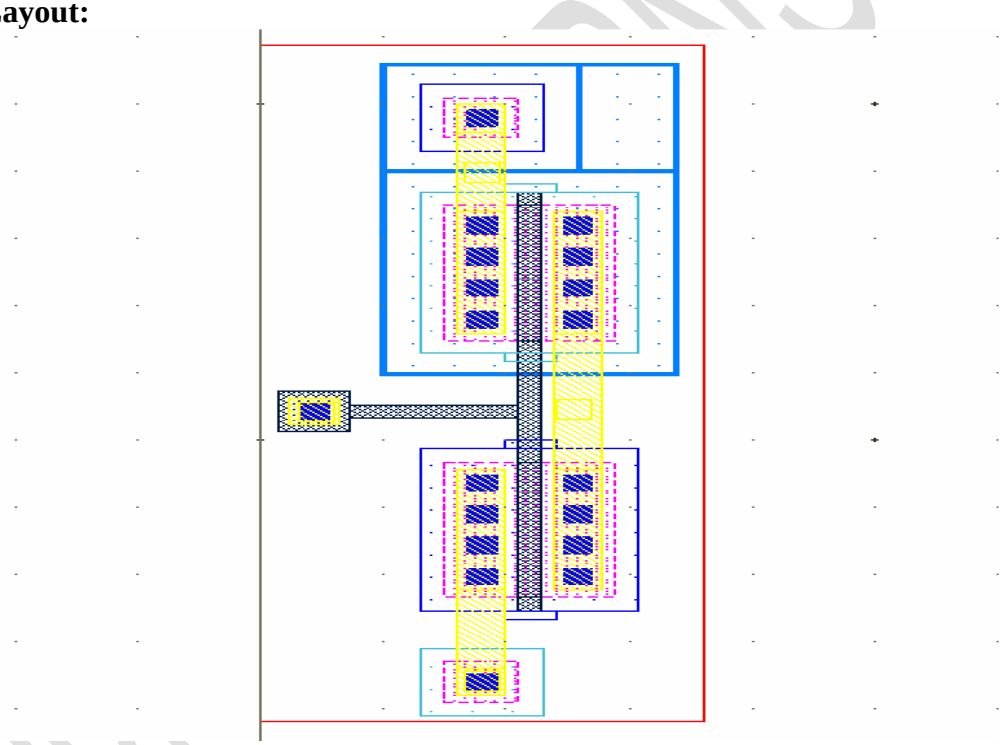


Analysis	Start time	Stop time
Transient	-	200ns
Dc	0	1.8V

Values of t_{pHL}, t_{pLH} and t_{PD} for different geometries

Width Settings	MOSFET	Width	t_{pHL}	t_{pLH}	t_{pd}
Wn=Wp	PMOS	800n	26.07 ps	71.04 ps	48.55 ps
	NMOS	800n			
Wn=Wp/2	PMOS	800n	45.77 ps	67.38 ps	56.57 ps
	NMOS	400n			
Wn=2Wp	PMOS	400n	24.59 ps	129.9 ps	77.29 ps
	NMOS	800n			

Layout:



EXPERIMENT – 2

Objective:

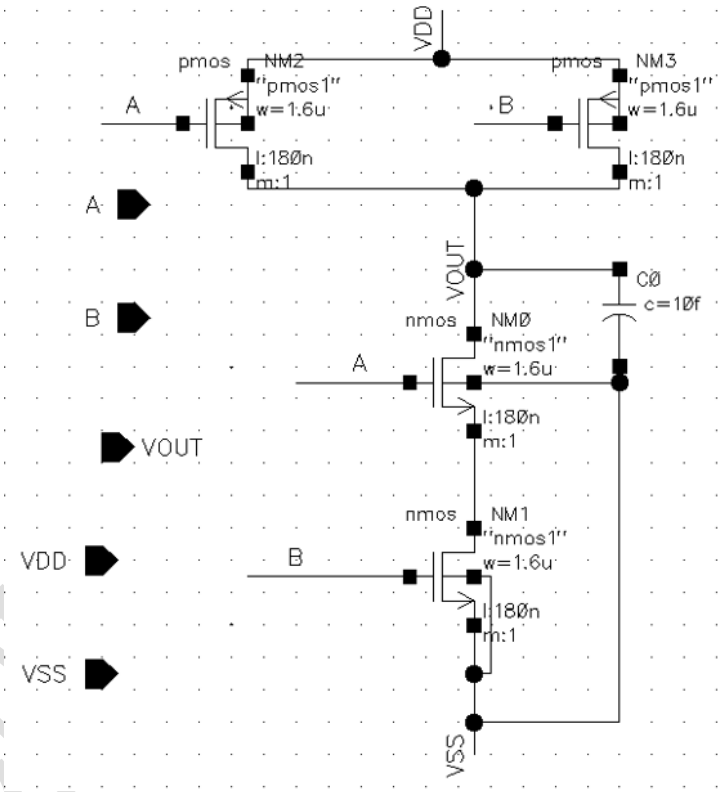
Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment

1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

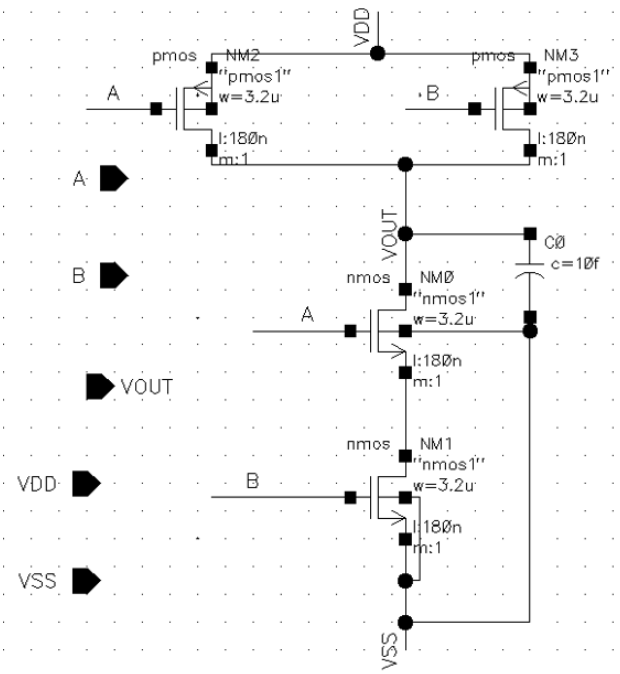
2 Draw the layout of NAND with Wp/Wn=40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Schematic

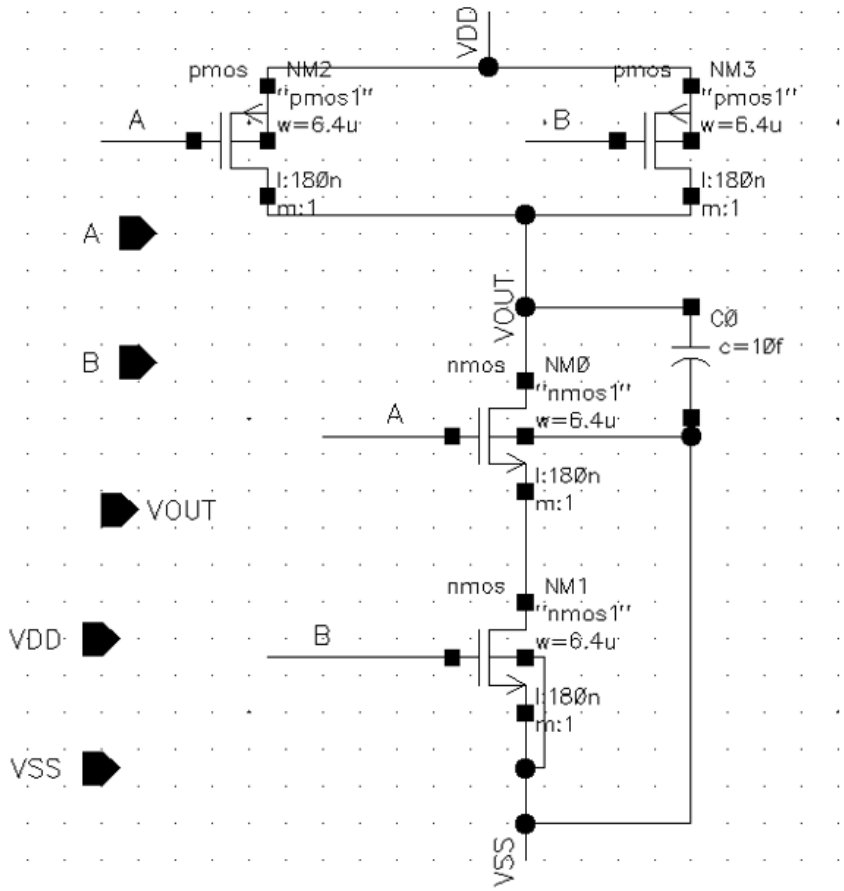
NAND2_1X



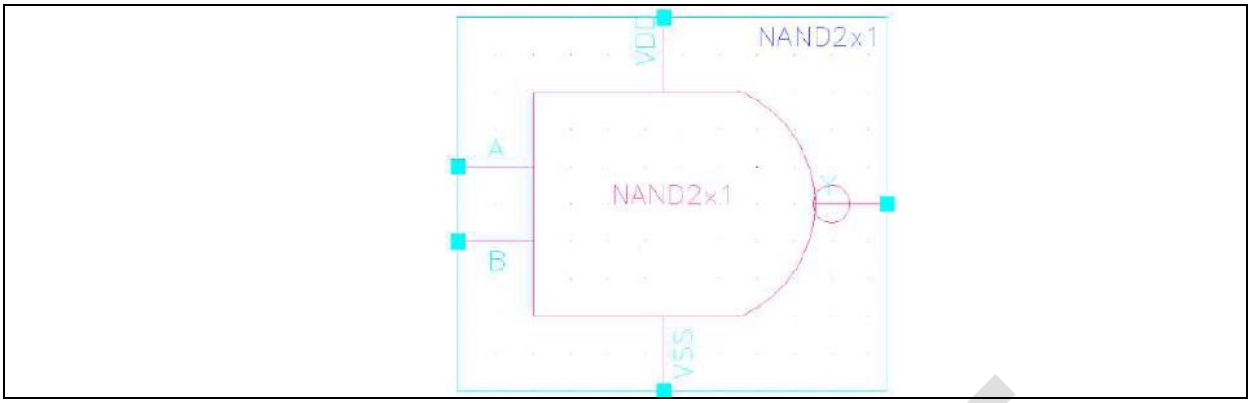
NAND2_2X



NAND2_4X



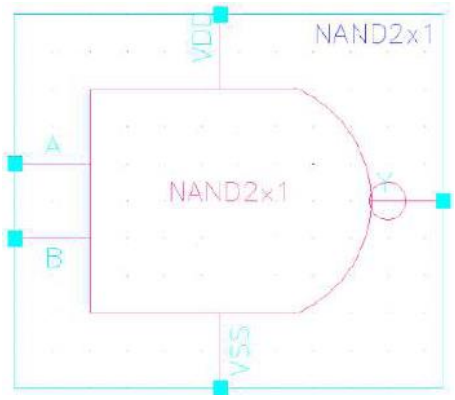
Symbol

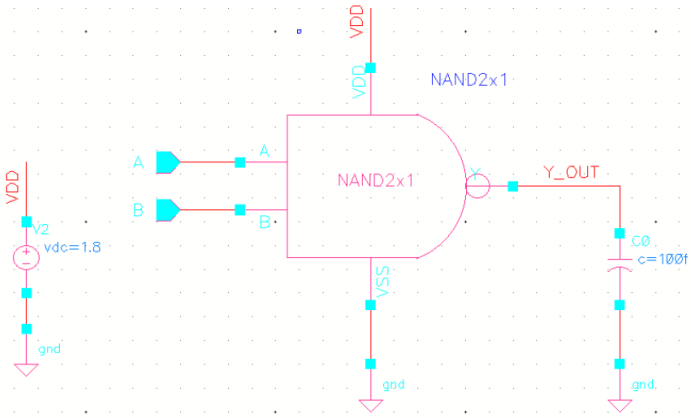


Length and Width of NMOS and PMOS Transistors for the condition

		NAND2_1X	**NAND2_2X**	**NAND2_4X**
Library Name	**Cell Name**	**Properties/comments**	**Properties/comments**	**Properties/comments**
gpdk180	nmos	Model Name= nmos1 (NM0); W= 1.6u; L=180n	Model Name= nmos1 (NM0); W= 3.2u; L=180n	Model Name= nmos1 (NM0); W= 6.4u; L=180n
gpdk180	nmos	Model Name= nmos1 (NM1); W= 1.6u; L=180n	Model Name= nmos1 (NM1); W= 3.2u; L=180n	Model Name= nmos1 (NM1); W= 6.4u; L=180n
gpdk180	pmos	Model Name = pmos1 (PM0); W= 1.6u; L=180n	Model Name = pmos1 (PM0); W= 3.2u; L=180n	Model Name = pmos1 (PM0); W= 6.4u; L=180n
gpdk180	pmos	Model Name = pmos1 (PM1); W= 1.6u; L=180n	Model Name = pmos1 (PM1); W= 3.2u; L=180n	Model Name = pmos1 (PM1); W= 6.4u; L=180n

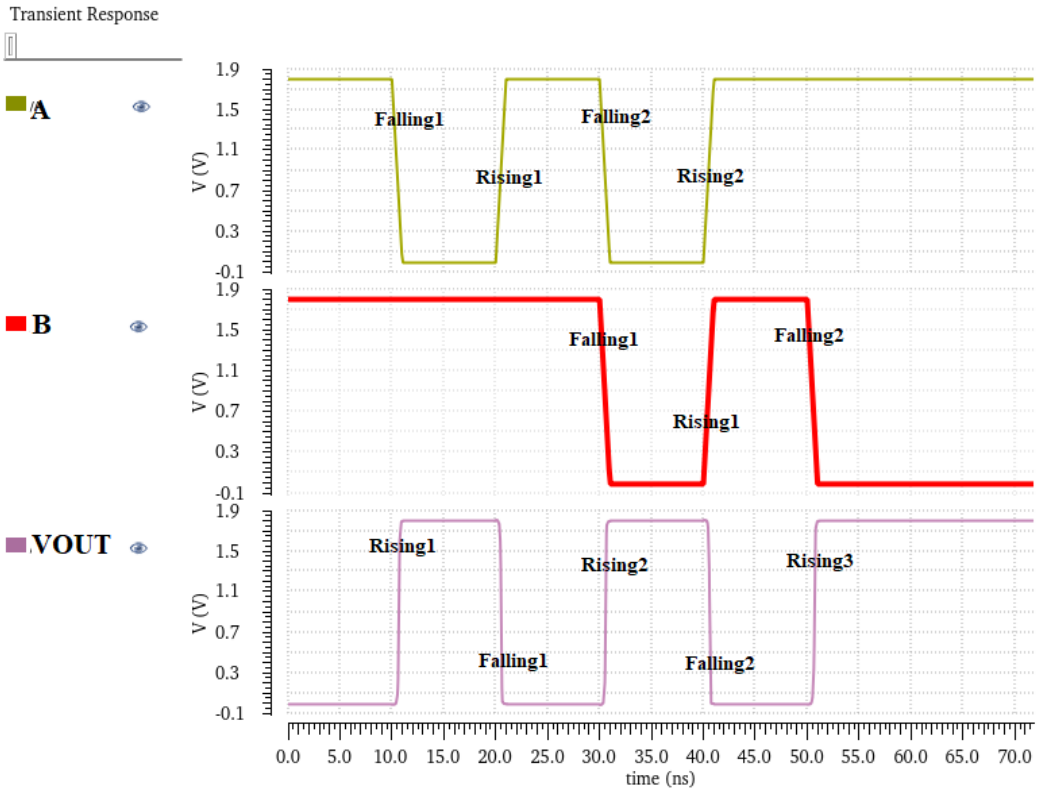
Symbol **Test Circuit**





Symbol Parameters	Library Name	Cell Name	Properties/comments
	USN	Inv	symbol
A	analoglib	Vpulse	V1 = 0V, V2 =1.8V, Delay = 0s, Rise time=1ns; fall time=1ns; Pulse Width = 10ns, Period = 20n s
B	analoglib	Vdc, gnd	V1 = 0V, V2 =1.8V, Delay = 0s, Rise time=1ns; fall time=1ns; Pulse Width = 20ns, Period = 40n s
Vo	analoglib	Cap	10fF
VSS	analoglib	Gnd	
VDD	analoglib	Vdd	DC Voltage=1.8V

Simulation Waveform (Transient):



Waveform Generation:

- ✓ *To calculate delay for all 4 conditions i.e. 00, 01, 10, 11.*
- ✓ *Go to ADEL from schematic window,*
- ✓ *Choose Transient analysis.*
- ✓ *Select input and output as A, B, Vout.*
- ✓ *Goto Setup-Stimuli*
- ✓ *For*
  - o *Vdd: enabled √(tick) Function- dc (1.8)*
  - o *Vss: enabled √ Function- dc (0)*
  - o *A: enabled √ Function- bit (one value-1.8; zero value-0; Rise Time-1ns; Fall Time-1ns; pattern parameter data- 101011)*
  - o *B: enabled √ Function- bit (one value-1.8; zero value-0; Rise Time-1ns; Fall Time-1ns; pattern parameter data- 111010)*

Delay Calculation:

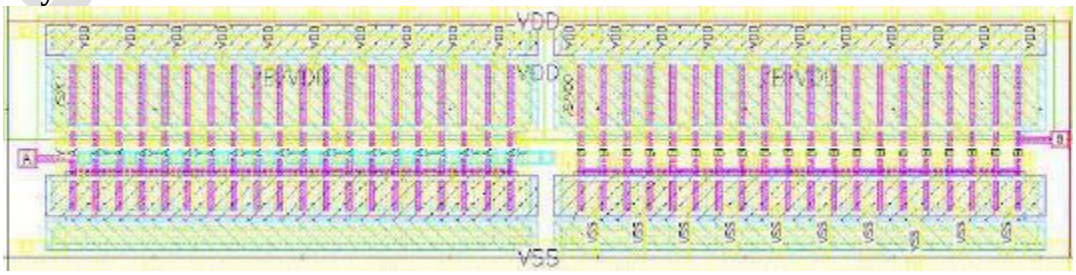
- ✓ *Goto Tools-Calculator*
- ✓ *Set all parameters as shown in table below*

Input	*Signal1*	*Signal2*	*Threshold1 & Threshold2*	*Edge Number1*	*Edge Number 2*	*Edge Type1*	*Edge Type2*
01	***A***	***Vout***	***0.9***	***1***	***1***	***Falling***	***Rising***
11	***A***	***Vout***	***0.9***	***1***	***1***	***Rising***	***Falling***
00	***A***	***Vout***	***0.9***	***2***	***2***	***Falling***	***Rising***
10	***B***	***Vout***	***0.9***	***2***	***3***	***Falling***	***Rising***

Values of 2-input CMOS NAND gate NAND_1X, NAND_2X, NAND_4X

NAND Typ	MOSFET	Length	Width	Tp00	Tp01	Tp10	Tp11	Tp_{Max}
NAND2X1	PMOS/ NMOS	180n	1.6u	110.1 ps	203.6 ps	238.1 ps	52.47 ps	238.1ps
NAND2X2	PMOS/ NMOS	180n	3.2u	88.79 ps	175 ps	213.5 ps	33.8 ps	213.5 ps
NAND2X4	PMOS/ NMOS	180n	6.4u	75.5 ps	158.1 ps	199.4 ps	22.78 ps	199.4 ps

Layout



EXPERIMENT – 3

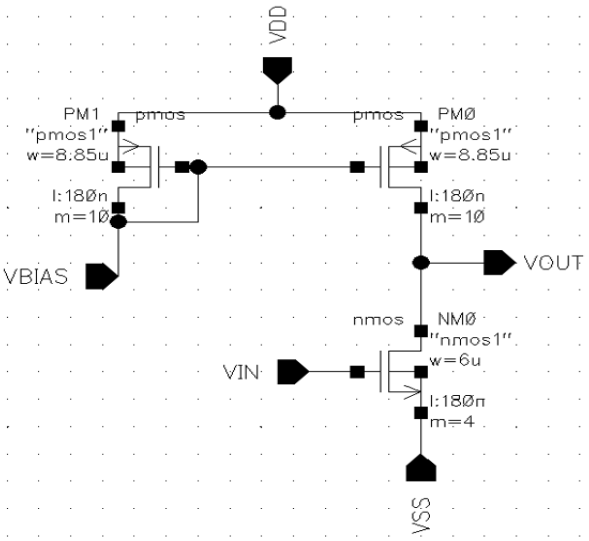
COMMON SOURCE AMPLIFIER WITH PMOS CURRENT MIRROR LOAD

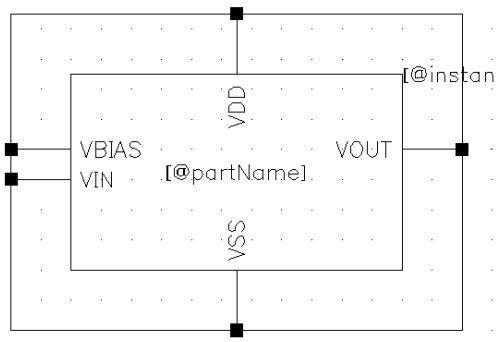
Objective:

(a) Capture the Schematic of a Common Source Amplifier with PMOS Current Mirror Load and find its Transient Response and AC Response. Measure the UGB and amplification Factor by varying transistor geometries, study the impact of variation in width to UGB.

(b) Draw the layout of Common Source Amplifier, use optimum layout methods. Verify DRC and LVS, extract the parasitics and perform the post layout simulation, compare the results with pre layout simulations. Record the observations

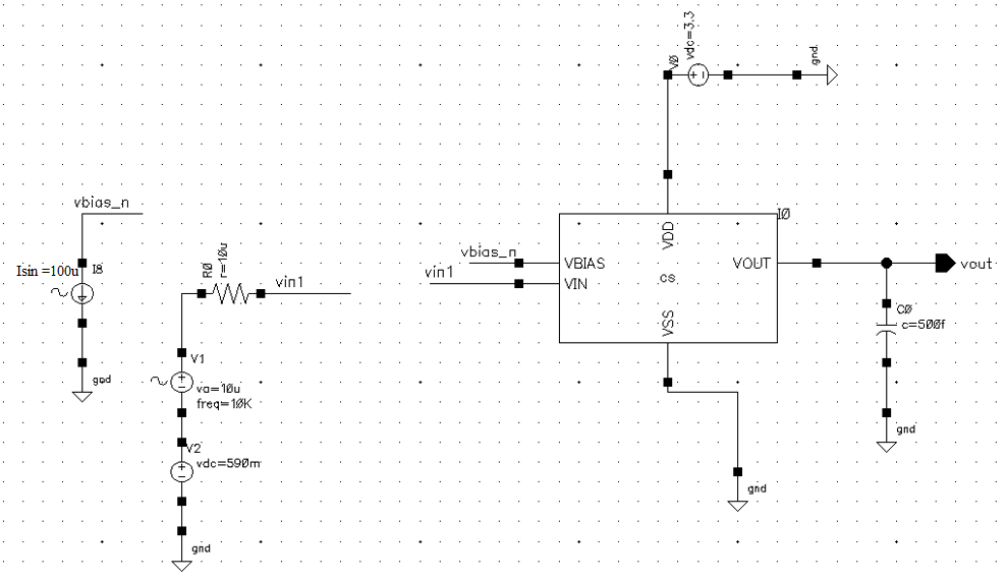
Schematic **Symbol**





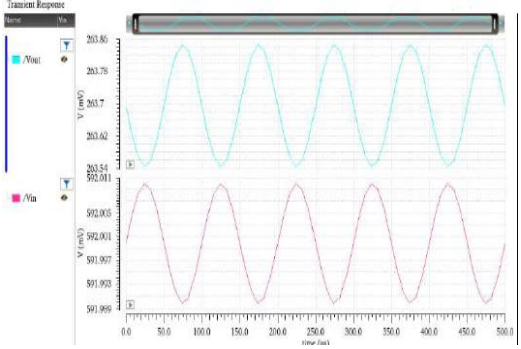
Library Name	Cell Name	Properties / Comments
gpdk180	nmos	Model Name = nmos1 (NM0); Wn= 6u; L = 180u
gpdk180	pmos	Model Name = nmos1 (PM0); Wp= 8.85u; L = 180u

Test Circuit:

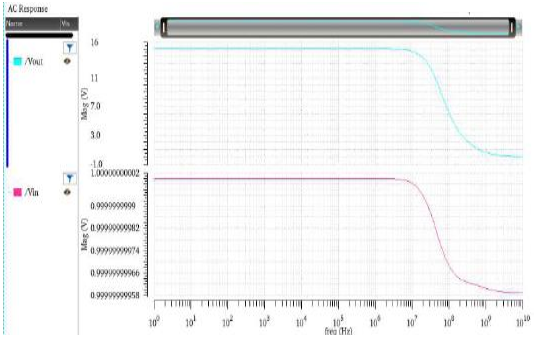


Symbol Parameters	Library Name	Cell Name	Properties/comments
	USN	Inv	symbol
Vdd	analoglib	Vdc	DC Voltage=3.3V
Vin	analoglib	vsin	AC Magnitude = 1 V, Amplitude = 10uV, Frequency = 10K Hz (Vin)
		res	Resistance=10u ohms
		vdc	DC voltage = 590uV VBIAS_N V (Vin)
Vb	analoglib	Isin	DC current = 100u A (Vbias_P)
Vo	analoglib	Cap	100fF
Vss	analoglib	Gnd	

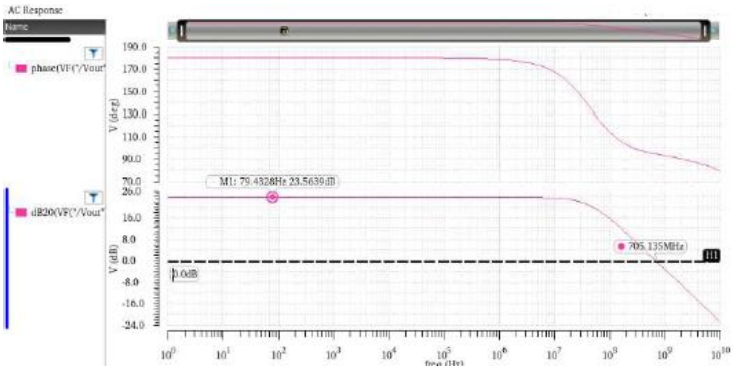
Simulation Waveform (Transient, AC, DC):



Transient Analysis



AC Analysis

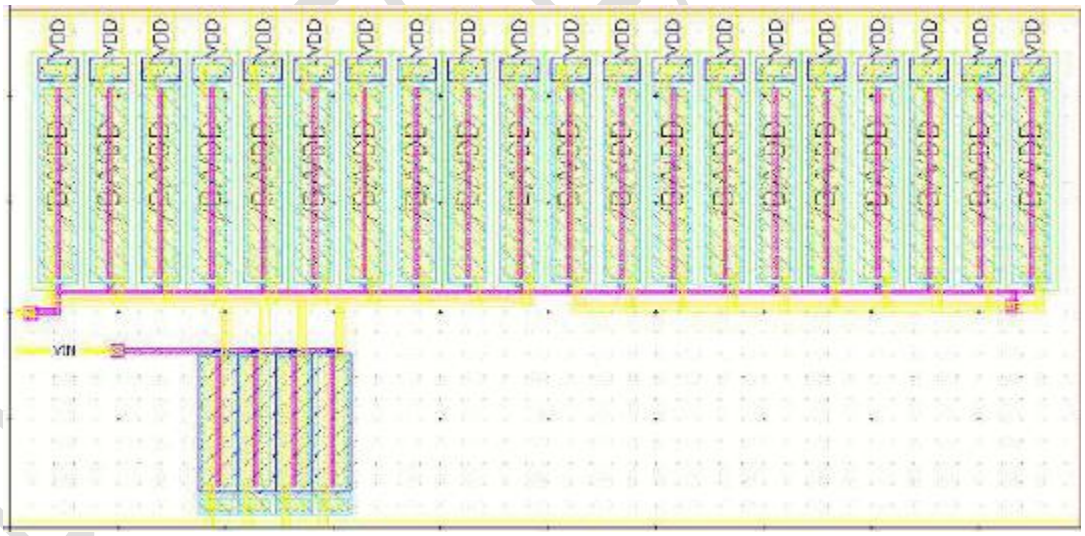


Gain-Phase Plot

UGB Calculation:

- ✓ Select AC analysis
- ✓ Goto ADEL window,
  - Results – Direct plot –AC gain and phase
  - Select output wire and input wire (in the same order)
- ✓ Press H (for horizontal line) and double click on horizontal line, choose Y-position to "0"
- ✓ Make note of Unity gain Bandwidth value

Layout:



EXPERIMENT – 4
2 – STAGE OPERATIONAL AMPLIFIER

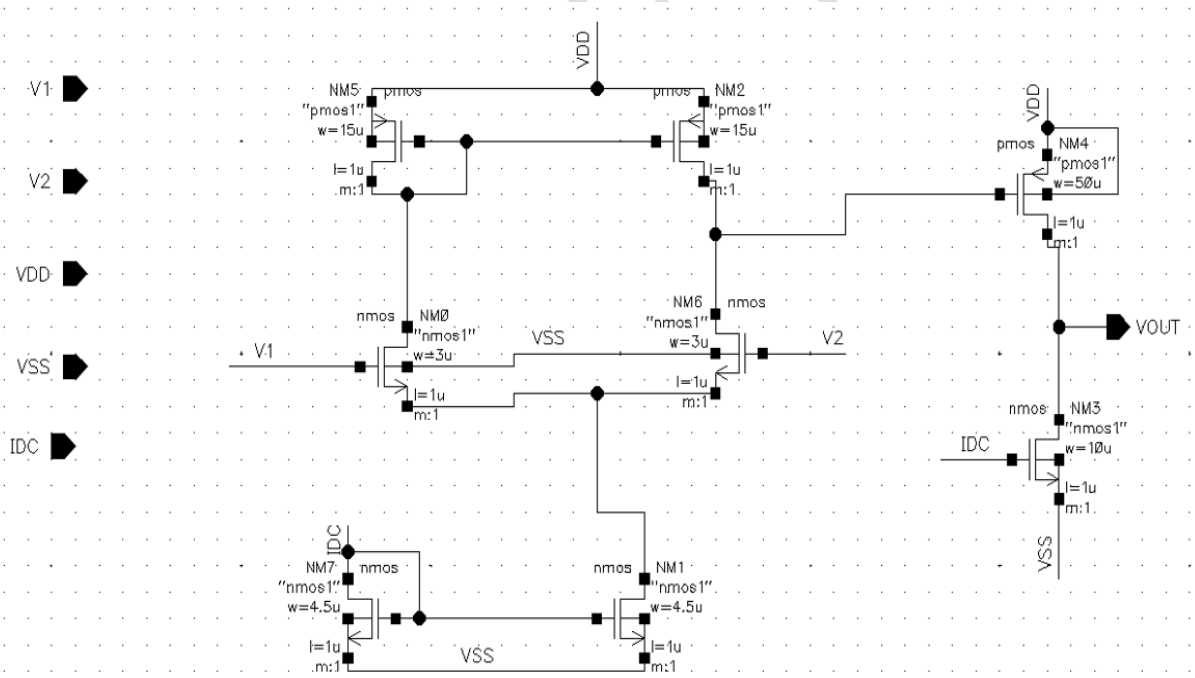
Objective:

(a) Capture the Schematic of a 2 – Stage Operational Amplifier and measure the following:

1. UGB
2. dB Bandwidth
3. Gain Margin and Phase Margin with and without coupling capacitance
4. Use the Op-Amp in the Inverting and Non-Inverting configuration and verify its functionality
5. Study the UGB, 3 dB Bandwidth, Gain and Power Requirement in Op-Amp by varying the stage wise transistor geometries and record the observations

(b) Draw the layout of 2 – stage Operational Amplifier with the maximum transistor width set to 300 (in 180 / 90/ 45n m Technology), choose appropriate transistor geometries as per the results obtained in 4(a). Use optimum layout methods. Verify DRC and LVS, extract the parasitics and perform the post layout simulation, compare the results with pre layout simulations. Record the observations.

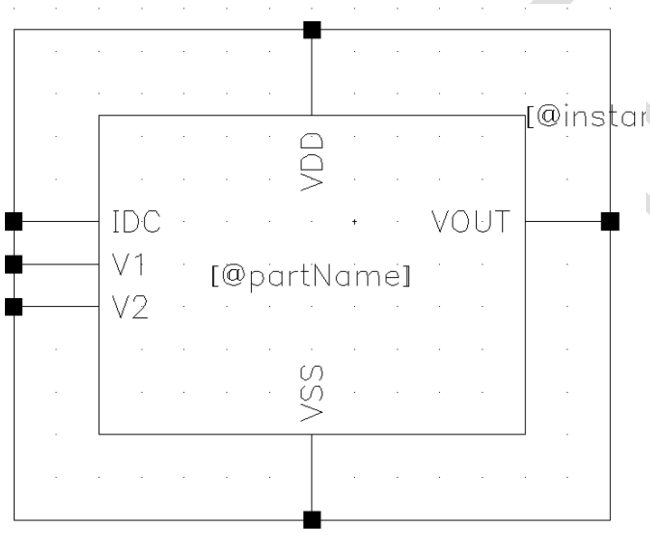
Schematic



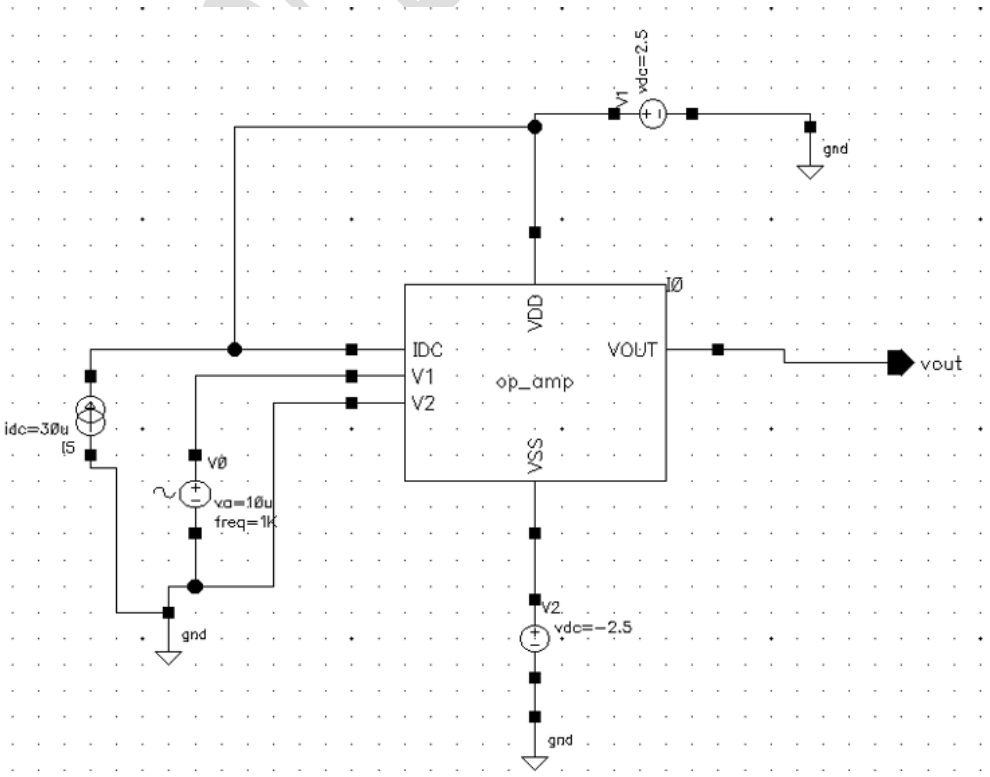
Library Name	Cell Name	Properties/comments
gpdk180	NM2,NM52	Width, W = 15u Length, L = 1u
gpdk180	NM0,NM6	Width, W = 3u Length, L = 1u

gpdk180	NM7,NM1	Width, W = 4.5u Length, L = 1u
gpdk180	NM4	Width, W = 50u Length, L = 1u
gpdk180	NM3	Width, W = 10u Length, L = 1u

Symbol

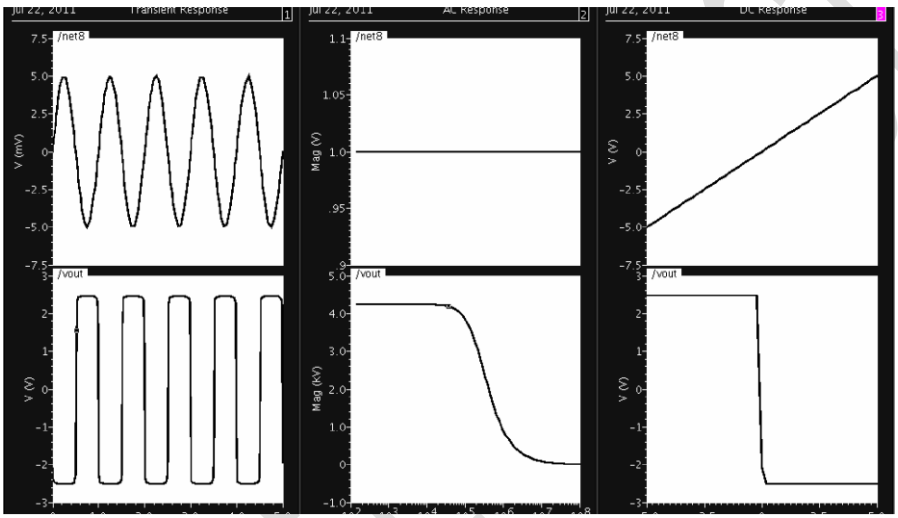


Test Circuit:



Symbol Parameters	Library Name	Cell Name	Properties / Comments
	USN	Op_amp	Symbol
Vin	analogLib	vsin	Define specification as AC Magnitude = 1; Amplitude = 5m;Frequency = 1K
Vb	analogLib	vdc	-2.5
Vss	analogLib	vdc	-2.5
vnonb	analogLib	gnd	
idc	analogLib	Idc	DC current = 30u

Simulation Waveform (Transient, AC, DC):



dB Bandwidth Calculation:

- ✓ Goto AC response waveform
- ✓ Make note of Vmax
- ✓ Press H (for horizontal line) and double click on horizontal line, choose Y-position to "**0.707*Vmax**"
- ✓ Make note of dB Bandwidth value

Gain Margin and phase margin andUGB Calculation:

- ✓ Select AC analysis
- ✓ Goto ADEL window,
  - Results – Direct plot –AC gain and phase
  - Select output wire and input wire (in the same order)
- ✓ Press H (for horizontal line) and double click on horizontal line, choose Y-position to "0"
- ✓ Make note of Unity gain Bandwidth value

Layout: