

# Design of LCL- DAB DC DC Converter with feedforward control

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**Abstract**—This paper introduces a resonant dual active bridge (DAB) converter that incorporates a tuned inductor–capacitor–inductor (LCL) network. Compared to conventional DAB converters, the LCL-type resonant DAB (LCL-DAB) DC–DC converter offers notable benefits, such as improved suppression of power backflow and enhanced voltage gain. As a result, LCL-DAB converters show great potential for use in applications like DC microgrids, electric vehicles, and uninterruptible power supplies. The performance of DAB converter is studied using mathematical model under various operating condition.

## I. INTRODUCTION

Bidirectional DC–DC converters are extensively applied in systems such as distributed generation, electric vehicles, and uninterruptible power supplies. With the rapid advancement of DC microgrid technologies, these converters are expected to play an increasingly pivotal role in power conversion systems. To ensure voltage compatibility and electrical isolation, transformers—either operating at low or high frequency—are commonly integrated into bidirectional isolated DC–DC converter designs. Compared to their low-frequency counterparts, which tend to be bulky and inefficient, high-frequency isolated DC–DC converters are gaining popularity due to their compact size, higher power density, and cost-effectiveness.

Among the various high-frequency isolated DC–DC converters, the dual-active-bridge (DAB) type stands out because of its beneficial characteristics, including high power density, electrical isolation, and rapid dynamic performance as explained in [1]. Its symmetrical configuration allows for bidirectional power flow, while the high-frequency transformer contributes to the converter's compact and efficient design. In a DAB converter, the inductor is effectively situated between two PWM-controlled voltage sources, each governed by distinct modulation techniques like single-phase-shift (SPS), extended-phase-shift (EPS), dual-phase-shift (DPS), or triple-phase-shift (TPS) control.

However, due to phase differences between voltage and current, there are instances when they flow in opposite directions. This results in a portion of power reversing its path and returning to the input source, known as backflow power [4]. Such backflow can negatively impact the converter's performance by increasing conduction losses, copper losses, and current stress, ultimately reducing overall efficiency.

This study introduces an innovative dual active bridge (DAB) converter design that incorporates a resonant network

aimed at reducing the converter's reactive power demand across varying load conditions. The configuration makes use of a tuned inductor–capacitor–inductor (LCL) network, which integrates the isolation transformer's leakage inductance to effectively lower bridge current levels. As a result, both switching and conduction (copper) losses are minimized. The converter operates under a straightforward control strategy, where identical PWM signals are applied to both bridges, and a constant phase shift of either  $+90^\circ$  or  $-90^\circ$  is maintained to manage both the direction and amount of power transferred. Analytical evaluations and simulation results are described in [2] which validate the converter's capability to achieve efficient bidirectional power transfer across a broad spectrum of power levels and DC input voltages

## II. SYSTEM OVERVIEW

Figure 1 illustrates the basic structure of a conventional dual active bridge (DAB) DC–DC converter, which primarily includes two identical H-bridge circuits, a high-frequency transformer, and an inductor. Figure 2 presents the representative waveforms under a single-phase-shift (SPS) modulation method. The phase shift introduces a timing mismatch between the primary voltage  $u_p$  and the secondary voltage  $u_s$  creating a voltage differential across the inductor. As a result, the inductor current  $i_L$  varies over time. Notably, during the interval  $0 \leq t \leq t_0$ ,  $u_p$  is positive while  $i_L$  is negative, indicating that energy is being returned to the input source—commonly referred to as power backflow. It has been explained in [4]

Building upon the conventional DAB DC–DC converter architecture, the LCL-DAB variant replaces the single filter inductor with an LCL-type resonant network. As illustrated in Figure 3, this resonant network is composed of two inductors,  $L_1$  and  $L_2$ , along with a capacitor  $C_1$ . The transformer's leakage inductance is reflected to the primary side and incorporated into inductor  $L_2$ . For analytical purposes and to maintain symmetry,  $L_1$  and  $L_2$  are assumed to have identical inductance values, and the transformer's turns ratio is considered as  $N:1$ . The corresponding equivalent circuit model is displayed in Figure 4. Both primary and secondary bridge voltages,  $u_p$  and  $u_s$ , are square waveforms that can be produced using various modulation strategies. Unlike traditional DAB converters, the presence of additional components in the LCL tank complicates the time-domain approach. As a result, this work employs a phasor-based method, which analyzes each sinusoidal component at its respective frequency and then

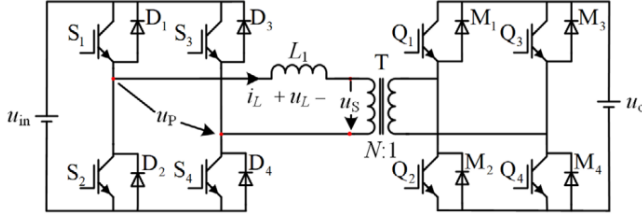


FIGURE 1 Topology diagram of a DAB DC-DC converter

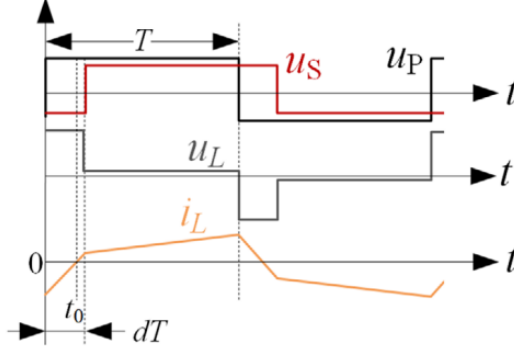


FIGURE 2 Main waveforms with SPS modulation scheme

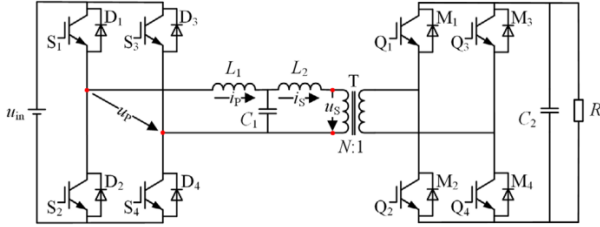


FIGURE 3 Topology diagram of an LCL-DAB converter

reconstructs the total response by summing them, leveraging the linear characteristics of the circuit.

As illustrated in Figure 4, the equivalent circuit of the LCL-DAB DC-DC converter can be modeled as a two-port network, with its input and output behavior described by Equation (1). In this context, the resonant angular frequency is defined as  $\omega = 1/\sqrt{Lc}$  and the characteristic impedance is given by  $Z_0 = \omega L = \sqrt{L/c}$  where  $L$  represents the inductance value common

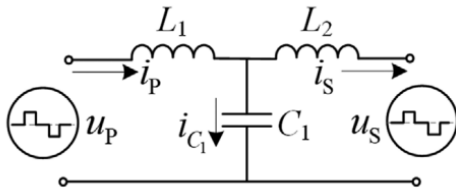


FIGURE 4 Equivalent model of an LCL-DAB converter

$$\begin{cases} \dot{U}_P = j \left( \omega L_1 - \frac{1}{\omega C_1} \right) \dot{I}_P + j \frac{1}{\omega C_1} \dot{I}_S \\ \dot{U}_S = j \left( \frac{1}{\omega C_1} - \omega L_2 \right) \dot{I}_S - j \frac{1}{\omega C_1} \dot{I}_P \end{cases} \quad (1)$$

$$\begin{cases} \dot{U}_P = j Z_0 \dot{I}_S \\ \dot{U}_S = -j Z_0 \dot{I}_P \end{cases} \quad (2)$$

to both filter inductors,  $L_1$  and  $L_2$ . When the converter's switching frequency matches the resonant frequency Equation (1) simplifies to the form presented in Equation (2).

From Equation (2), it is evident that the voltage  $U_P$  leads the output current  $I_S$  by  $90^\circ$ , and similarly, the input current  $I_P$  leads the output voltage  $U_S$  by  $90^\circ$ . When  $U_P$  and  $U_S$  are phase-shifted by  $90^\circ$ , the voltage and current waveforms on both sides align in phase, indicating that there is no reactive power flow. Based on the correlation between instantaneous and backflow power, minimizing reactive power also helps in reducing backflow power. Due to space constraints, a comprehensive analysis is not provided here. However, to achieve an operating condition without power backflow in an LCL-DAB converter, the following three requirements must be met:

1. The switching frequency should match the resonant frequency of the LCL network.
2. The phase difference between the primary and secondary side fundamental voltages and should be  $90^\circ$ .
3. Harmonic distortion within the converter must be kept to a minimum. While the first two criteria are relatively straightforward to satisfy, the link between harmonic content and backflow power does not identify a specific modulation range where backflow power is fully suppressed. As a result, the defined operational range that ensures zero backflow power is introduced below, assuming the first two criteria are already fulfilled.

### III. MATHEMATICAL ANALYSIS

This study utilizes the triple-phase-shift (TPS) modulation strategy for the LCL-DAB DC-DC converter, as it generalizes all other phase-shift-based control methods. In this approach,  $d_1$   $d_2$  represent the internal phase shift ratios, while  $d$  defines the phase shift between the primary and secondary bridges. Based on the second requirement outlined in Section 2, the switching frequency is set equal to the resonant frequency  $f_s$ , and the inter-bridge phase shift  $d$  is fixed at 0.25 throughout the subsequent analysis.

#### A. Power Throughput

to study the harmonics involved, fourier expansion is done for primary and secondary voltages. since,  $U_P$  is an odd function, their fourier decomposition are:

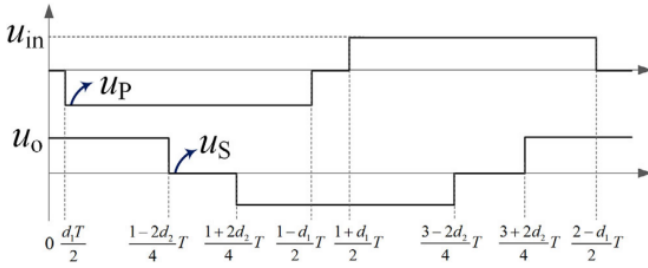


FIGURE 5 Waveforms of  $u_p$  and  $u_s$  with TPS modulation scheme

$$\begin{cases} u_p(t) = \sum_{n=1,3,5,\dots} \frac{-4U_{in}}{n\pi} \cos(n\pi d_1) \sin(n\omega_s t), \\ u_s(t) = \sum_{n=1,3,5,\dots} (-1)^{\frac{n-1}{2}} \frac{4NU_0}{n\pi} \cos(n\pi d_2) \cos(n\omega_s t), \end{cases}$$

the above equation can be represented in phasor form as above written equations.

$$\begin{cases} \hat{U}_{p,n} = j \frac{2\sqrt{2}U_{in} \cos(n\pi d_1)}{n\pi} \\ \hat{U}_{s,n} = (-1)^{\frac{n-1}{2}} \frac{2\sqrt{2}NU_0 \cos(n\pi d_2)}{n\pi} \end{cases}$$

$$\begin{cases} I_{p,n} = \frac{2\sqrt{2}}{n^2(2-n^2)\sqrt{\pi}} \times \left[ U_{in} \cos(n\pi d_1)(1-n^2) + j(-1)^{\frac{n-1}{2}} NU_0 \cos(n\pi d_2) \right] \\ I_{s,n} = \frac{2\sqrt{2}}{n^2(2-n^2)\sqrt{\pi}} \times \left[ U_{in} \cos(n\pi d_1) + j(-1)^{\frac{n-1}{2}} NU_0 \cos(n\pi d_2) \right] \end{cases}$$

assuming that there is no power loss in transmission, active power is expressed as

$$P_{total} = \frac{8NU_{in}U_0}{\pi^2 Z_0} \sum_{n=1,3,5} \frac{(-1)^{\frac{n-1}{2}} \cdot \cos(n\pi d_1) \cos(n\pi d_2)}{n^3 \cdot (2-n^2)},$$

the power equation is very complex and needs to be simplified. It is found out that the fundamental power equation contribute to more than 96 percent of more. hence it is feasible to approximate power equation as

$$P = \frac{8NU_{in}U_{out}\cos(\pi d_1)\cos(\pi d_2)}{\pi^2 Z_0}$$

$$P = \frac{8NU_{in}U_{out}\cos(\pi d_1)\cos(\pi d_2)}{\pi^2 Z_0}$$

### B. Operation under no backflow power

Since the converter operates symmetrically in each half cycle and the primary aim is to ensure zero power backflow in the LCL-DAB DC-DC converter, it is essential—besides meeting the two earlier conditions ( $d_1 = d_2$  and  $d=0.25$ )—to align the polarities of voltage and current on both sides of the LCL resonant network. Based on the preceding analysis, the current waveforms  $i_p$  and  $i_s$  can be approximated as sinusoidal. This allows the condition for no backflow to be simplified into four inequality expressions. Specifically, Equations (9) and (10) serve as sufficient criteria to prevent backflow on the primary side ('P'), while Equations (11) and (12) fulfill the same purpose for the secondary side ('S').

$$i_p \left( \frac{d_1}{2} T \right) \leq 0 \quad (9)$$

$$i_p \left( \frac{1-d_1}{2} T \right) \leq 0 \quad (10)$$

$$i_s \left( \frac{1+2d_2}{4} T \right) \leq 0 \quad (11)$$

$$i_s \left( \frac{3-2d_2}{4} T \right) \leq 0. \quad (12)$$

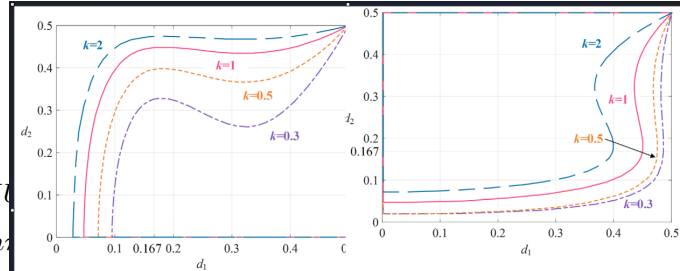


FIGURE 7 Design regions of  $d_1$  and  $d_2$  under no backflow power at 'P' side

FIGURE 8 Design regions of  $d_1$  and  $d_2$  under no backflow power at 'S' side

Based on Equation (6), it can be concluded that if both Equations (9) and (12) are met, power backflow will be eliminated on both the primary ('P') and secondary ('S') sides. This is because the solution set of the first inequality is inherently included within that of the second, and the third and fourth inequalities are effectively equivalent. In summary, ensuring that Equation (9) is satisfied is sufficient to prevent backflow on the primary side, while satisfying Equation (12) alone ensures the same on the secondary side. Hence, to ensure no backflow power,  $d_1$  and  $d_2$  should be estimated properly. the selection of  $d_1$  and  $d_2$  is dependent on turn ratio, input and output voltages, impedance. the control of  $d_1$  and  $d_2$  determine the fairness of operation.

As illustrated in Figure 7, for varying values of  $k$ , the area enclosed by the boundaries of  $d_1$   $d_2$  represents the valid design space where no power backflow occurs on the primary side. The figure shows that this design region becomes larger as  $k$  increases. Moreover, for any given  $k$ , the widest range for without backflow is achieved when  $k=0.167$ , which aligns with prior findings about the connection between harmonic distortion and modulation range. The expansion of the design region is attributed to the use of the TPS modulation technique. Figure 8 presents a contrasting trend for the secondary side, where the backflow-free region becomes smaller as  $k$  increases. Due to the symmetrical nature of the converter, the optimal design range for  $d_1$  is observed when  $d_2=0.167$ . Since the system uses

a resistive load, this study concentrates on mitigating backflow on the primary side. Thus, based on Figure 7, it is evident that selecting a suitable value of  $d_1$  can effectively maintain a no-backflow operating condition in most scenarios [3].

#### IV. MODELLING OF LCL DAB CONVERTER

To properly design the controller parameters, it is essential to develop an accurate model of the LCL-DAB DC-DC converter. This is achieved using the generalized average modeling technique, which simplifies the system by approximating variables up to the first order. This approach strikes a balance between simplicity and precision. It involves selecting the DC components and first-order harmonics of the inductor currents and capacitor voltages as the system's state variables. Using these, a complete continuous-time average model of the converter can be constructed.

Up and Us can be expressed in time domain as:-

$$u_P(t) = s_1(t) \cdot U_{in} \quad (15)$$

$$u_S(t) = s_2(t) \cdot N U_o \quad (16)$$

where  $s_1(t)$  and  $s_2(t)$  is depicted in fig5.

$s_1(t)$  and  $s_2(t)$  are periodic functions. it is expanded by fourier series expansion. thence, phasor method is used to do mathematical calculation. the conversion of these switching function is expressed below:

$$\langle s_1 \rangle = j \frac{2 \cos(\pi d_1)}{\pi}$$

$$\langle s_2 \rangle = \frac{2 \cos(\pi d_2)}{\pi}$$

When the inductor currents and the capacitor voltage are selected as state variables, the large-signal dynamic behavior of the LCL-DAB converter can be described using differential equations.

$$\begin{cases} L \frac{di_p(t)}{dt} = s_1(t) \cdot u_{in}(t) - u_{C1}(t) \\ L \frac{di_s(t)}{dt} = -s_2(t) \cdot N u_o(t) + u_{C1}(t) \\ C_2 \frac{du_{C2}(t)}{dt} = s_2(t) \cdot N i_s(t) - \frac{u_o(t)}{R} \\ C_1 \frac{du_{C1}(t)}{dt} = i_p(t) - i_s(t) \\ u_{C1}(t) = u_o(t) \end{cases}$$

converting the state in small signal analysis,

$$\langle i_P \rangle_{1R} = \Delta \langle i_P \rangle_{1R} + I_{P1R} \quad (28)$$

$$\langle i_P \rangle_{1I} = \Delta \langle i_P \rangle_{1I} + I_{P1I} \quad (29)$$

$$\langle i_S \rangle_{1R} = \Delta \langle i_S \rangle_{1R} + I_{S1R} \quad (30)$$

$$\langle i_S \rangle_{1I} = \Delta \langle i_S \rangle_{1I} + I_{S1I} \quad (31)$$

$$\langle u_{C1} \rangle_{1R} = \Delta \langle u_{C1} \rangle_{1R} + U_{C11R} \quad (32)$$

$$\langle u_{C1} \rangle_{1I} = \Delta \langle u_{C1} \rangle_{1I} + U_{C11I} \quad (33)$$

$$\langle u_o \rangle_0 = \Delta \langle u_o \rangle_0 + U_{o0} \quad (34)$$

$$\frac{d}{dt} \begin{bmatrix} \Delta \langle i_P \rangle_{1R} \\ \Delta \langle i_P \rangle_{1I} \\ \Delta \langle i_S \rangle_{1R} \\ \Delta \langle i_S \rangle_{1I} \\ \Delta \langle u_{C1} \rangle_{1R} \\ \Delta \langle u_{C1} \rangle_{1I} \\ \Delta \langle u_o \rangle_0 \end{bmatrix} = \begin{bmatrix} 0 & \omega & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ -\omega & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & 0 & \omega & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & -\omega & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & -\frac{1}{C_1} & 0 \\ 0 & \frac{1}{C_1} & 0 & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \cdot \begin{bmatrix} \Delta \langle i_P \rangle_{1R} \\ \Delta \langle i_P \rangle_{1I} \\ \Delta \langle i_S \rangle_{1R} \\ \Delta \langle i_S \rangle_{1I} \\ \Delta \langle u_{C1} \rangle_{1R} \\ \Delta \langle u_{C1} \rangle_{1I} \\ \Delta \langle u_o \rangle_0 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ \frac{2 \cos(\pi D_1)}{\pi} & 0 & 0 \\ -\frac{2 \sin(\pi D_1) U_{in}}{L} & 0 & 0 \\ 0 & 0 & \frac{2N \sin(\pi D_2) U_o}{L} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{4N I_{S1R} \sin(\pi D_2)}{C_2} \end{bmatrix} \cdot \begin{bmatrix} \Delta \langle u_{in} \rangle_0 \\ \Delta d_1 \\ \Delta d_2 \end{bmatrix}$$

By eliminating the large-signal components, the small-signal model of the LCL-DAB converter can be obtained, as shown, indicating that the system exhibits seventh-order dynamics. To streamline computations and make the model more practical for real-world implementation, the analysis focuses only on the relevant variables: the output voltage variation  $\langle u_o \rangle$  and the internal phase shift variation  $d_2$ .

$$G_{vd2}(s) = \frac{-4N R I_{S1R} \sin(\pi D_2)}{RC_2 s + 1} = \frac{-8\sqrt{2} N R U_{in} \cos(\pi D_1) \sin(\pi D_2)}{Z_0 \beta (RC_2 s + 1)}.$$

#### V. CONTROL SYSTEM

To ensure that the LCL-DAB DC-DC converter operates reliably without experiencing power backflow, the first step is to carefully choose an optimal value for the phase shift ratio  $d_1$ . This selection plays a crucial role in maintaining the desired power flow conditions under steady-state operation. Following this, the steady-state value of the inner phase shift ratio  $d_2$  must be determined with sufficient margin to accommodate expected variations in operating conditions, such as load or input voltage changes. To further enhance the system's dynamic performance, a feedforward control mechanism is integrated into the design. This method helps the converter respond more quickly and effectively to disturbances or setpoint changes. Finally, a proportional-integral (PI) controller is designed by utilizing the previously developed system model. The model provides the necessary insight into the system dynamics, allowing the PI parameters to be selected for both stability and fast transient response.

##### A. The estimation of $d_1$

As outlined in Section 3, ensuring that the LCL-DAB DC-DC converter operates without power backflow requires the operating conditions to remain within the defined design boundaries shown in Figure 7. It is observed that when  $d_1$  approaches a value near 0.167, the allowable range for  $d_2$  expands, offering a broader backflow-free operating region. However, in real-world implementations, additional control goals—such as regulating the output voltage and managing power transmission—must also be considered. For instance, when a specific steady-state value of  $d_1$  denoted as  $D_1$  is selected, it directly influences the maximum amount of power the converter can transfer. Therefore, a balance must be struck between minimizing backflow power and meeting other performance criteria.

$$U_{o \max} = \frac{4N U_{in} R \cos(\pi D_1)}{\pi^3 * f l}$$

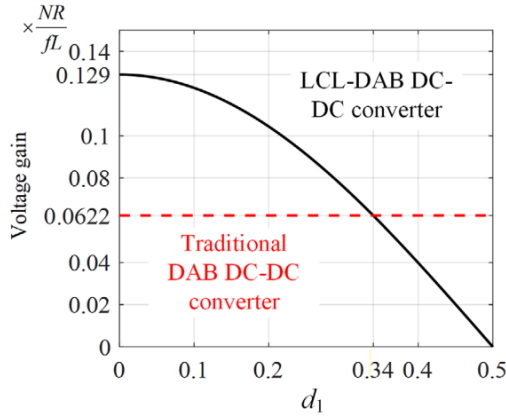


FIGURE 9 Voltage gain for two types of DAB DC-DC converters

### B. The determination of steady-state value $D_2$

In this section,  $d_2$  refers to the instantaneous phase shift ratio, while  $D_2$  represents its steady-state value. Their interaction is illustrated in Figure 10. As shown earlier in Figure 7, selecting a suitable value for  $d_1$  can maximize the feasible operating range of  $d_2$  that ensures the LCL-DAB DC-DC converter operates without any reverse power flow. However, this configuration only guarantees no backflow under most conditions, not all. This is because  $d_2$ , being the primary control input in the proposed control strategy, is continuously regulated in real-time. Even slight deviations around its steady-state value  $D_2$  can occur due to dynamic load or supply changes.

If during this adjustment process, the instantaneous value  $d_2$  crosses the boundary of the no-backflow operating region, power backflow becomes inevitable. Therefore, it is critical to choose the converter's steady-state operating point with sufficient safety margin. This precaution ensures that the dynamic variations of  $d_2$  remain well within the acceptable design range and do not breach the limits that lead to unwanted backflow conditions. Proper selection of

$D_2$  is thus essential for maintaining stable and efficient converter operation under dynamic scenarios

### C. Feedforward control

The conventional output voltage control strategy using constant feedforward compensation is illustrated in the block diagram. In this approach, a fixed value of

$D_2$  is applied as a feedforward signal to enhance the dynamic performance of the converter. Additionally, a delay component

$$e^{(-t_d s)}$$

is incorporated after the PI controller to account for computational delays inherent in digital microcontroller-based implementations.

While this method is straightforward and easy to implement, its ability to respond effectively to sudden disturbances is

limited. This is because the control system always relies on a constant steady-state reference value for the control variable, around which real-time adjustments are made. During abrupt changes in input voltage or load conditions, the entire responsibility of regulating the output falls on the PI controller. This often results in sluggish transient performance.

To address these limitations, an improved control scheme is proposed, as depicted in Figure 11. This enhanced approach employs a dynamic feedforward compensation technique, allowing the feedforward signal to adapt in real time based on system conditions. By actively adjusting the feedforward term, the converter achieves faster and more robust responses to disturbances, improving overall performance under dynamic operating conditions.

For any LCL-DAB converter operating with the TPS modulation strategy, Equation (40) is inherently satisfied, which allows for a redefinition of the feedforward compensation formula. However, this equation includes the resonant impedance  $Z_o$ , which makes the expression dependent on the converter's primary circuit parameters. In real-world implementations, obtaining precise values of inductance can be challenging, especially since inductance may vary depending on the current flow.

To address this issue, two possible methods can be applied depending on the specific application needs. The first is a simplified method that directly inverts Equation (40) to compute the feedforward term—an approximate approach. The second is a more precise method that eliminates the need for accurate inductance values by introducing a set of known steady-state operating points.

By referencing steady-state conditions, the impedance term  $Z_o$  in the equation can be effectively eliminated, leading to a revised expression as shown. This simplification is based on the assumption that  $d_1 = D_1$ , where  $D_1$  represents the selected value from Part A.

the feedforward compensation term is derived as presented. The coefficient for the feedforward term is given by:

$$k_{ff} = \cos(\pi D_2) \cdot \frac{U_{in}}{I_o}, \quad (1)$$

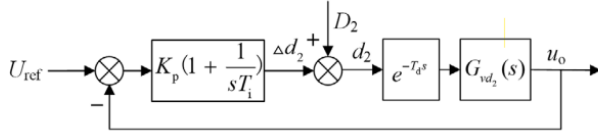
$$\begin{aligned} i_o &= \frac{8N u_{in} \cos(\pi d_1) \cos(\pi d_2)}{\pi^2 Z_o} \\ I_o &= \frac{8N U_{in} \cos(\pi D_1) \cos(\pi D_2)}{\pi^2 Z_o} \\ D'_2 &= \frac{1}{\pi} \cdot \cos^{-1} \left[ \frac{k_{ff} i_o}{u_{in}} \right] \end{aligned}$$

### D. The parameters of PI regulator

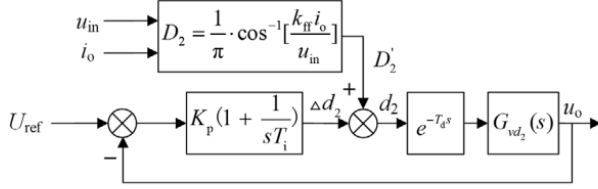
A PI controller is selected for the closed-loop regulation of the output voltage in this system. The tuning parameters for the PI regulator can be determined based on the method discussed previously. Referring to Figure 11, the open-loop transfer function of the overall control system can be derived as follows:

$$T(s) = K_p \left( 1 + \frac{1}{sT_i} \right) e^{-T_d s} \cdot \frac{m}{RC_2 s + 1}$$

Therefore, the phase of open-loop transfer function at  $\omega$  is given by:



**FIGURE 10** Output voltage control block diagram with the traditional constant feedforward compensation



**FIGURE 11** Output voltage control block diagram with the proposed dynamic feedforward compensation

$$\angle T(j\omega_c) = \tan^{-1}(\omega_c T_i) - \frac{\pi}{2} - \omega_c T_d - \tan^{-1}(\omega_c R C_2) = -\pi + \varphi_m$$

Define integral time as:

$$T_i = \frac{0.8}{\omega_c}$$

then phase margin is

$$\varphi_m = \tan^{-1}(\omega_c T_i) + \frac{\pi}{2} - \omega_c T_d - \tan^{-1}(\omega_c R C_2)$$

$$\varphi_m = \tan^{-1}(\omega_c T_i) + \frac{\pi}{2} - \omega_c T_d - \tan^{-1}(\omega_c R C_2)$$

The magnitude condition at crossover frequency is:

$$\|T(j\omega_c)\| = |K_p| \cdot \sqrt{1 + \frac{1}{\omega_c^2 T_i^2}} \cdot \frac{|m|}{\sqrt{R^2 C_2^2 \omega_c^2 + 1}} = 1 \quad (2)$$

Solving for the proportional gain:

$$|K_p| = \sqrt{\frac{R^2 C_2^2 \omega_c^2 + 1}{m^2 \left(1 + \frac{1}{\omega_c^2 T_i^2}\right)}}$$

## VI. PROPOSED METHODS TO IMPLEMENT CONCLUSION

A MATLAB simulation has been developed to analyze the operational characteristics and performance of the system under various conditions. This simulation serves as a foundational step before the physical implementation of the device using a microcontroller and associated hardware components. By examining the correlation between the inner phase shift ratio (d) in the primary bridge and the operational region where no backflow power occurs, an optimal value of d can be determined. This ensures that the LCL-DAB DC-DC converter functions efficiently without any reverse power flow.

The secondary bridge's inner phase shift ratio (d) is designated as the control variable to regulate the output voltage, ensuring it accurately tracks the reference voltage. To further enhance the system's responsiveness to sudden changes—such as fluctuations in input voltage or variations in load—a dynamic feed-forward compensation loop has been integrated. This loop improves transient response, allowing for faster stabilization and better performance under dynamic operating conditions.

The combination of these control strategies—precise phase shift regulation and adaptive feed-forward compensation—ensures stable and efficient converter operation across different scenarios. The MATLAB simulation provides critical insights into the system's behavior, facilitating the optimization of control parameters before hardware deployment.

## VII. ACKNOWLEDGMENT

The author gratefully acknowledges Dr. Sandip Ghosh for his unwavering support, insightful guidance. Sincere gratitude is also extended to the teaching assistants under his supervision for their valuable assistance in carrying out the simulation studies related to this project.

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