ProtectIT

DEGGENDORF INSTITUTE OF TECHNOLOGY DIIT

FPGA-Programming

Block 15 - Part 02

information about **student project work**

Prof. Dr. Martin Schramm

FPGA-Programming – Block 15 – information about examination

- student project work (summer term 2020)

there will not be a written examination!

  - task description:

as a team, conceptual design, implement and functional verify a VHDL based digital circuit

a team consists of max. 5 students

you are free in the choice of what functionality the circuit should comprise

groups will be created in iLearn

  - time frame:

project phase <u>starts on Monday 29. June</u> (directly after the time the last lecture block material is intended for) and <u>ends on Monday 27. July</u>

one minute to midnight

for mandatory aspects, see next slides

time to finish: 4 weeks

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mandatory key features

  - the circuit mandatory has to use following peripherals
    - **a subset or all of the switches {SW[0], …, SW[9]}**
    - **a subset or all of the push buttons {KEY[0], …, KEY[3]}**
    - **a subset or all of the red LEDs {LEDR[0], …, LEDR[9]}**
    - **a subset or all of the 7-segment displays {HEX0, …, HEX5}**
  - the circuit must consist of multiple entities
    - **at least five entities - the divide and conquer principle must be clearly visible**
  - as system clock, the circuit must use the 50 MHz clock CLOCK_50 provided on the DE1-SoC board
    - **for slower circuits use appropriate enable signals**

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mandatory key features

  - the circuit mandatory must comprise a state machine
    - **type (Moore or Mealy FSM) is up to you**
  - the circuit mandatory must comprise generic entities
    - **must be parameterizable**
  - at least one entity of the circuit should perform mathematical operations
    - **use numeric_std package and appropriate conversions**
  - a self-checking testbench must be created, which can be used to fully functional verify the correct behavior of the circuit
    - **comprised of various procedures to test functionality**

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mandatory key features

  - timing constraints have to be set and the maximum possible frequency of the final solution has to be given
    - **use TimeQuest Analyzer**
  - the circuit should contain a memory block
    - **LPM or described in VHDL is up to you**
  - deliver a short documentation together with the circuit
    - **ShareLatex, Word, etc. up to you**
  - optional:

for bonus points

    - **create and deliver an Algorithmic State Machine (ASM) chart for the circuit**
    - **create and deliver a block diagram chart for the circuit**