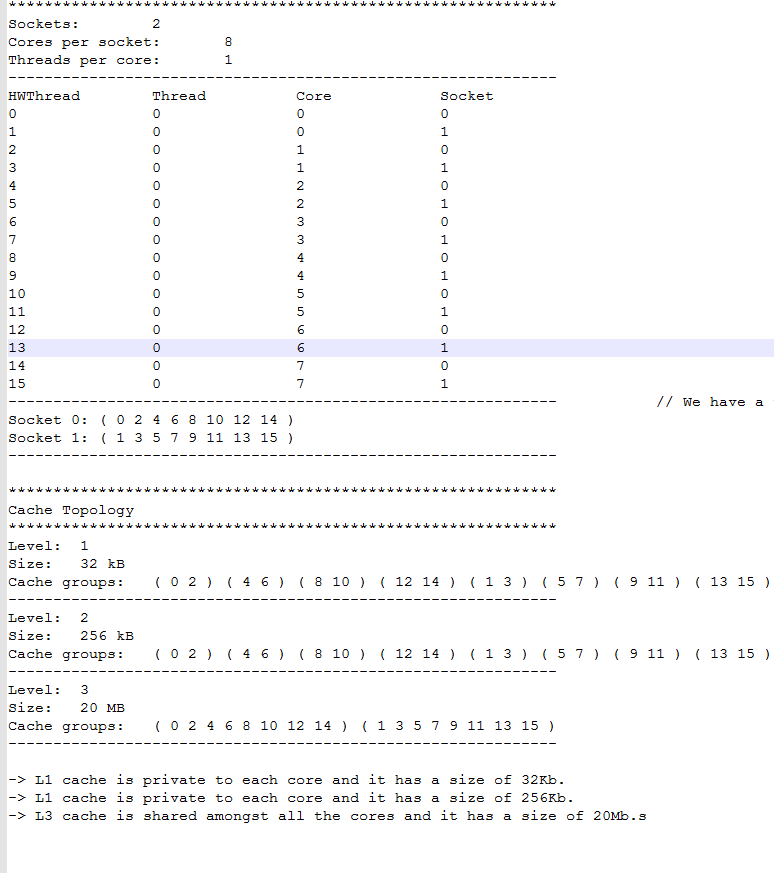
Q1) How is the memory subsystem structured on your machine? What is the highest level of data cache? How big is it? How is it shared across core?

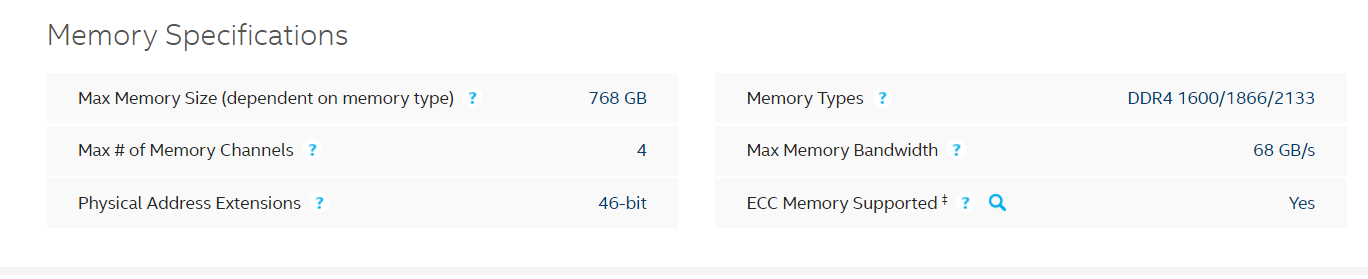


Q2)How much DRAM memory? Memory speed? Memory Technology? How much bandwidth can your processor draw from the bus?

Ans- We have the following processor.



So with the help of this <https://ark.intel.com/products/83361/Intel-Xeon-Processor-E5-2667-v3-20M-Cache-3_20-GHz> reference we get the following Information.



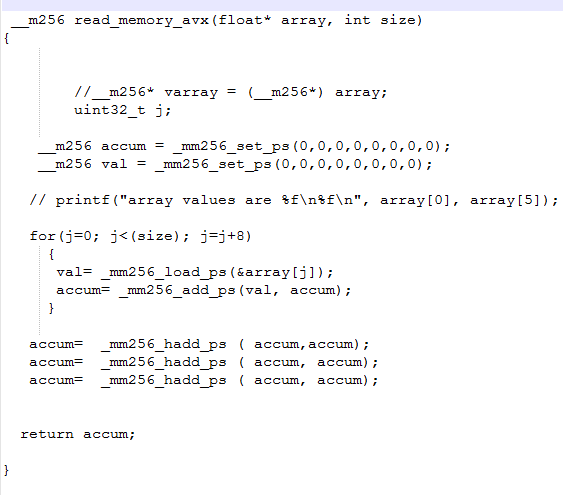
* The site claims the Max memory bandwidth of Xeon Processor to be 68GB/s.

Q2) **Bandwidth Measurement**

Code for measuring Bandwidth using Read operation

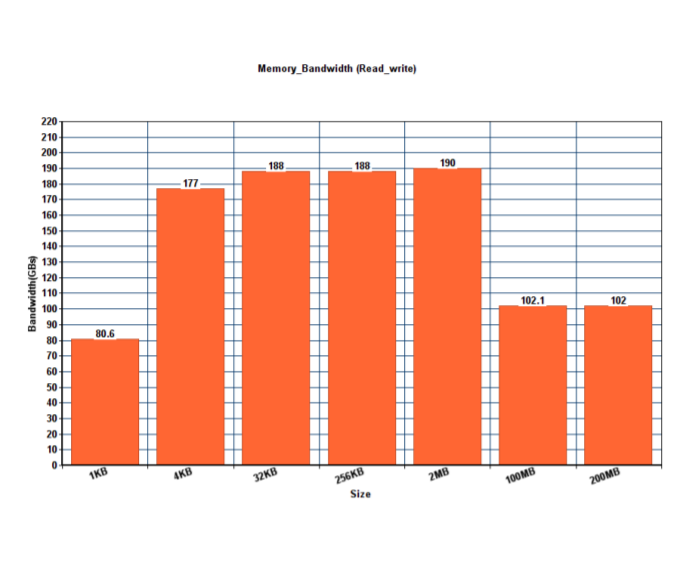
1. Measuring Read Bandwidth.

* To measure read bandwidth, we compute the sum of an array.

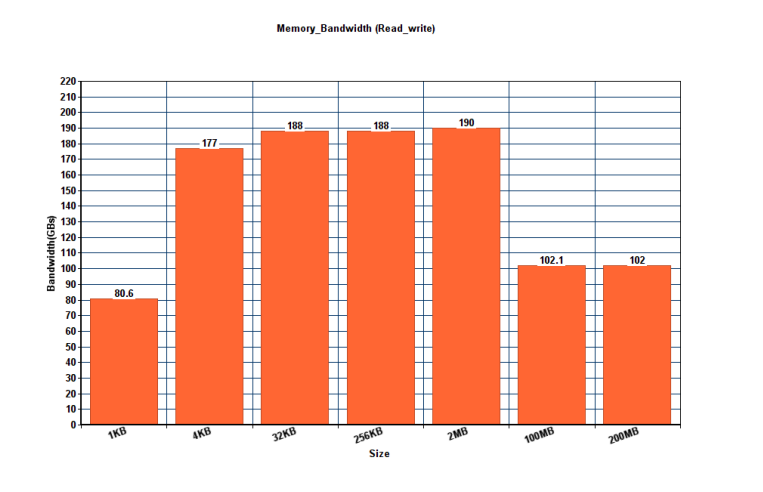


* We pass the array and the size of that array to read\_memory\_avx function.
* We basically calculate the sum of an array in that function using the add\_ps function.
* You need multiple h\_add often becasue it sums pairwise.
* We return the sum of the array where it was called.
* Now I took the bandwidth measurement at various sizes and plotted the graph displayed below.

2) Measuring Write bandwidth.



1. Measuring Read write bandwidth



**Measuring Latency**

