8x1 Multiplexer Using 4x1 Multiplexer

Group Number:- 16

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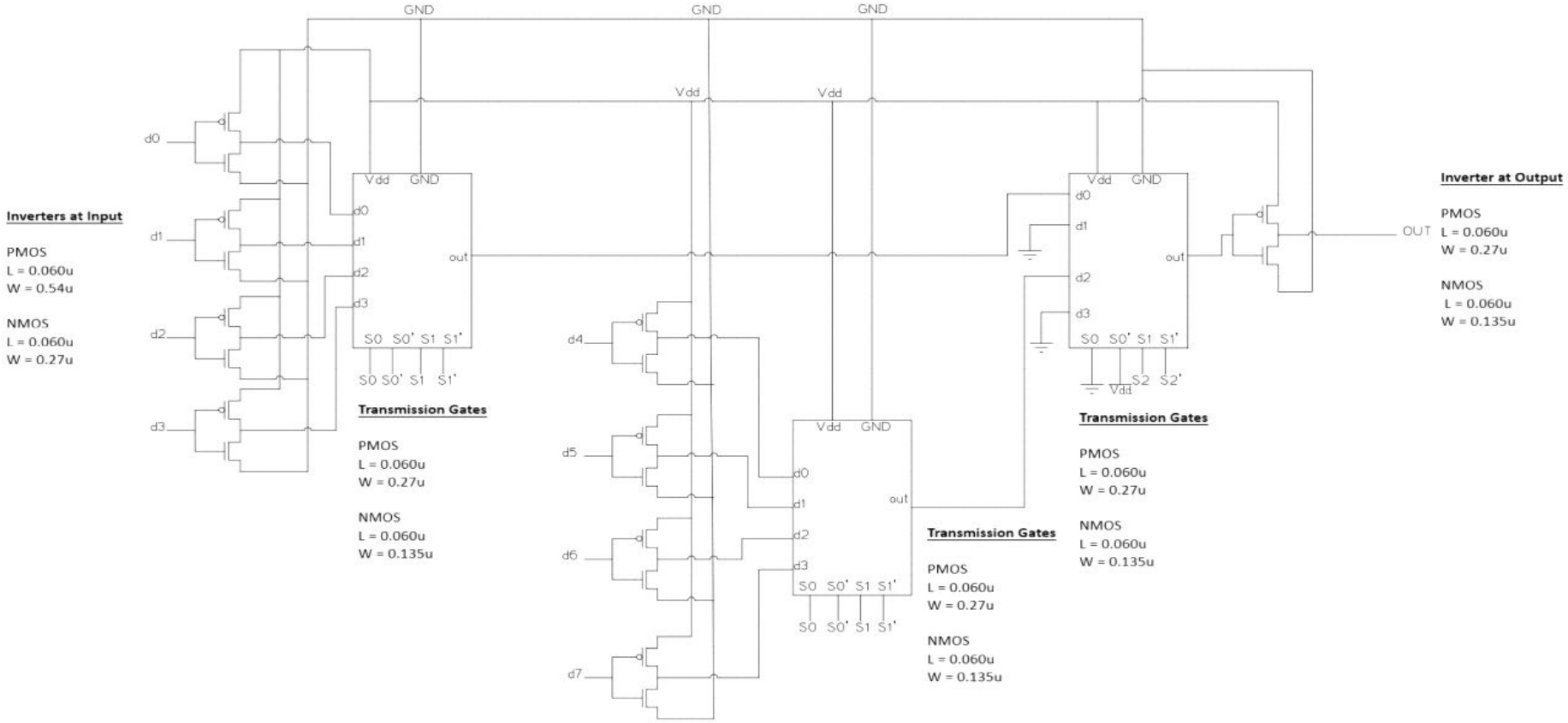
Schematic + Sizing



Inverters at Input

PMOS
L = 0.060u
W = 0.54u

NMOS
L = 0.060u
W = 0.27u

Transmission Gates

PMOS
L = 0.060u
W = 0.27u

NMOS
L = 0.060u
W = 0.135u

Transmission Gates

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Transmission Gates

PMOS
L = 0.060u
W = 0.27u

NMOS
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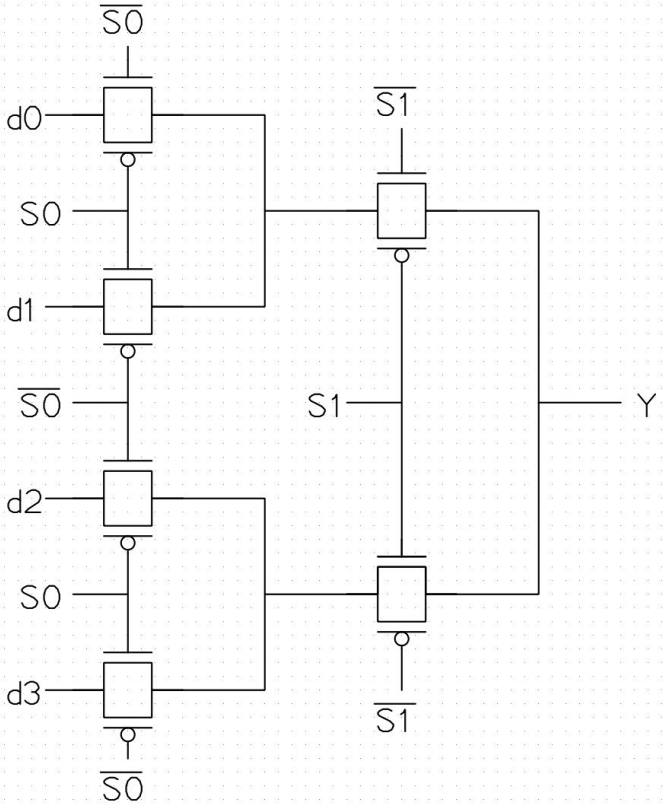
W = 0.135u

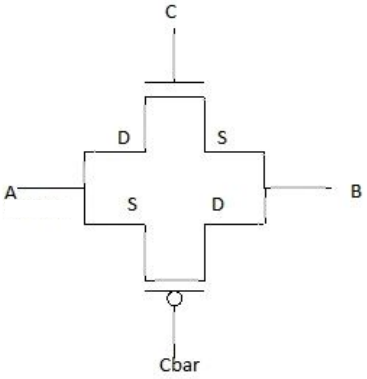
Inverter at Output

PMOS
L = 0.060u
W = 0.27u

NMOS
L = 0.060u
W = 0.135u

Inside 4x1 Mux





A	C	Cbar	B
0	0	1	H.Imp
1	0	1	H.Imp
0	1	0	0
1	1	0	1

Here we have used Transmission Gates to reduce the number of transistor as conventional 8x1 mux circuit has large no. of transistors which leads to higher delay, high power consumption and larger area.

Stimuli For Verification & Verification Plan

Delay Calculations

Input D0 Toggle and Select Line Remain Constant

Delays	TT.lib	SS.lib
TPHL	325.76ps	421.03ps
TPLH	308.69ps	395.66ps

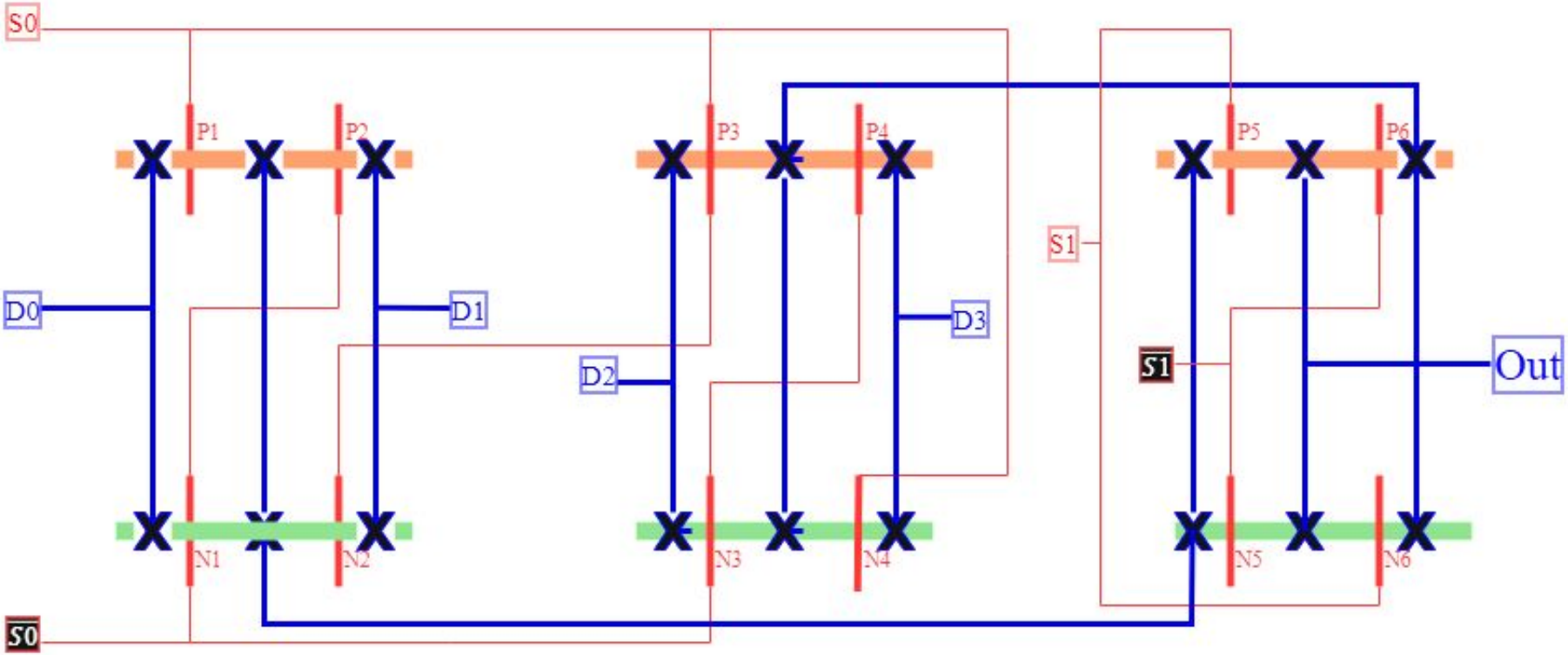
Input D0, S1 and S2 Constant S0 Toggle

Delays	TT.lib	SS.lib
TPHL	326.94ps	423.03ps
TPLH	298.15ps	380.92ps

Input D0, S0 and S1 Constant S2 Toggle

Delays	TT.lib	SS.lib
TPHL	209.77ps	268.76ps
TPLH	205.20ps	249.79ps

Stick Diagram For 4x1 Mux



Future Work + Work Distribution

Future Work:

- Try to decrease delay by using a 2x1 mux for final stage.
- Make Layout and try to minimize the area.
- Post layout simulations along with parasitic extraction.

Work Distribution:

- Virtuoso Schematic, Simulations, Delay Calculations : Abhinav Maurya
- XCircuit Schematic : Vanshika Sharma, Priyansh Pal
- Stick Diagram : Chandra M M. Dodda