

# 8x1 Multiplexer Using 4x1 Multiplexer

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Group Number:- 16

Guided By:- Dr. Anuj Grover

Group Members:-

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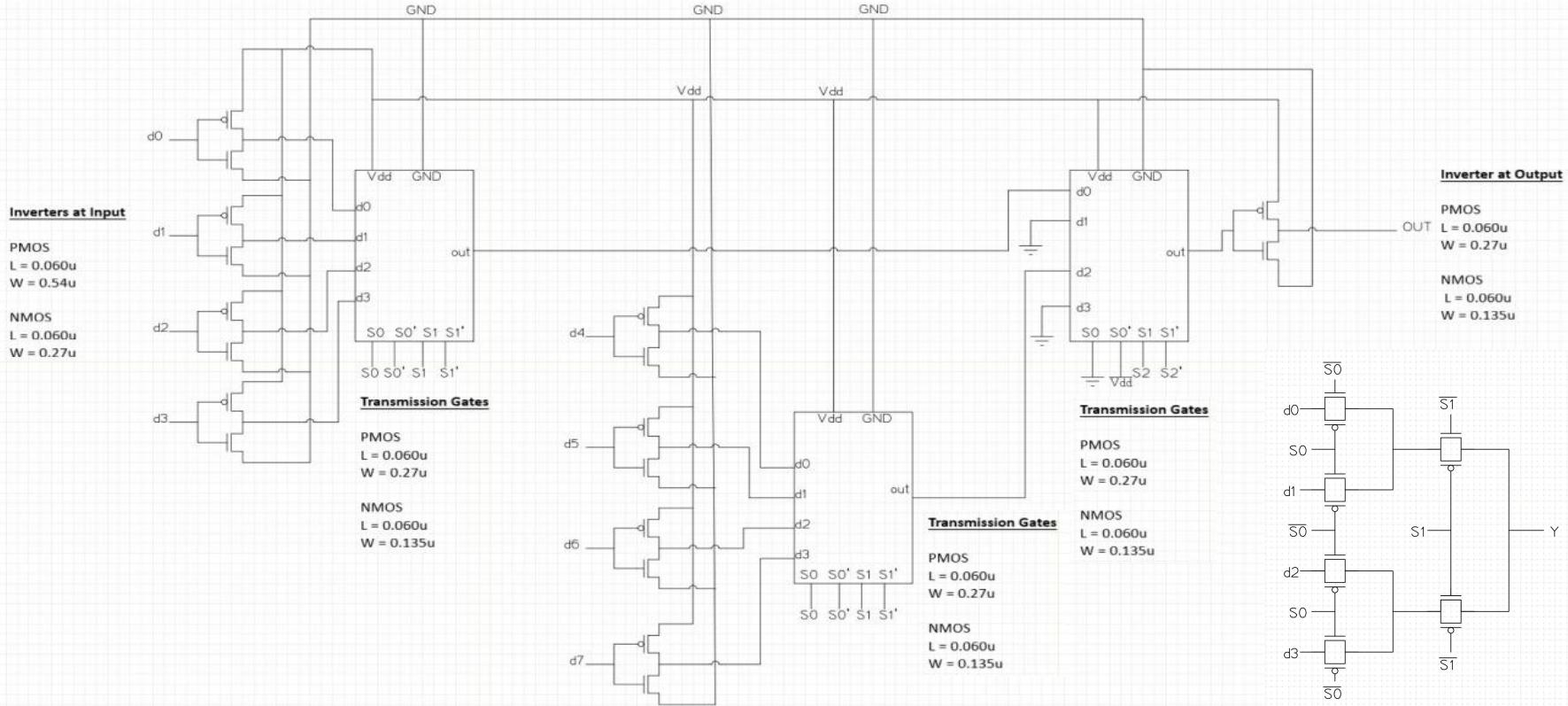
Vanshika Sharma (MT25155)

Chandra M M. Doddha (MT25110)

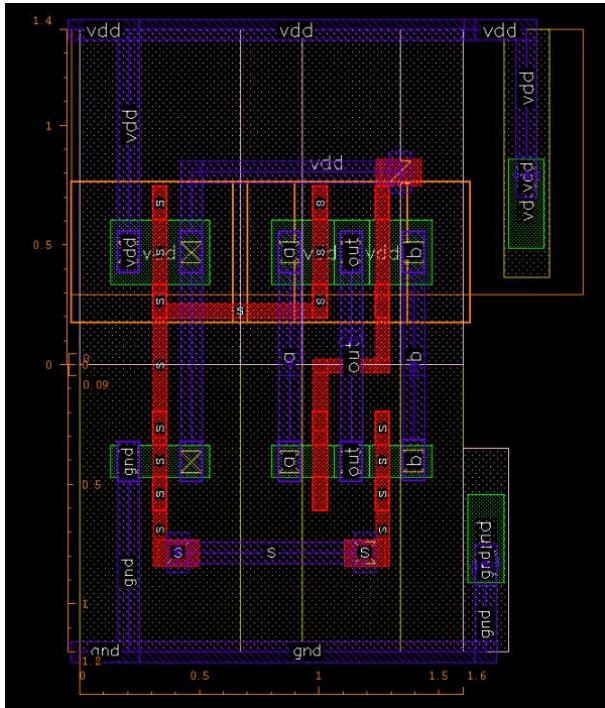


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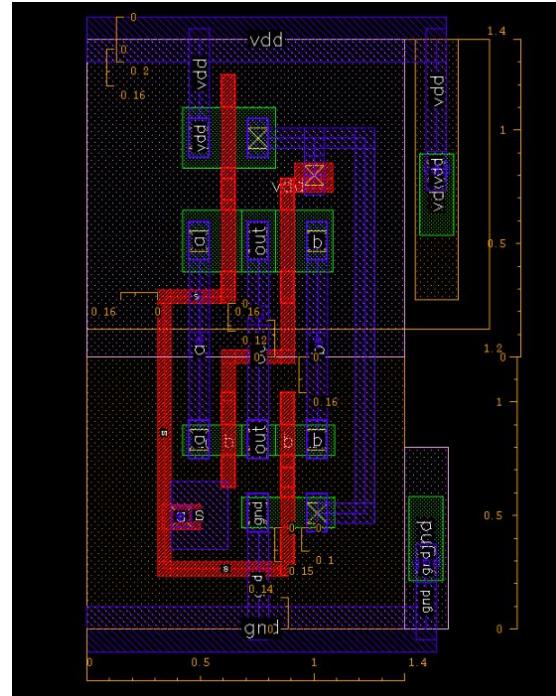
# Schematic + Sizing



# Layouts of 2x1 Mux

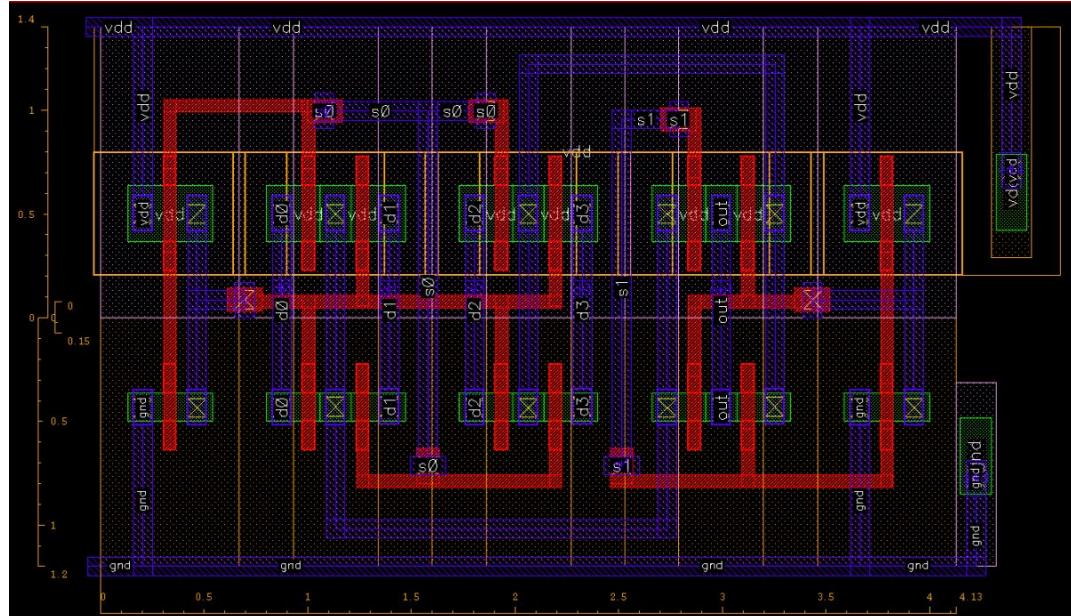


8 Tracks of M3 =>  $8 \times 0.2 = 1.6\mu\text{m}$   
Area =  $2.6 \times 1.6 = 4.16\mu\text{m}^2$

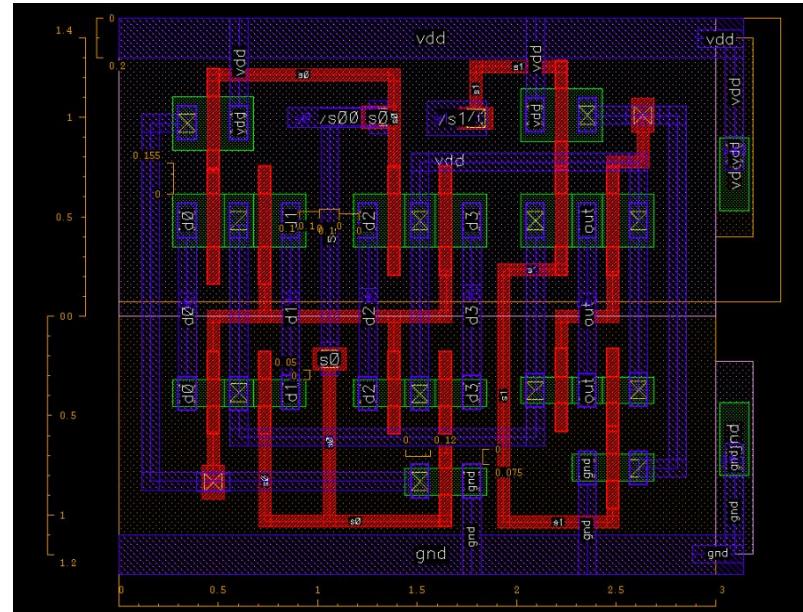


7 Tracks of M3 =>  $7 \times 0.2 = 1.4\mu\text{m}$   
Area =  $2.6 \times 1.4 = 3.64\mu\text{m}^2$

# Layouts of 4x1 Mux

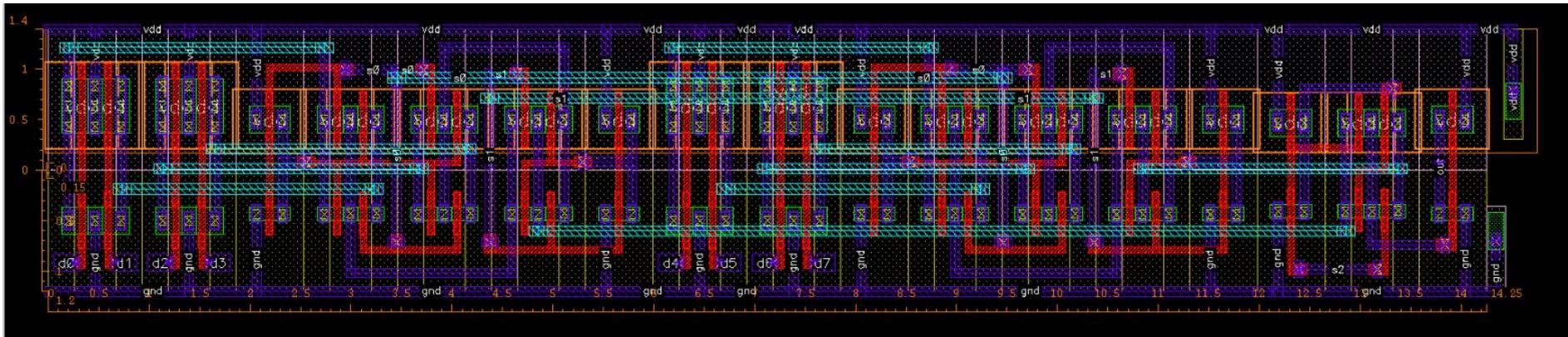


21 Tracks of M3 =>  $21 \times 0.2 = 4.2\text{um}$   
Area =  $2.6 \times 4.2 = 10.92\text{um}^2$



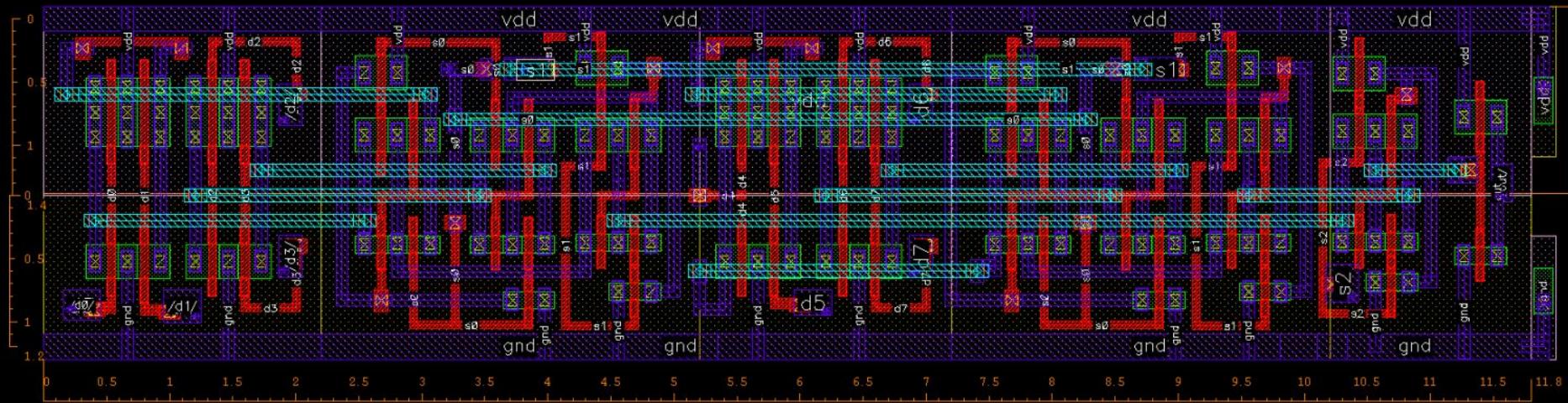
15 Tracks of M3 =>  $15 \times 0.2 = 3\text{um}$   
Area =  $2.6 \times 3 = 7.8\text{um}^2$

# 1st Layout of 8x1 Mux



72 Tracks of M3 =>  $72 \times 0.2 = 14.4\mu m$   
Area =  $2.6 \times 14.4 = 37.44\mu m^2$

## Final Layout of 8x1 Mux



59 Tracks of M3 =>  $59 \times 0.2 = 11.8\text{um}$   
Area =  $2.6 \times 11.8 = 30.68\text{um}^2$

We are able to reduce 13 tracks in the final layout that saves 6.76um<sup>2</sup> of area.

# DRC/LVS Reports of Final Layout



The screenshot shows two side-by-side windows of the Calibre RVE interface.

**Left Window (DRC Report):** The title bar says "Calibre - RVE v2013.1.34.21 : mux\_8x1\_n.drc.results". The menu bar includes File, View, Highlight, Tools, Window, Setup. The toolbar has icons for Open, Save, Print, etc. A search bar is at the top. The main area displays a table of results:

Layout Cell Type	Source Cell	Net	Instance	Port
mux_8x1_n	mux_8x1_n	34L_34S	56L_56S	14L_14S

**Right Window (LVS Report):** The title bar says "Calibre - RVE v2013.1.34.21 : svdb mux\_8x1\_n". The menu bar includes File, View, Highlight, Tools, Window, Setup. The toolbar has icons for Open, Save, Print, etc. A search bar is at the top. The main area displays a table of results:

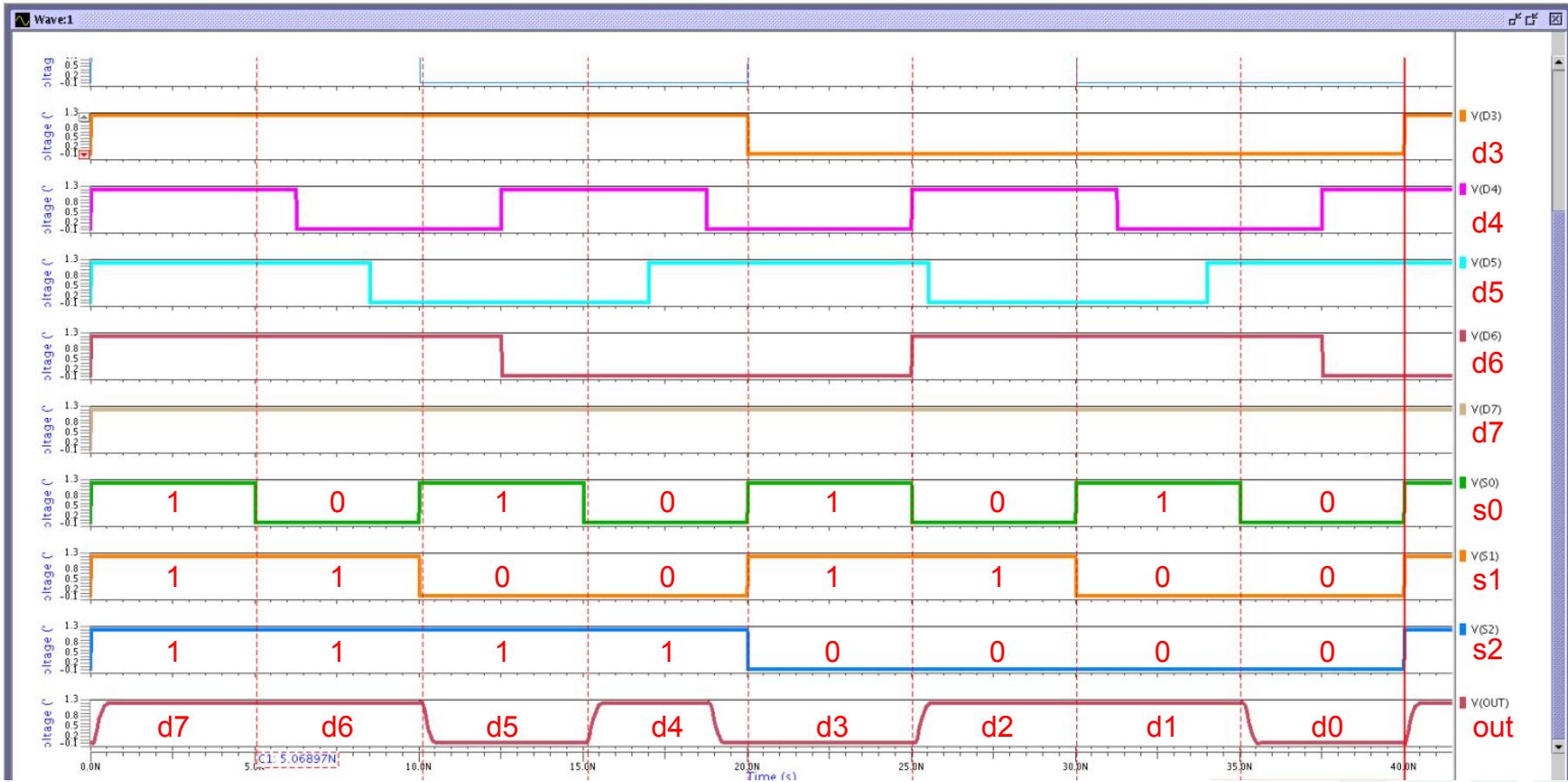
Layout Cell Name	Source Cell Name	Cell Comparison Results (Top Level)
mux_8x1_n	mux_8x1_n	CORRECT

Below this, there are sections for "NUMBER OF OBJECTS" and "INFORMATION AND WARNINGS".

DRC Report (No Unresolved DRC Error)

Clean LVS Report

# Post Layout Simulation For Functional Verification



# Pre/Post Layout Delay Calculations



Input Lines constant and One Select Line toggles at a Time

Worst Case Delay

Select Lines are Constant and D0 input toggles

Best Case Delay

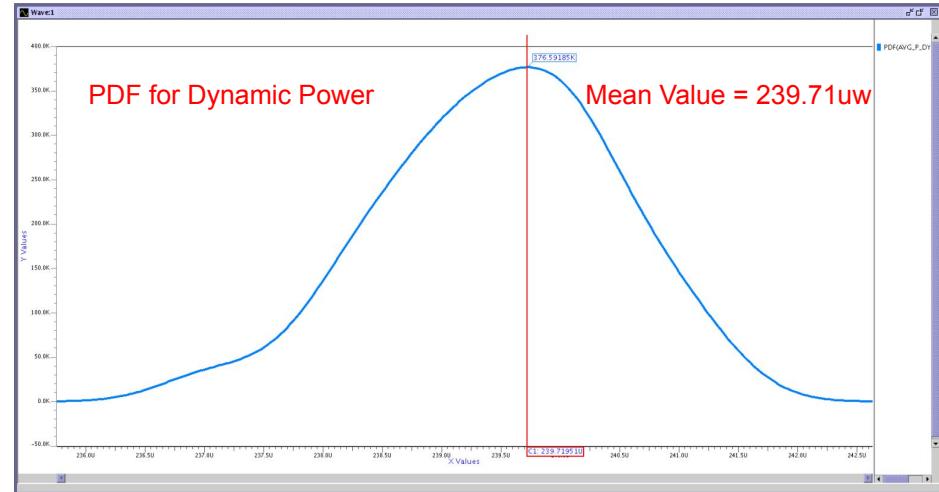
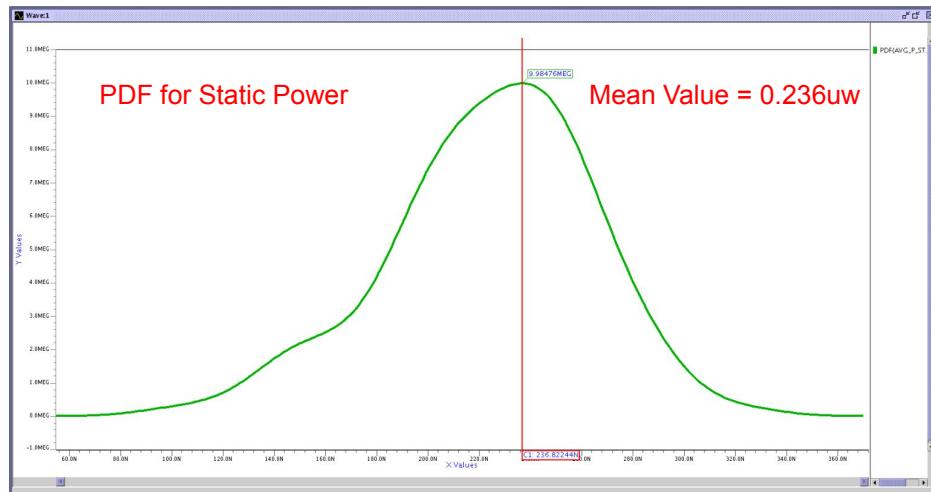
Input Lines and Select lines	Delays	Pre-layout Simulation		Post-layout Simulation	
		TT.lib	SS.lib	TT.lib	SS.lib
D0=1 D1 to D7 = 0 S0 toggles S1, S2 = 0	TPHL_S0	212.17ps	358.25ps	257.93ps	433.39ps
	TPLH_S0	206.20ps	337.39ps	247.70ps	411.93ps
D0=1 D1 to D7 = 0 S1 toggles S0, S2 = 0	TPHL_S1	202.30ps	339.84ps	248.70ps	417.61ps
	TPLH_S1	196.18ps	319.05ps	233.69ps	384.10ps
D0=1 D1 to D7 = 0 S2 toggles S0, S1 = 0	TPHL_S2	176.62ps	292.61ps	197.95ps	326.94ps
	TPLH_S2	172.06ps	273.87ps	190.09ps	302.14ps
S0,S1,S2 = 0 D0 toggles	TPHL_D0	215.07ps	364.64ps	261.74ps	440.18ps
	TPLH_D0	211.35ps	345.80ps	253.23ps	422.77ps

# Power Calculations and Monte Carlo For Power

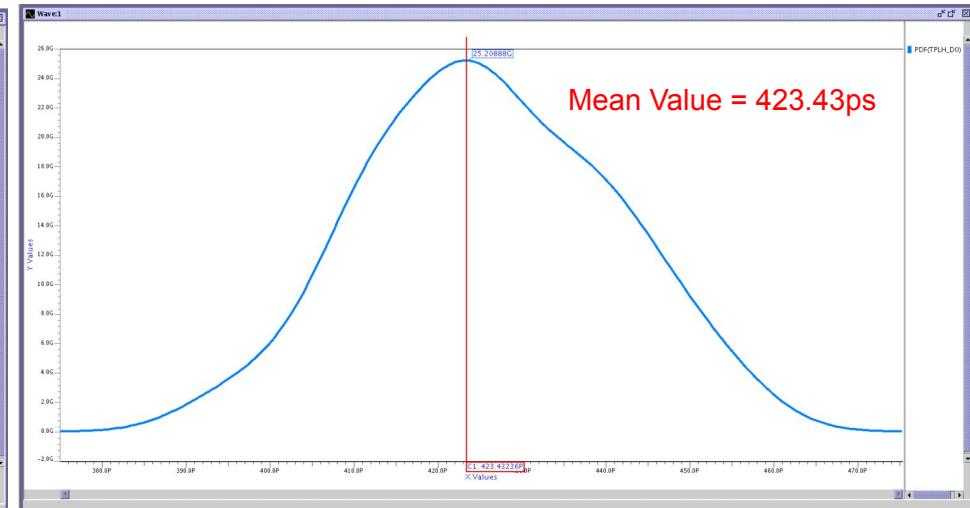
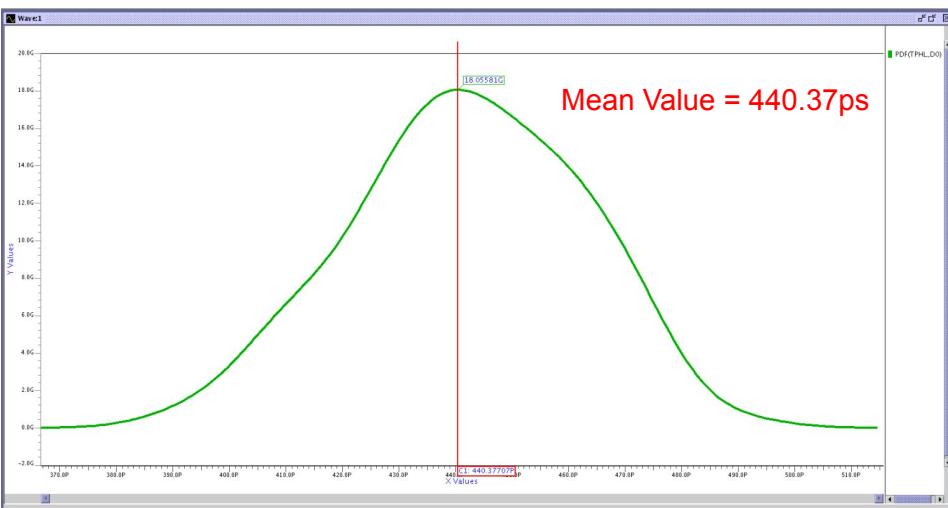


For Worst Case Power Calculation  
PVT = FF,1.32V,-40

Power	Pre Layout	Post Layout
Dynamic Power	163.40uw	239.83uw
Static Power	0.393uw	0.234uw



# Monte Carlo Simulations for Worst Case Delay



Ran Monte Carlo Simulations for the worst case of delay calculations and got these Probability Density Function Graph of TPHL(Green) & TPLH (Blue) for PVT = SS,1.08V,125C.

# Conclusion/Work Distribution/Future Work

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## Conclusion:

We are able to make a complete layout of 8x1 Mux using the standard cells of 4x1 Mux. We did many iterations on the layout to reduce the area of the final layout

## Work Distribution:

- Abhinav Maurya -> Layout, Power Calculations, Post Layout & Monte Carlo Simulations
- Vanshika Sharma, Priyansh Pal -> XCircuit Schematic & Parasitic Extractions
- Chandra M M. Doddha -> Delay Calculation