**KAJOL BHUTADA**

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**OBJECTIVE**

Seeking a full-time in physical design where I can put my technical skills using my academic knowledge.

**EXPERIENCE**

**SOC Design Engineer Intern at Intel Corporation, Folsom CA (June 2022 – Present)**

* Responsible for Converging block level Timing/Power/Area for core design.
* Responsible for Setup/Hold path solving by looking into PVT scenarios.
* Responsible for handling multiple blocks at same time and been successful in multitasking and meeting tight timeline.
* Understanding of Design collateral and its impact of Block closure. Familiar in solving complex min/max timing paths by working with senior Engineers.
* Scripting done to speed up day to day task.
* Owned 4 block in parallel in ECO phase of project, fixes done to minimize the loops of the design.

**Portland State University (Jan 2021 – Present)**

2 years of Academic experience in CMOS Design, Physical aspect of chip design and ASIC flow.

**EDUCATION**

Portland State University, Portland, OR (Expected Graduation Winter 2023)

M.S in Electrical and Computer Engineering **(GPA: 4 /4)**

SRM University, India (May 2016)

B. Tech in Electrical and Computer Engineering **(GPA: 7.6 /10)**

**ACADEMIC SUMMERY**

* Coursework in Microprocessor System Design, Computer Architecture, ASIC Modelling and Synthesis, Low Power Design.
* Good academic knowledge in Digital Integrated Circuit Design.
* Experience in C, C++, Verilog, System Verilog.
* Familiar with DC/ICC/PT tools for optimize design for PPA.
* Investigated Layouts of ISO cells, Level shifter cells and AON cells.

**TECHNICAL SKILLS**

* EDA and Simulation Tools: Cadence Virtuoso editor, ModelSim, QuestaSim, PT/ICC/DC, Synopsys DC compiler, Synopsys Prime Time, Cadence Innovus.
* Hardware Languages: Verilog, System Verilog.
* Programming Languages: C, C++.
* Scripting Languages: TCL, UNIX.
* OS: LINUX, Windows

**ACADEMIC PROJECTS**

# [DC Compiler] Synthesis of 4-bit counter

* Designed/synthesized 4-bit counter to analyze the PPA of the design.
* Analyzed max critical path to understand the delay trend on data path w.r.t clock path with given libs.
* Analyzed gate count and tried to do the RTL optimization to reduce the overall Area.

# [CADENCE] Standard cell design using Cadence Virtuoso tool.

* Designed a CMOS Invertor using Cadence Virtuoso tools for different loads: FO0, FO1, FO2, FO4, FO8 and with respective input slews.
* Simulated DC & transient analysis to calculate cell rise/fall delay, rise/fall slew.

# [DC/ICC/PT] RTL2GDS for ORCA\_TOP design

* Ran floorplan aware synthesis by reading in the .def file along with SDC constraints, behavioral Verilog and. libs for given PVT corner. Analyzed the PPA at the end of syn to optimize the RTL
* Ran APR flow with/without using syn placement and compared QOR at end of route-opt.
* Analyzed the Dyn/Leak power at every stage of APR to understand the effect of gate count on power.

# [System Verilog] Design/simulation of L1 cache in multiprocessor system using MESI protocol.

* Designed a L1 cache simulator (16k sets of 64byte lines) with 4-way set associative using LRU replacement policy for a new 32-bit processor in a shared memory configuration in a multiprocessor system using MESI Protocol. TCL/UNIX] Automation using TCL
* **[TCL/UNIX] Automation using TCL**
* Wrote a script to collect data from the log file and count Number of errors in the log file.
* Wrote an automation to find out number of ports in Verilog modules
* Familiar with python programming and have done hands on few basic codes
* Familiar with grep/awk/sed usage in Unix.