

Sri Sai Vidya Vikas Shikshana Samithi ®

**SAI VIDYA INSTITUTE OF TECHNOLOGY**

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**Syllabus:**

**Bipolar Junction Transistors:** Introduction, BJT Voltages & Currents, BJT Amplification, Common Base Characteristics, Common Emitter Characteristics, Common Collector Characteristics, BJT Biasing: Introduction, DC Load line and Bias point.

**Field Effect Transistor:** Junction Field Effect Transistor, JFET Characteristics, MOSFETs: Enhancement MOSFETs, Depletion Enhancement MOSFETs.

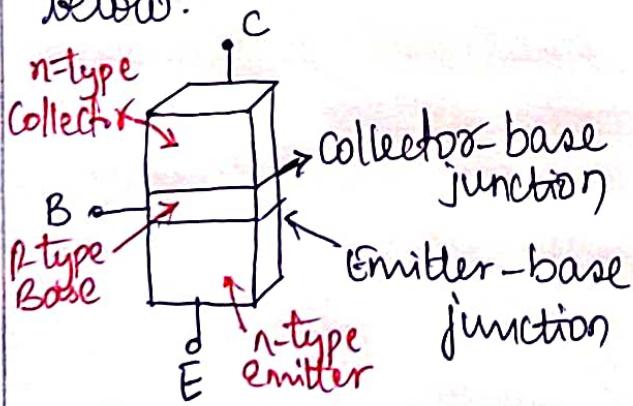
Syllabus:

Bipolar junction transistors: Introduction , BJT Voltages and currents, BJT Amplification, common Base, common Emitter, common collector characteristics, BJT Biasing : Introduction, Dc load line and Bias point.

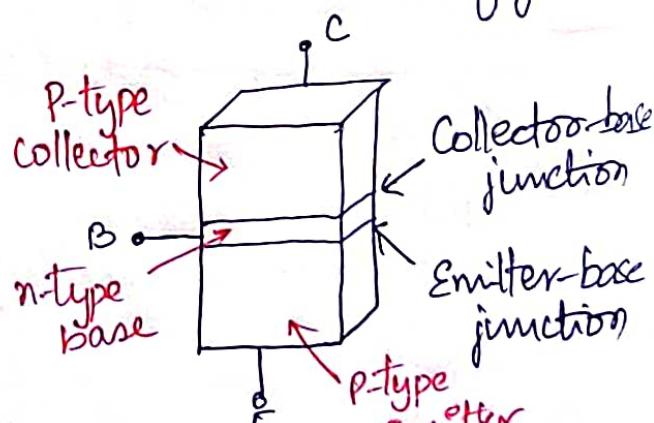
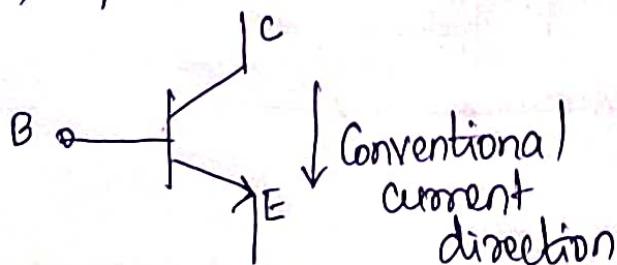
Field effect transistor: junction field effect transistor, JFET characteristics, MOSFET'S: Enhancement MOSPET'S, Depletion Enhancement MOSPET'S.

Introduction:

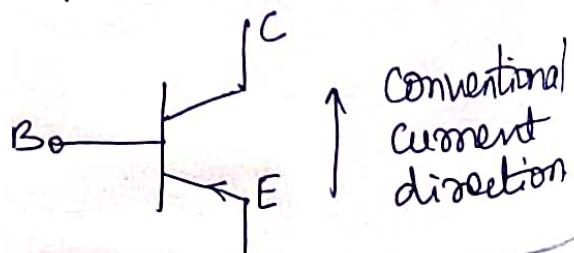
- A bipolar junction transistor (BJT) has three layers of semiconductor material.
- These are arranged either in npn sequence or in pnp sequence , and each of the three layers has a terminal.
- The transistor can be used for current amplification
- The two types of transistors are shown in figure below.



a) npn transistor



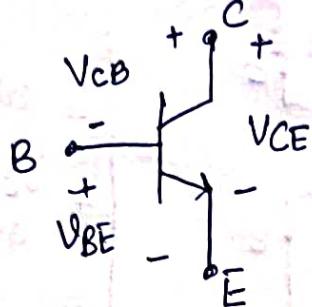
b) pnp transistor.



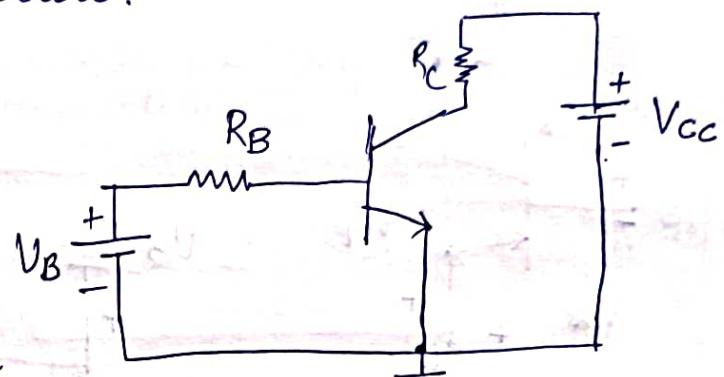
## BJT Voltages and Currents:

### Terminal Voltages: a) n-p-n transistor:

- The terminal voltage polarities for an npn transistor are shown in figure below.



a) npn terminal voltage polarities

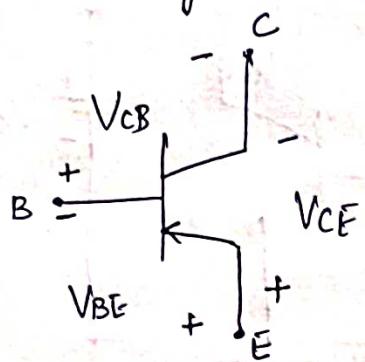


b) voltage source connection.

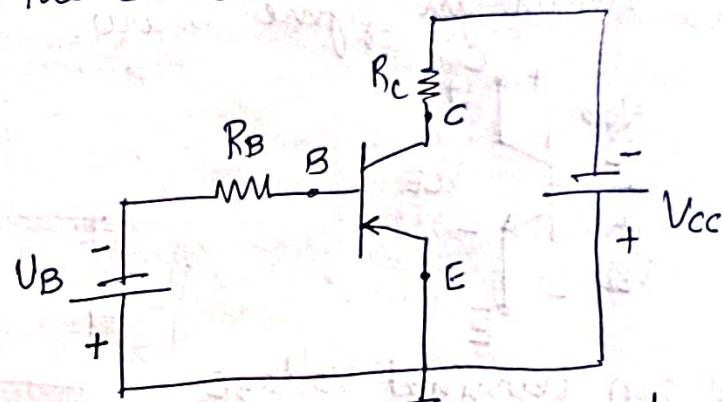
- For an npn transistor, the base is biased positive w.r.t emitter, and collector is then biased to higher positive voltage than base.
- Fig (b) shows, that the voltage sources are usually connected to the transistors via resistors.
- The base voltage  $V_B$  is connected via resistor  $R_B$ , and the collector supply  $V_{cc}$  is connected via  $R_c$ .
- The negative terminals of the two voltage sources are connected at the transistor emitter terminal.
- $V_{cc}$  is always much larger than  $V_B$  and this ensures that the collector-base junction remains reverse-biased: positive on collector (n-side) and negative on base (p-side).
- Typical transistor base-emitter voltages are similar to the diode forward voltages: 0.7V for a silicon transistor and 0.3V for a germanium device.
- Collector voltages might be from 3V to 20V for many of a transistor.

## b) pnp transistors

- For pnp device, the base is biased negative with respect to the emitter, and the collector is made more negative than the base.



fig(a): pnp terminal  
Voltage polarities



b) voltage source connection.

- Voltage sources are connected via resistors, and the source positive terminals connected at the emitter.
- With  $V_{CC}$  larger than  $V_B$ , the collector is more negative than the (n-type) base and thus the collector-base junction is kept reverse-biased.
- \* All BJT's (pnp & pnp) are normally operated with the collector-base junction reverse-biased and the base-emitter junction forward-biased.

## Transistor Currents:

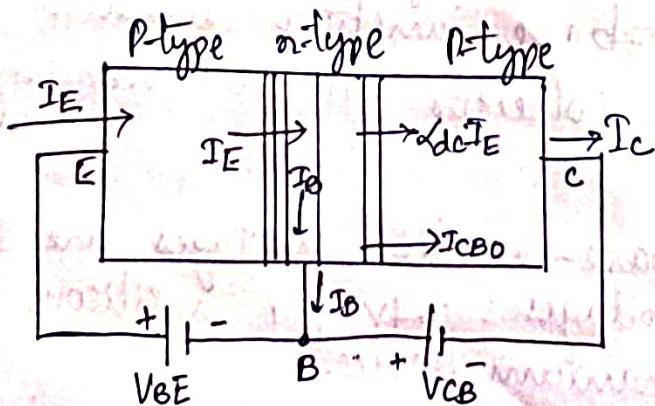
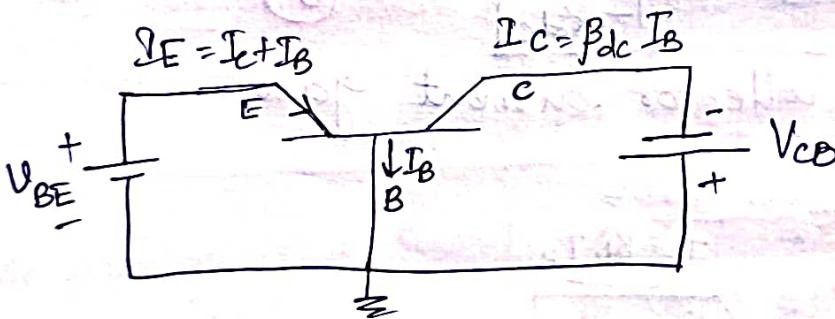


fig: currents in a pnp transistors.

- \* The collector current ( $I_c$ ) approximately equals to emitter current ( $I_E$ ).
- \* The base current ( $I_B$ ) is very much smaller than  $I_E$ .
- \* A very small reverse leakage current ( $I_{CBO}$ ) occurs at the collector-base junction.
- \* The various current components that flow within a transistor is shown in figure.
- \* The current flowing into the emitter terminal is referred to as emitter current ( $I_E$ ), collector terminal as collector current ( $I_c$ ), base terminal as base current ( $I_B$ ).
- \* Both  $I_c$  and  $I_B$  flow out of the transistor while  $I_E$  flows into the transistor.

$$\therefore I_E = I_c + I_B \rightarrow ①$$



- \* Most of the emitter current  $I_E$  crosses to the collector and only a small portion flows out of the base terminal.

$$\therefore I_c = \alpha_{dc} \cdot I_E \rightarrow ②$$

where,  $\alpha_{dc}$  - emitter to collector current gain.

- Because the collector-base junction is reverse-biased, a very small reverse saturation current ( $I_{CBO}$ ) flows across the junction.
- $I_{CBO}$  is named as collector-base leakage current, and is normally small and it can be ignored.

Substitute Eq<sup>n</sup> ① in ②,

$$I_C = \alpha_{dc} (I_C + I_B) \rightarrow ③$$

$$I_C = \alpha_{dc} I_C + \alpha_{dc} I_B.$$

$$I_C - \alpha_{dc} I_C = \alpha_{dc} I_B$$

$$I_C (1 - \alpha_{dc}) = \alpha_{dc} I_B$$

$$\boxed{I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}}} \rightarrow ④$$

Eq<sup>n</sup> ④ can be written as,

$$\boxed{I_C = \beta_{dc} \cdot I_B} \rightarrow ⑤$$

where,

$$\boxed{\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}} \rightarrow ⑥$$

$\beta_{dc}$  = base to collector current gain.

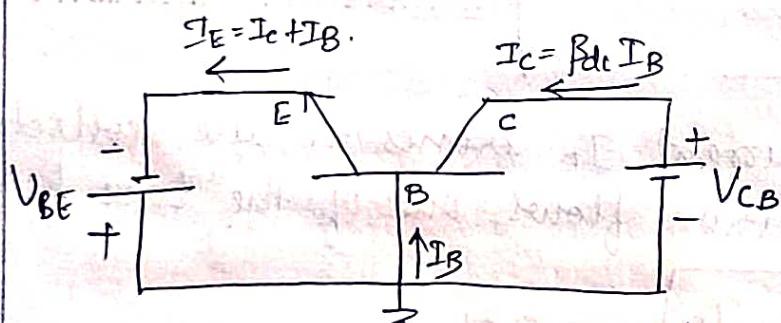


fig: Terminal currents for npn transistors.

- \* Here in npn transistor  $I_B$  and  $I_C$  are assumed to flow into the device and  $I_E$  is taken as flowing out.
- \* Since electrons are the majority charge carriers in npn transistor, they move in a direction opposite to conventional current direction.

problem:

- ① Calculate  $I_c$  and  $I_E$  for a transistor that has  $\alpha_{dc} = 0.98$  and  $I_B = 100\mu A$ . Determine the value of  $\beta_{dc}$  for the transistor.

Soln: Given:  $\alpha_{dc} = 0.98$ ,  $I_B = 100\mu A$ .

$$\beta_{dc} = ? \quad I_c = ?, \quad I_E = ?$$

$$I_c = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} = \frac{0.98 \times 100\mu A}{1 - 0.98}$$

$$\boxed{I_c = 4.9mA}$$

$$\text{WKT, } I_c = \alpha_{dc} \cdot I_E$$

$$I_E = \frac{I_c}{\alpha_{dc}} = \frac{4.9mA}{0.98}$$

$$\boxed{I_E = 5mA}$$

$$\text{WKT, } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98}$$

$$\boxed{\beta_{dc} = 49}$$

- ② Calculate  $\alpha_{dc}$  and  $\beta_{dc}$  for the transistor shown, if  $I_c$  is measured as  $1mA$  and  $I_B$  is  $25\mu A$ . Determine the new base current to give  $I_c = 5mA$ .

Soln: Given:  $\alpha_{dc} = ?$ ,  $\beta_{dc} = ?$

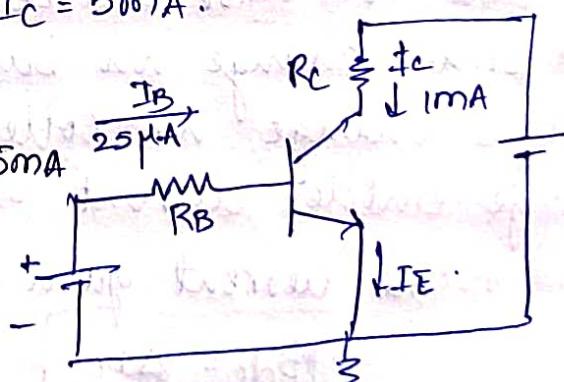
$$I_{B\text{new}} = ? \text{ for } I_c = 5mA$$

$$I_c = 1mA \quad \& \quad I_B = 25\mu A$$

$$\text{WKT, } \beta_{dc} = \frac{I_c}{I_B}$$

$$= \frac{1mA}{25\mu A}$$

$$\boxed{\beta = 40}$$



$$I_E = I_c + I_B \Rightarrow I_E = 1mA + 25\mu A, \boxed{I_E = 1.025mA}$$

$$\text{WKT, } \alpha_{dc} = \frac{I_c}{I_E} = \frac{0.1mA}{1.025mA}$$

$$\boxed{\alpha_{dc} = 0.976}$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{5mA}{40}$$

$$\boxed{I_B = 125\mu A}$$

- ③ Determine  $\alpha_{dc}$  and  $I_B$  for a transistor that has  $I_C$  equal to  $2.5mA$  and  $I_E = 2.55mA$ . Calculate  $\beta_{dc}$  for the transistor?
- ④ A transistor has measured currents of  $I_C = 3mA$  and  $I_E = 3.03mA$ . Calculate new current levels when the transistor is replaced with a device that has  $\beta_{dc} = 75$ . Assume that  $I_B$  remains constant.

### BJT Amplification

#### Current Amplification:

$$\text{WKT, } I_C = \alpha_{dc} \cdot I_E \rightarrow ①$$

Thus, transistor can be used for current amplification.

- \* A small change in base current ( $\Delta I_B$ ) produces a large change in collector current ( $\Delta I_C$ ) and a large emitter current change ( $\Delta I_E$ )

$\therefore$  The current gain from base to collector is

$$\boxed{\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}}$$

$\rightarrow ②$

- \* The increasing and decreasing levels of input and output currents may be defined as alternating quantities.

- The alternating current gain from base to collector is

$$B_{ac} = \frac{I_c}{I_b} \rightarrow (3)$$

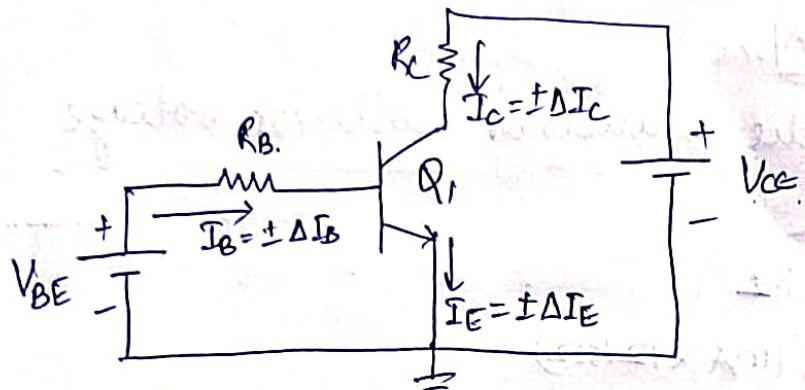
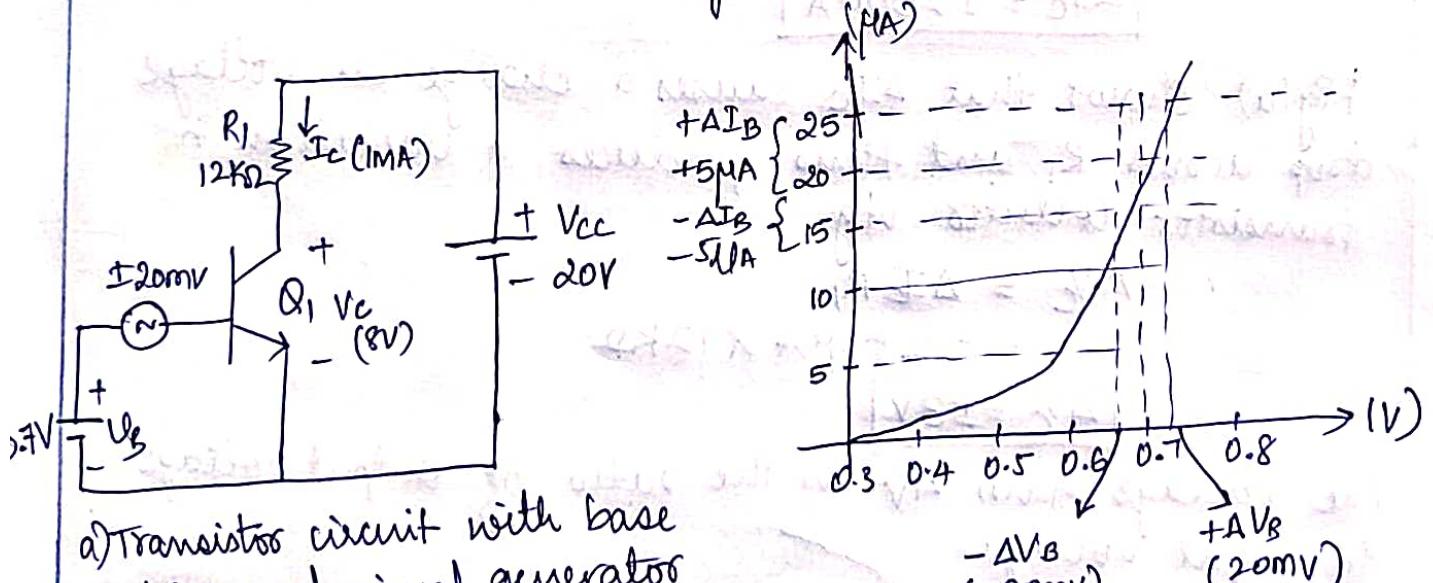


fig: current levels and current changes.

## ② Voltage Amplification:

→ Assume that the transistor  $Q_1$  has  $\beta_{dc} = 50$ . The 0.7V dc voltage source ( $V_B$ ) forward biases the transistor emitter-base junction.



a) Transistor circuit with base bias and signal generator

b)  $V_B$  changes produce  $I_B$  changes

- An AC signal source ( $v_i$ ) in series with  $U_B$  provides a  $\pm 20mV$  input voltage.
- The transistor collector is connected to a 20V dc voltage source  $V_C$  via a  $12k\Omega$  collector resistor  $R_C$ .

From fig (b)  $I_B = 20 \mu A$ .

$$\begin{aligned}\therefore I_C &= \beta_{dc} \cdot I_B \\ &= 50 \times 20 \mu A \\ \boxed{I_C} &= 1mA\end{aligned}$$

- The dc level of the transistor collector voltage can now be,

$$\begin{aligned}V_C &= V_{cc} - I_C R_L \\ &= 20 - (1mA \times 12k\Omega) \\ \boxed{V_C} &= 8V\end{aligned}$$

- The  $I_B$  change produces a change in collector current.

$$\begin{aligned}\Delta I_C &= \beta_{dc} \Delta I_B \\ &= 50 \times (\pm 5 \mu A) \\ \boxed{\Delta I_C} &= \pm 250 \mu A\end{aligned}$$

- Fig(a) shows that  $\Delta I_C$  causes a change in voltage drop across  $R_L$  and thus produces a variation in transistor collector vtg.

$$\begin{aligned}\Delta V_C &= \Delta I R_L \\ &= \pm 250 \mu A \times 12k\Omega \\ \boxed{\Delta V_C} &= \pm 3V\end{aligned}$$

- The voltage gain  $A_V$  is the ratio of output voltage to input voltage.

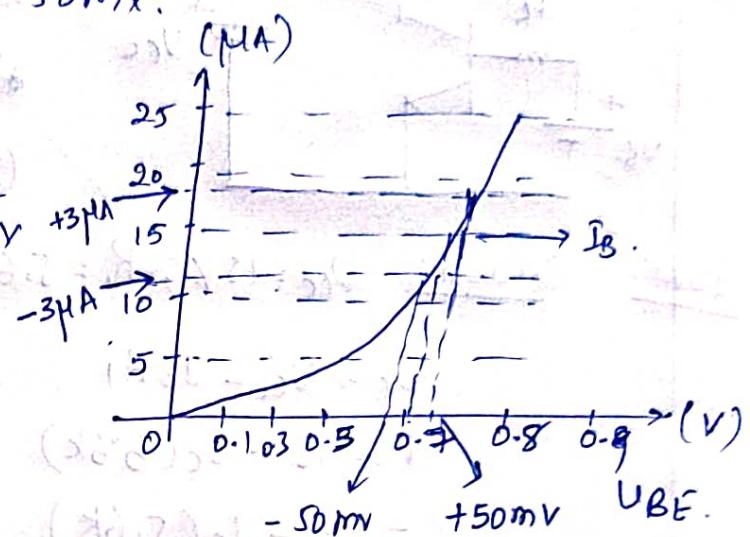
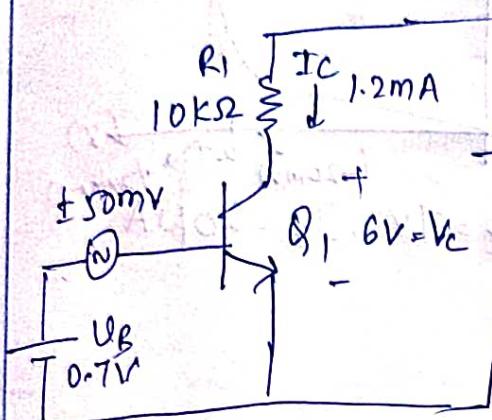
$$A_C = \frac{\Delta V_C}{\Delta V_B} = \frac{\pm 3V}{\pm 20mV}$$

$$\boxed{A_V = 150}$$

- The circuit ac input is the base voltage change  $\Delta V_B$  and the ac output is the collector voltage change ( $\Delta V_C$ ). Because the output is greater than the input, the circuit has a voltage gain. It is a voltage amplifier.

Problem.

- (a) Determine the dc collector voltage for the circuit (a) below. If the transistor has the  $I_B/V_{BE}$  characteristics shown in fig (b) and  $\beta_{dc} = \beta_{ac} = 80$ , calculate the circuit voltage gain when  $V_i = \pm 50mV$ .



from Ques.

$$I_B = 15\mu A \text{ for } V_B = 0.7V$$

$$I_C = \beta_{dc} \cdot I_B = 80 \times 15\mu A$$

$$\boxed{I_C = 1.2mA}$$

$$\begin{aligned} V_C &= V_{CC} - I_C R_1 \\ &= 18 - (1.2mA \times 10k\Omega) \\ \boxed{V_C = \pm 6V} \end{aligned}$$

from fig,  $I_b = \pm 3\mu A$ , for  $V_i = \pm 50mV$ .

$$\begin{aligned} I_C &= \beta_{ac} I_b \\ &= 80 \times \pm 3\mu A \end{aligned}$$

$$\boxed{I_C = \pm 240\mu A}$$

$$V_o = I_C R_1 = \pm 240\mu A \times 10k\Omega$$

$$\boxed{V_o = \pm 2.4V}$$

$$A_v = \frac{V_o}{V_i} = \frac{\pm 2.4V}{\pm 50mV} = 48.$$

$$\boxed{A_v = 48}$$

BJT Biasing - Process of setting or providing DC Voltage which helps in the functioning of the circuit.

### DC Load Line :-

- \* The DC load line for a transistor circuit is a straight line drawn on the transistor V-I characteristics.
- \* For common emitter (CE) circuit, the load line is a graph of collector current ( $I_C$ ) versus collector-emitter voltage ( $V_{CE}$ ). For a given value of collector resistance ( $R_C$ ) & a given supply voltage ( $V_{CC}$ ).
- \* The load line shows all corresponding levels of  $I_C$  &  $V_{CE}$  that can exist in a particular circuit.

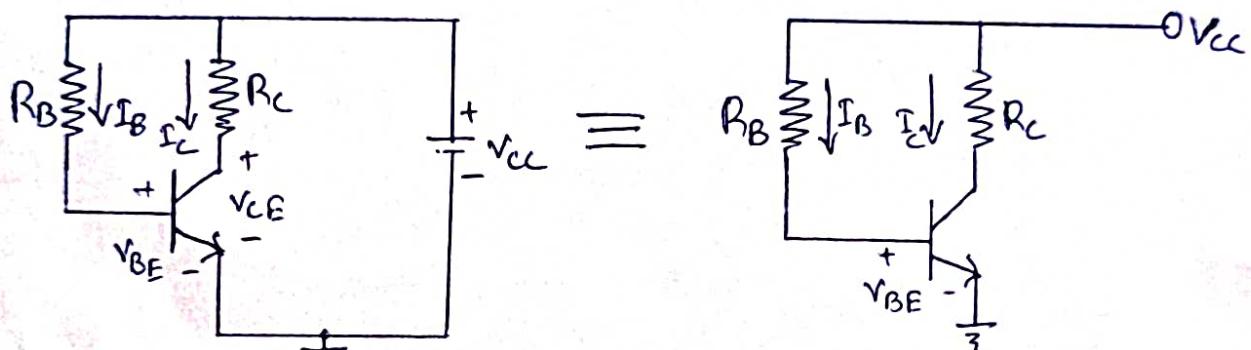


fig ① Transistor in CE configuration biased in Active region

- \* Consider an NPN transistor in CE configuration biased in active region.
- \* The DC supply voltage  $V_{CC}$  forward biases the base-emitter junction & reverse biases the collector-base junction.

Applying KVL to collector-emitter end we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE} \rightarrow ①$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \text{or}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = V_{CE} \left( -\frac{1}{R_C} \right) + \frac{V_{CC}}{R_C} \rightarrow ②$$

OR,

$$I_C = \left[ -\frac{1}{R_C} \right] V_{CE} + \frac{V_{CC}}{R_C} \rightarrow ②$$

- \* Equation ② is similar to the equation representing a straight line i.e.  $y = mx + c$

$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

$$y = mx + c$$

{ By comparison it is noted that along y-axis we have  $I_C$  & along x-axis we have  $V_{CE}$  with slope of line  $m = -1/R_C$

- \* To obtain a straight line consider 2 different conditions

1) put  $I_C = 0$ , in eq ①

$$I_B(MA)$$

2) put  $V_{CE} = 0$ , in eq ②

i.e.  $I_C R_C = V_{CC} - V_{CE} \rightarrow ①$

i) When  $I_C = 0$ , then  $V_{CE} = V_{CC}$

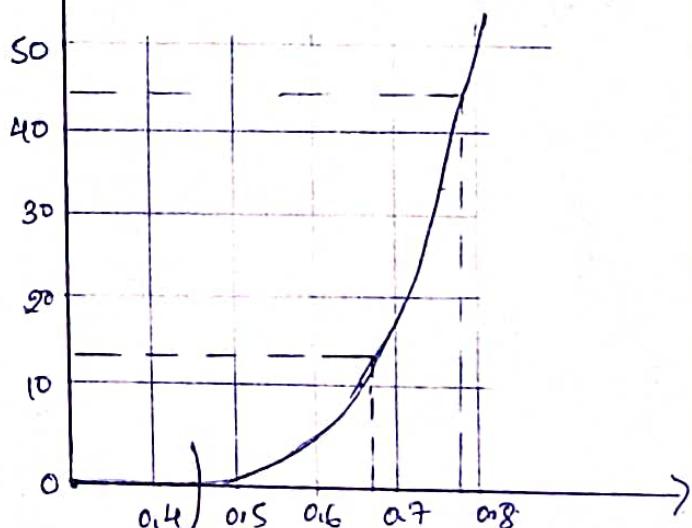
i.e.  $0 = V_{CC} - V_{CE}$ .

$$V_{CE} = V_{CC} \rightarrow ③$$

2) When  $V_{CE} = 0$ , then  $I_C = \frac{V_{CC}}{R_C}$

i.e.  $I_C R_C = V_{CC} - 0$ .

$$I_C = \frac{V_{CC}}{R_C} \rightarrow ④$$



b) Input characteristic of transistor.

- \* From eq ③ & ④ we will obtain a straight line on the o/p characteristics curve of the transistor circuit with 2 extreme points being  $(V_{CE}, I_C) = (V_{CC} - V_{CC}/R_C, 0)$ .

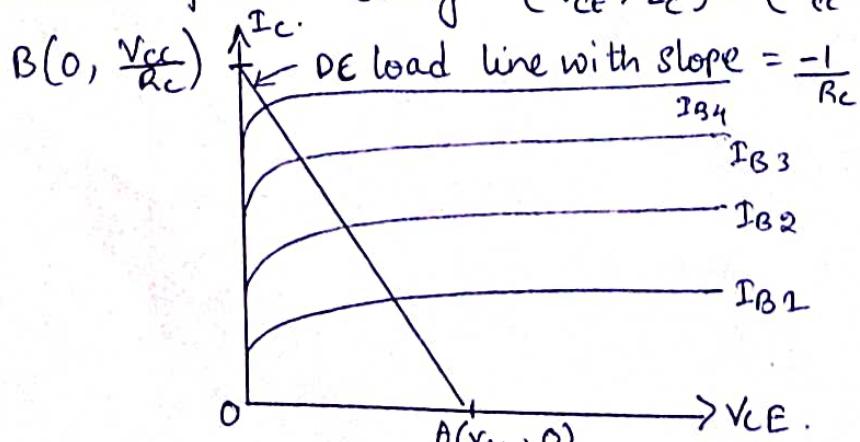
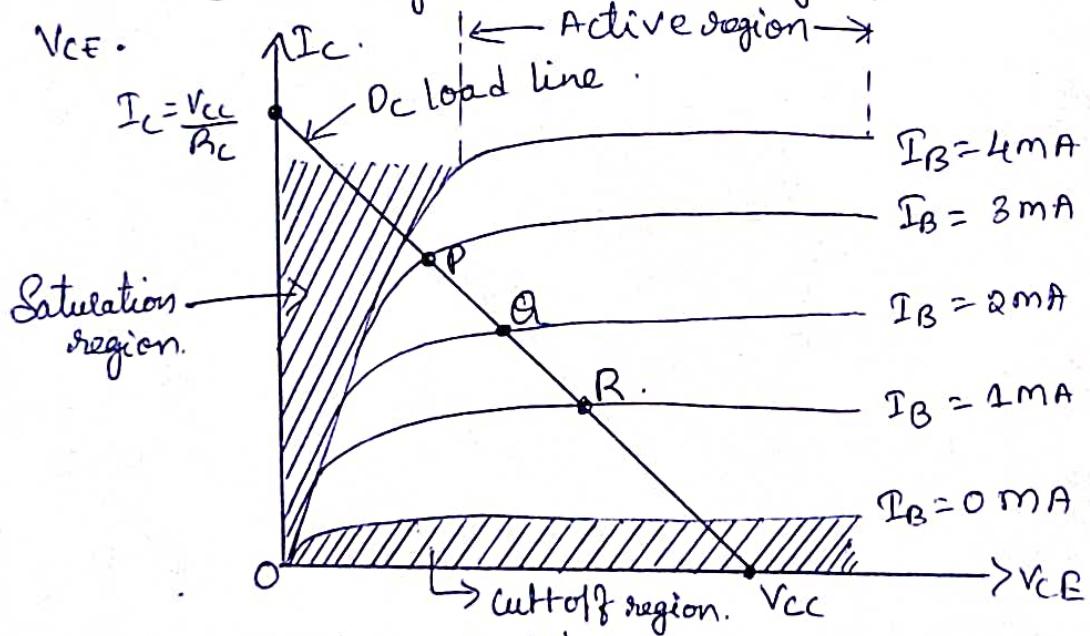


Fig ② DC load line drawn on transistor CE o/p characteristics.

- \* The straight line obtained by joining  $(V_{CE}, I_C)$  these points is called the DC load line as shown in above figure.

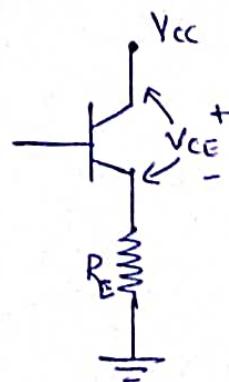
DC Bias point or Q-point or dc operating point or Quiescent point :-

- \* Q-point identifies the transistor collector current ( $I_C$ ) and collector-emitter voltage ( $V_{CE}$ ) when there is no ac signal at the base terminal.
- \* the intersection of DC load line with the OIP characteristic curve gives the co-ordinates of the Q-point.
- \* When a signal is applied to the transistor base,  $I_B$  varies according to the instantaneous amplitude of the signal. This causes  $I_C$  to vary & consequently produces a variation in  $V_{CE}$ .



Effect of Emitter Resistor :-

- \* In fig ① resistor  $R_E$  is in series with the transistor emitter terminal & the supply voltage connected directly to the collector terminal.
- \*  $R_E$  is the dc load.



$$\text{Fig ① } R_L(\text{dc}) = R_E$$

\* By applying KVL to collector-emitter circuit

$$V_{CC} - V_{CE} - I_E R_E = 0 \rightarrow ①$$

assuming  $I_E \approx I_c$

$$V_{CC} - V_{CE} - I_c R_E = 0.$$

$$I_c R_E = V_{CC} - V_{CE} \rightarrow ②$$

$$I_c = \frac{V_{CC} - V_{CE}}{R_E}$$

$$I_c = -\frac{V_{CE}}{R_E} + \frac{V_{CC}}{R_E}$$

$$I_c = \left( \frac{-1}{R_E} V_{CE} \right) + \frac{V_{CC}}{R_E} \rightarrow ③$$

i) put  $I_c = 0$  in eq ②.

$$V_{CE} = V_{CC} \rightarrow ④$$

(ii) put  $V_{CE} = 0$  in eq ②

$$I_c = \frac{V_{CC}}{R_E} \rightarrow ⑤$$

eq ④ & ⑤ are the dc load line points.

(iii) with  $R_C$  &  $R_E$  :-

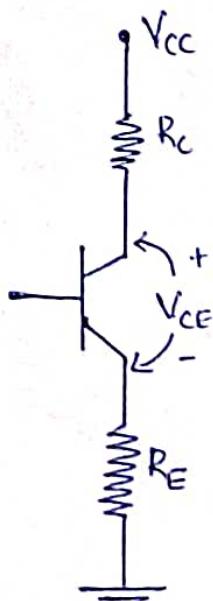
\* In fig (b), both collector & emitter resistors  $R_C$  &  $R_E$  are present, & the total dc load in series with the transistor is  $(R_C + R_E)$ .

\* Assuming  $I_E \approx I_c$ .

\* Applying KVL to collector-emitter circuit,

$$V_{CC} - I_c R_c - V_{CE} - I_c R_E = 0.$$

$$I_E \approx I_c$$



$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0.$$

$$V_{CC} - I_C [R_C + R_E] - V_{CE} = 0.$$

$$I_C [R_C + R_E] = V_{CC} - V_{CE} \rightarrow ②$$

$$I_C = \frac{V_{CC} - V_{CE}}{[R_C + R_E]}$$

$$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$I_C = \left[ -\frac{1}{R_C + R_E} \right] V_{CE} + \frac{V_{CC}}{R_C + R_E} \rightarrow ③$$

i) put  $I_C = 0$  in eq ②

$$V_{CE} = V_{CC} \rightarrow ④$$

ii) put  $V_{CE} = 0$  in eq ②.

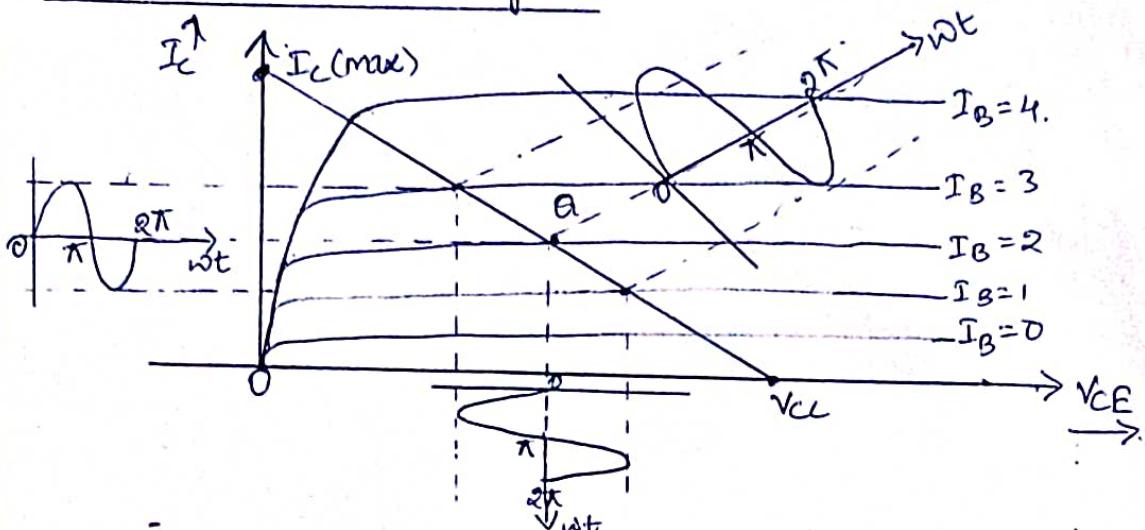
$$I_C = \frac{V_{CC}}{R_C + R_E} \rightarrow ⑤$$

eq ④ & ⑤ are the dc load line point.

### Selection of operating point :-

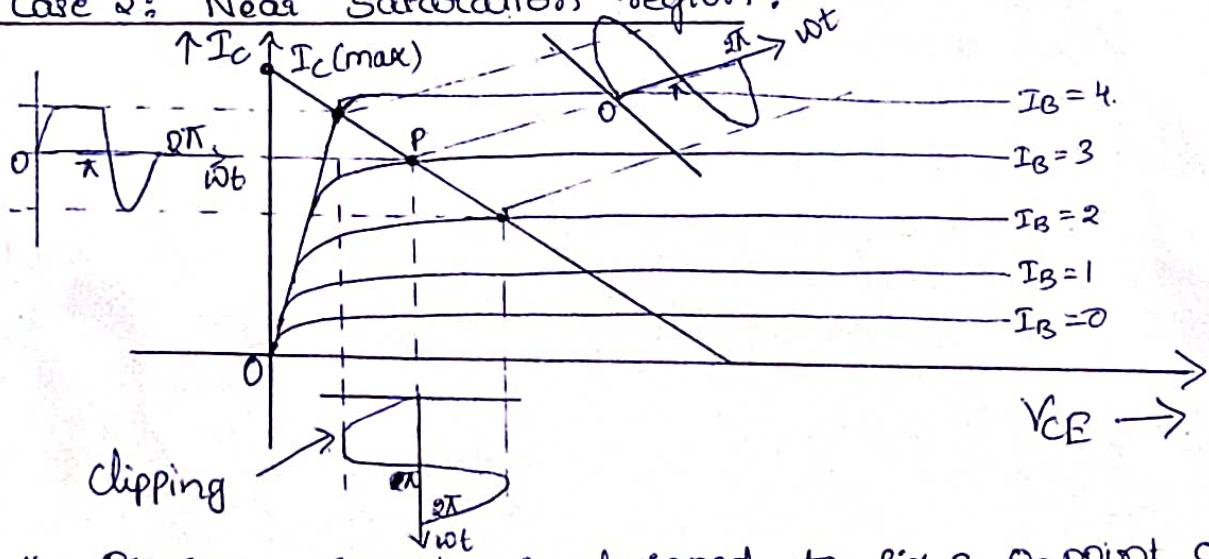
- \* The operating point can be selected at three different positions on the dc load line i.e.
  - 1) In Active region.
  - 2) Near Saturation region.
  - 3) Near cut-off region.

### Case 1: In Active region:-



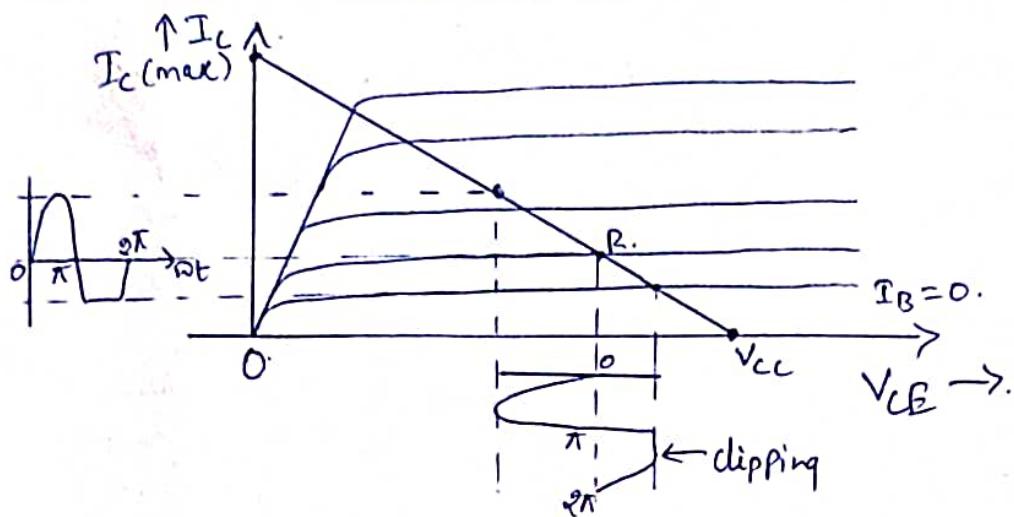
- \* Biasing circuit is designed to fix a Q-point at point 'Q' as shown in fig. i.e at the centre of active region. The o/p signal is Sinusoidal waveform without any distortion. Thus point Q is the best operating point.

### Case 2: Near Saturation region :-



- \* Biasing circuit is designed to fix a Q-point at point 'P' as shown in above figure. point 'P' is very near to the Saturation region.
- \* The o/p signal is clipped at the positive half cycle i.e. distortion is present at the o/p.
- ∴ point 'P' is not a suitable operating point.

case 3 : Near cut-off regions :-



- \* Biasing circuit is designed to fix a Q-point at point 'R' as shown in above figure. point 'R' is very near to the cut-off region.
- \* The o/p signal is clipped at the negative half cycle i.e distortion is present at the o/p.  
 $\therefore$  point 'R' is not a suitable operating point.

1) Draw the dc load line for the circuit in fig ①  $V_{cc} = +20V$

Apply KVL to collector emitter ckt

$$V_{cc} - I_c R_c - V_{ce} = 0.$$

$$V_{ce} = V_{cc} - I_c R_c \rightarrow ①$$

2) To find  $V_{ce}$ , put  $I_c = 0$  in eq ①

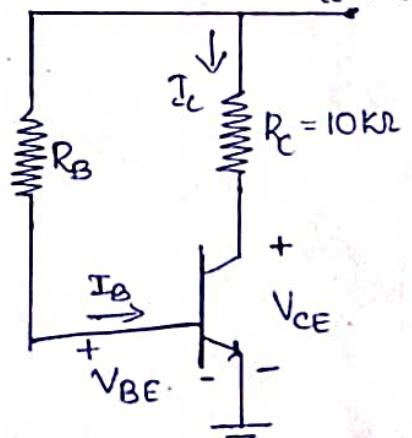
$$V_{ce} = V_{cc} - 0.$$

$$V_{ce} = 20V$$

3) To find  $I_c$ , put  $V_{ce} = 0$  in eq ①

$$0 = 20V - I_c (10k\Omega)$$

$$I_c (10k\Omega) = 20V$$



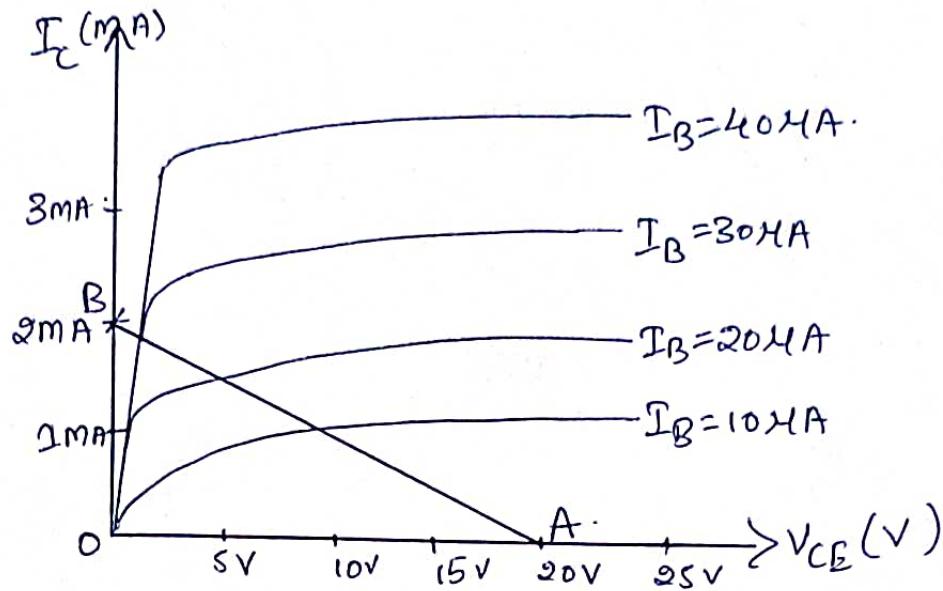
$$\text{i.e. } V_{ce} = V_c - I_c R_c$$

$$0 = V_{cc} - I_c R_c$$

$$I_c R_c = V_{cc}$$

$$I_c = V_{cc} / R_c$$

$$I_C = \frac{20V}{10k\Omega} = 2mA$$



DC Load line points :

- |                            |              |
|----------------------------|--------------|
| 1) $I_C = 0, V_{CE} = 20V$ | i.e Point A  |
| 2) $V_{CE} = 0, I_C = 2mA$ | i.e Point B. |

2. Draw the new dc load line for the circuit in fig ①  
when  $R_C = 12k\Omega$

WKT.  $V_{CE} = V_{CC} - I_C R_C \rightarrow ①$

- (1) put  $I_C = 0$  in eq ①,

$$V_{CE} = V_{CC}$$

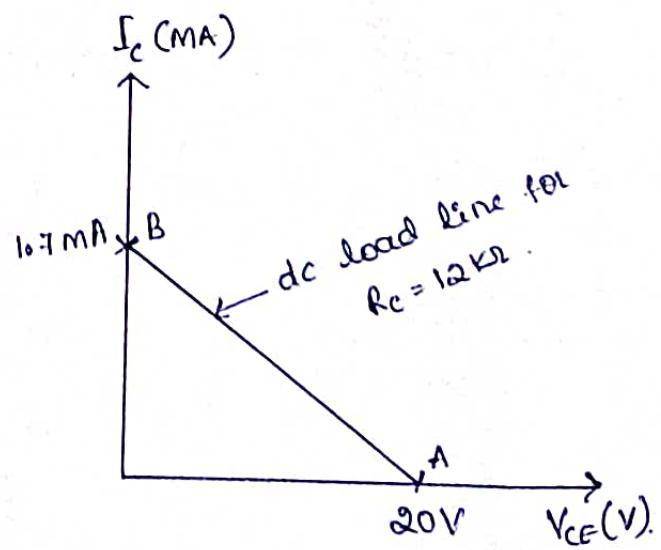
$$\boxed{V_{CE} = 20V}$$

- (2) put  $V_{CE} = 0$  in eq ①.

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{20V}{12k\Omega}$$

$$\boxed{I_C = 1.7 \text{ mA}}$$



3) The transistor circuit in fig ① has the collector characteristics as shown in fig ②. Determine the circuit Q-point & estimate the maximum symmetrical o/p voltage swing. Note that  $V_{CC} = 18V$ ,  $R_C = 2.2k\Omega$  &  $I_B = 40\mu A$ .

Sol:

Dc load line :-

$$\text{WKT } V_{CE} = V_{CC} - I_C R_C \quad ①$$

1) Put  $I_C = 0$  in eq ①

$$V_{CE} = V_{CC}$$

$$V_{CE} = 18V$$

point A.

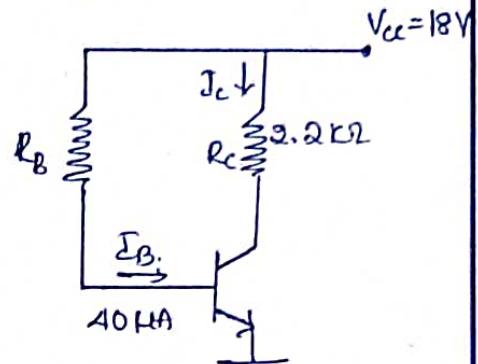


fig ①.

2) Put  $V_{CE} = 0$  in eq ①

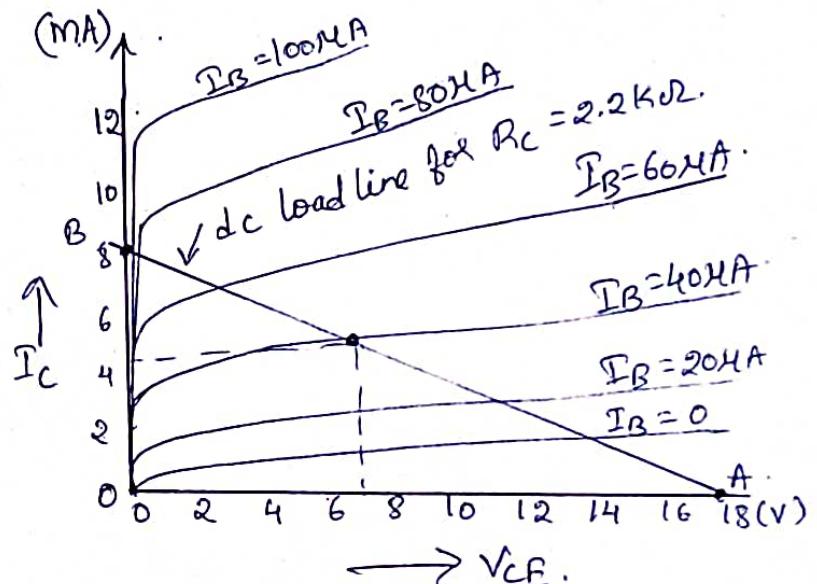
$$V_{CE} = V_{CC} - I_C R_C$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{18V}{2.2k\Omega}$$

$$I_C = 8.2\text{ mA}$$

point B.



\* Draw the dc load line through points A & B.

The Q-point is at the intersection of the load line & the  $I_B = 40\mu A$  characteristic.

\* the dc Bias conditions are

$$I_C \approx 4.1\text{ mA} \text{ & } V_{CE} \approx 9\text{ V}$$

\* The maximum symmetrical o/p voltage swing is

$$\Delta V_{CE} \approx +9\text{ V}$$

\* calculate  $\alpha_{dc}$  and  $\beta_{dc}$  for the transistor if  $I_c$  is measured as 1mA and  $I_B$  is 25μA. also determine the new base current to give  $I_c = 5\text{mA}$ .

[June - 08, 6M]

Given :- (i)  $I_c = 1\text{mA}$ ,  $I_B = 25\mu\text{A}$ ,  $\alpha_{dc} = ?$   $\beta_{dc} = ?$

(ii)  $I_c = 5\text{mA}$ ,  $I_B = ?$

Sol :-

$$\therefore * \beta_{dc} = \frac{I_c}{I_B} = \frac{1\text{mA}}{25\mu\text{A}} = 40.$$

$$* \alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{40}{1+40} = 0.9756.$$

ii) When  $I_c = 5\text{mA}$

$$* I_B = \frac{I_c}{\beta_{dc}} = \frac{5\text{mA}}{40} = 125\mu\text{A}.$$

\* calculate the values of  $I_c$ ,  $I_E$  and  $\beta_{dc}$  for a transistor with  $\alpha_{dc} = 0.98$  and  $I_B = 120\mu\text{A}$ .

[Jan - 09, 4M]

Given :  $\alpha_{dc} = 0.98$ ,  $I_B = 120\mu\text{A}$ ,  $I_c = ?$ ,  $I_E = ?$  &  $\beta_{dc} = ?$ .

Sol :

$$* \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} \approx 49$$

$$* I_c = \beta_{dc} I_B = 49 \times 120\mu\text{A} = 5.88\text{mA}.$$

\* Given  $I_E = 2.5\text{mA}$ ,  $\alpha = 0.98$  and  $I_{CEO} = 10\mu\text{A}$ , calculate  $I_B$  and  $I_c$

[Jan - 11, 4M]

Sol :-

WKT  $\alpha = \frac{I_c}{I_E}$ .

$$I_c = \alpha I_E = 0.98 \times 2.5\text{mA}$$

$I_c = 2.45\text{mA}$

$$NKT \quad I_E = I_B + I_C$$

$$I_B = I_E - I_C = 2.5 \text{ mA} - 2.45 \text{ mA}$$

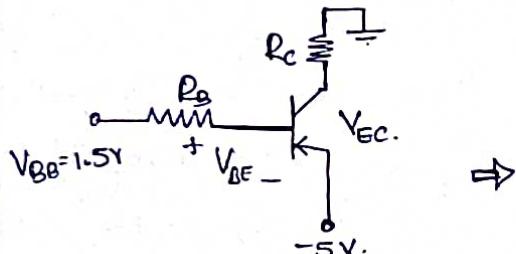
$$I_B = 50 \text{ nA}$$

- \* For the circuit shown below, the parameters are  $V_{BB} = 1.5 \text{ V}$ ,  $R_B = 580 \text{ k}\Omega$ ,  $V_{cc} = 5 \text{ V}$ ,  $V_{EB(\text{ON})} = 0.6 \text{ V}$  and  $\beta = 100$ . Find  $I_B$ ,  $I_c$ ,  $I_E$  and  $R_c$  such that  $V_{EC} = 1/2(V_{cc})$ .

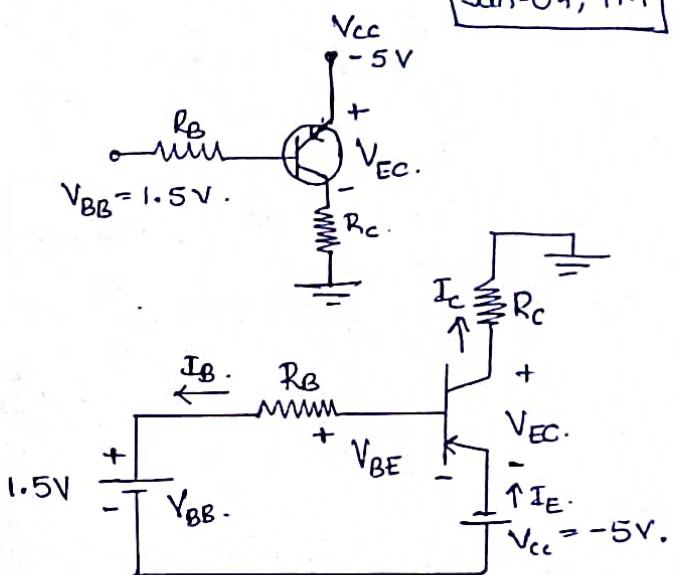
Given :-

$$V_{EC} = 2.5 \text{ V}$$

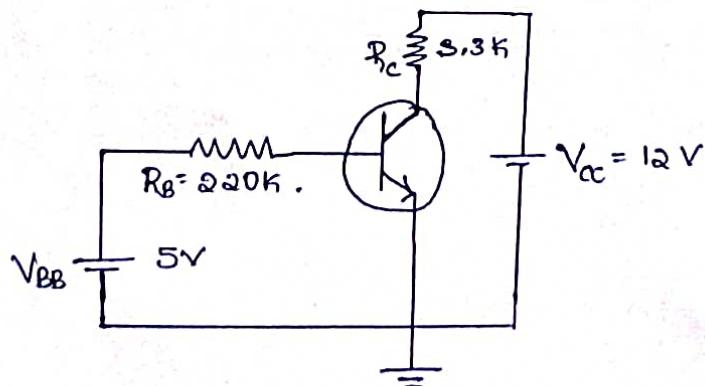
Sol:-



[Jan-07, 7M]



- \* Determine the transistor currents in the fig if  $\beta = 100$ .



[June -09, 8M]

Given:-  $V_{cc} = 12V$ ,  $V_{BB} = 5V$ ,  $R_B = 220k\Omega$ ,  $R_C = 3.3k\Omega$  &  $\beta = 100$

assuming  $V_{BE} = 0.7V$ .

Sol:-

Applying KVL to the Ip ckt.

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{220k\Omega}$$

$$I_B = 19.545 \text{ mA}$$

$$I_c = \beta I_B = 100 \times 19.545 \text{ mA}$$

$$I_c = 1.954 \text{ mA}$$

$$I_E = I_B + I_c = 19.545 \text{ mA} + 1.954 \text{ mA}$$

$$I_E = 1.974 \text{ mA}$$

Applying KVL from  $V_{cc}$ ,  $V_{BE}$  &  $V_{BB}$ .

$$-V_{cc} + V_{BE} - I_B R_B - V_{BB} = 0$$

$$-V_{cc} - V_{BB} + V_{BE} = I_B R_B$$

$$I_B = \frac{-V_{cc} - V_{BB} + V_{BE}}{R_B} = \frac{-5V - 1.5V + 0.6V}{580k\Omega} = \frac{-5.9V}{580k\Omega}$$

$$* I_B = -10.17 \text{ mA}$$

$$* I_c = \beta I_B = 100 \times 10.17 \text{ mA}$$

$$I_c = 1.017 \text{ mA}$$

$$* I_E = I_B + I_c = 10.17 \text{ mA} + 1.017 \text{ mA}$$

$$I_E = 1.027 \text{ mA}$$

\* Applying KVL from  $V_{CC}$ ,  $V_{EB}$  &  $R_C$ .

$$-V_{CC} + V_{EB} - I_C R_C = 0.$$

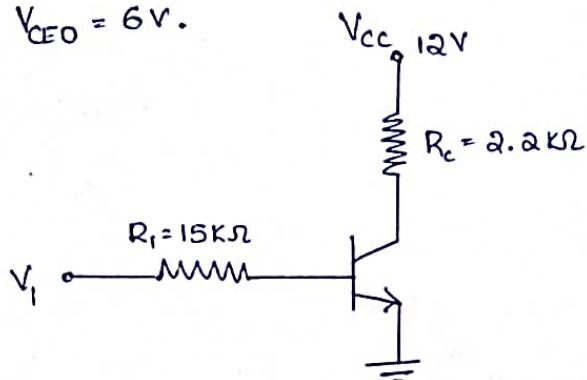
$$I_C R_C = -V_{CC} + V_{EB}$$

$$R_C = \frac{-V_{CC} + V_{EB}}{I_C} = \frac{-5V + 2.5V}{1.027 \text{ mA}}$$

$$R_C = 2.43 \text{ k}\Omega$$

\* For the transistor in fig  $\beta=30$ , determine  $V_i$  such that  $V_{CEO} = 6V$ .

June-07, 5M



Given :-  $V_{CC} = 12V$ ,  $R_i = 15 \text{ k}\Omega$ ,  $R_C = 2.2 \text{ k}\Omega$ ,  $V_{CE} = 6V$ ,  $\beta = 30$ .

Sol: Applying KVL to o/p ckt

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{12V - 6V}{2.2 \text{ k}\Omega}$$

\*  $I_C = 2.72 \text{ mA}$

\*  $I_B = \frac{I_C}{\beta} = \frac{2.72 \text{ mA}}{30}$

$I_B = 90.90 \text{ mA}$

Applying KVL to IIP ckt.

$$V_i - I_B R_B - V_{BE} = 0$$

$$V_i = I_B R_B + V_{BE} = (90.90 \mu A \times 15 k\Omega) + 0.7 V.$$

$$V_i = 2.06 V$$

- 1) calculate  $I_C$  &  $I_E$  for a transistor that has  $\alpha_{dc} = 0.98$  &  $I_B = 100 \mu A$ . Also determine the value of  $\beta_{dc}$  for the transistor. (Reference book).

Sol:

$$\star I_C = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B = \frac{0.98}{1 - 0.98} \times 100 \mu A = 4.9 mA$$

$$\star I_C = \alpha_{dc} I_E,$$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{4.9 mA}{0.98} = 5 mA$$

$$\star \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} = 49.$$

- 2) calculate  $\alpha_{dc}$  &  $\beta_{dc}$  for the transistor in fig ① if  $I_C$  is measured as 1mA, &  $I_B$  is 25  $\mu A$ . Also determine the new base current to give  $I_C = 5mA$ .

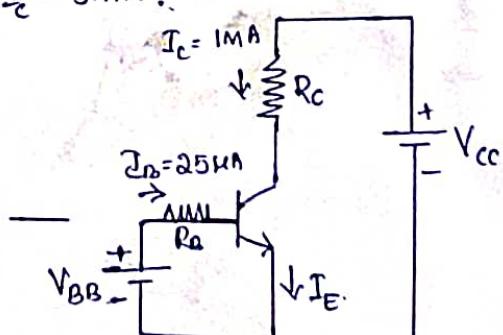
Sol:  $\star \beta_{dc} = \frac{I_C}{I_B} = \frac{1mA}{25 \mu A} = 40$

$$\star I_E = I_B + I_C = 1mA + 25 \mu A = 1.025 mA$$

$$\star \alpha_{dc} = \frac{I_C}{I_E} = \frac{1mA}{1.025 mA} = 0.976$$

$$\star \text{New base current to give } I_C = 5mA$$

$$I_B = I_C / \beta_{dc} = 5mA / 40 = 125 \mu A$$



(Reference book)

8) A transistor has  $I_B = 100 \mu A$  &  $I_c = 2mA$ , find

- i)  $\beta$  of the transistor.
- ii)  $\alpha$  of the transistor.
- iii) emitter current  $I_E$
- iv) If  $I_B$  changes by  $+25 \mu A$  &  $I_c$  changes by  $+0.6 mA$ .  
find the new value of  $\beta$ .

[July 06, 10 M]

Sol:- Given :  $I_B = 100 \mu A$  &  $I_c = 2mA$ ;

$$i) \beta = \frac{I_c}{I_B} = \frac{2mA}{100 \mu A} = \frac{2mA}{100 \mu A} = 20$$

$$ii) \alpha = \frac{\beta}{1+\beta} = \frac{20}{1+20} = 0.952$$

$$iii) I_E = I_B + I_c = 100 \mu A + 2mA = 2.1mA$$

$$iv) \text{New } I_B = 100 \mu A + 25 \mu A = 125 \mu A$$

$$\text{New } I_c = 2mA + 0.6mA = 2.6mA$$

$$\text{New } \beta = \frac{2.6mA}{125 \mu A} = 20.8$$

4. If  $\alpha$  for a transistor is 0.99, the base current is  $100 \mu A$ , estimate the collector current.

Sol: Given  $I_B = 100 \mu A$ ,  $\alpha = 0.99$

[March - 99, 5M]

$$\text{WKT. } \beta = \frac{I_c}{I_B} \quad \& \quad \beta = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{0.99}{1-0.99} = \underline{\underline{99}}$$

$$\begin{aligned} I_c &= \beta I_B \\ &= 99 \times 100 \mu A \end{aligned}$$

$$I_c = 9.9mA$$

$$* A_V = \frac{V_o}{V_i} = \frac{\pm 5.1 V}{\pm 50 mV} = \underline{\underline{102}}$$

\* The decrease in  $R_c$  reduces the voltage gain.

- (c) With change in transistor  $V_c = 9V$ , for  $V_{BE} = 0.7V$   
 $I_B = 30 \mu A$ .

$$V_o = V_{RC} = I_c R_c$$

$$\therefore \text{WKT. } V_c = V_{cc} - I_c R_c$$

$$\begin{aligned} I_c R_c &= V_{cc} - V_c \\ &= 25V - 9V \end{aligned}$$

$$I_c R_c = 16V$$

$$I_c = \frac{16V}{12k\Omega} = 1.33mA$$

$$* \beta_{dc} = \frac{I_c}{I_B} = \frac{1.33mA}{30\mu A}$$

$$\beta_{dc} = 44.33$$

## Input - Output characteristics of CB, CE & CC Configurations.

### Common Base Characteristics :- (NPN).

- \* Draw input and output characteristic of a transistor in common base configuration and explain in detail.

Jan 09, 8M

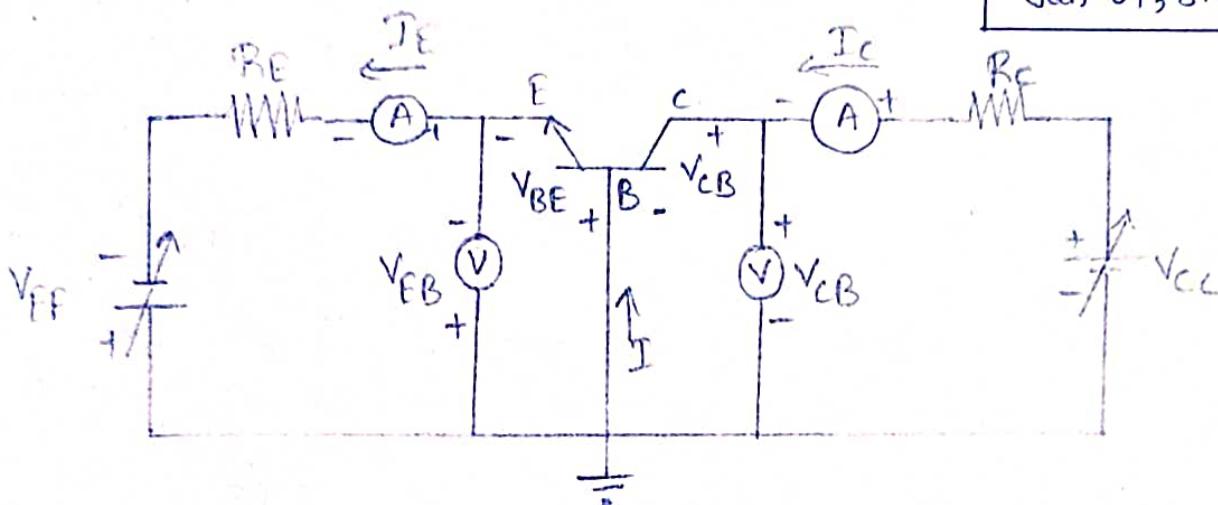


fig ① Common base configuration.

- { \* In fig ①, the emitter-base Junction (JE) is forward biased & the collector-base Junction (JC) is reverse biased.
- \* The emitter current  $I_E$  flows in the I/p ckt & the collector current  $I_C$  flows in the O/p ckt.
- q.

### I/p characteristics:-

- \* It is the curve between emitter current ' $I_E$ ' & emitter to base voltage ' $V_{EB}$ ' at constant collector-base voltage ' $V_{CB}$ '.
  - \* The emitter current is generally taken along Y-axis & emitter base voltage along X-axis as shown in fig ②.
- { 1) Keep O/p voltage  $V_{CB}$  to constant. .

3) Increase I<sub>IP</sub> voltage  $V_{EB}$  in small suitable steps.

3) Note down the corresponding I<sub>IP</sub> current ' $I_E$ '.

\* To obtain the I<sub>IP</sub> characteristic, the o/p voltage ' $V_{CB}$ ' is kept constant, I<sub>IP</sub> voltage ' $V_{EB}$ ' is varied in small intervals & the corresponding change in I<sub>IP</sub> current ' $I_E$ ' is recorded.

\*  $I_E$  is then plotted against  $V_{EB}$  as shown in fig ⑤. The experiment is repeated for other values of  $V_{CB}$  say 1V & 6V etc.

\* The emitter current ' $I_E$ ' increases rapidly with small increase in emitter-base voltage ' $V_{EB}$ '. It means the I<sub>IP</sub> resistance is very small.

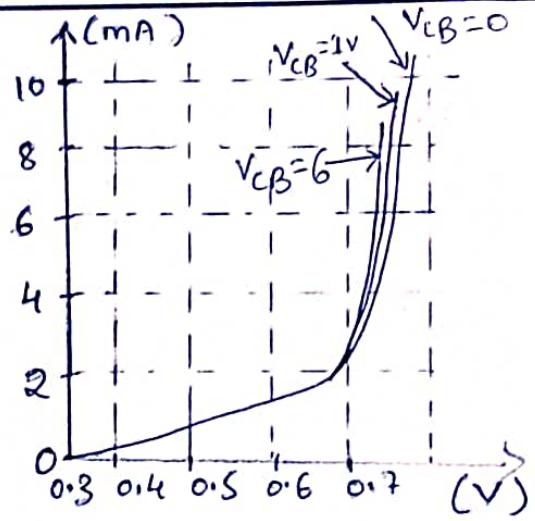
I<sub>IP</sub> resistance :- ( $R = \frac{V}{I}$ )

It is the ratio of change in emitter-base voltage  $\Delta V_{EB}$  to the resulting change in emitter current  $\Delta I_E$  at constant collector-base voltage  $V_{CB}$ .

i.e.

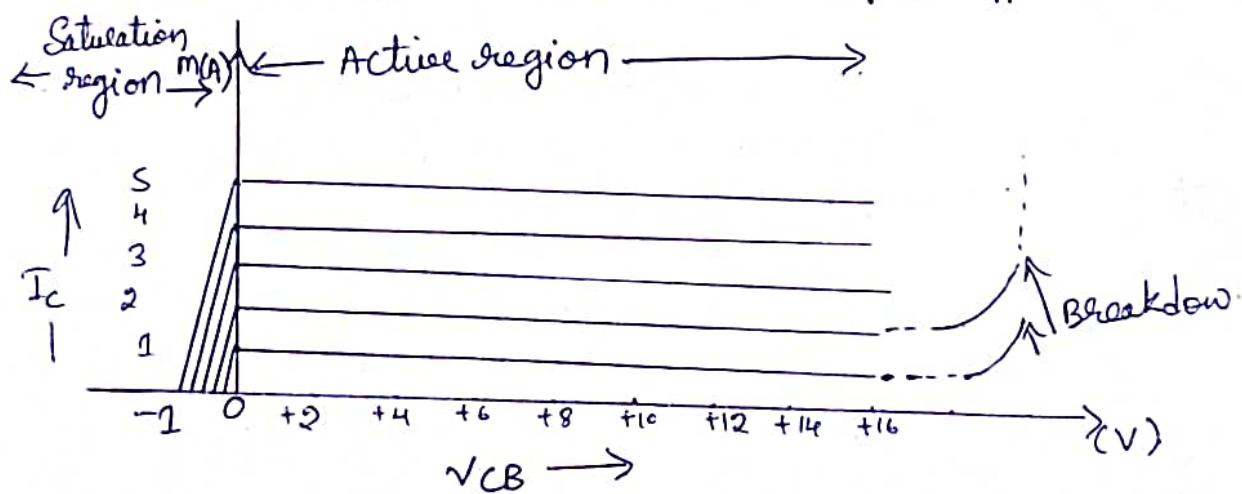
$$\boxed{\alpha_I = \left| \frac{\Delta V_{EB}}{\Delta I_E} \right| \text{constant } V_{CB}}$$

I<sub>IP</sub> resistance is quite small of the order of a few ohms.



## Olp characteristics :-

- \* These curves give the relationship between the collector current ' $I_c$ ' & the collector-base voltage ' $V_{CB}$ ' for a constant emitter current ' $I_E$ '.
- \* Collector current is taken along y-axis & collector voltage along x-axis.
- { \* we have to adjust the emitter-base voltage ' $V_{EB}$ ' to get a suitable value of emitter current ' $I_E$ ' (say  $I_E = 1\text{mA}, 2\text{mA}$  etc)
- \* The olp characteristic is obtained by keeping ' $I_E$ ' constant & by noting variation in collector current ' $I_c$ ' with variation in collector-base voltage ' $V_{CB}$ '.
- \* If we plot a graph with collector-base voltage ' $V_{CB}$ ' along with the horizontal axis & the collector current  $I_c$  along the vertical axis, which results fig (3) olp characteristics.



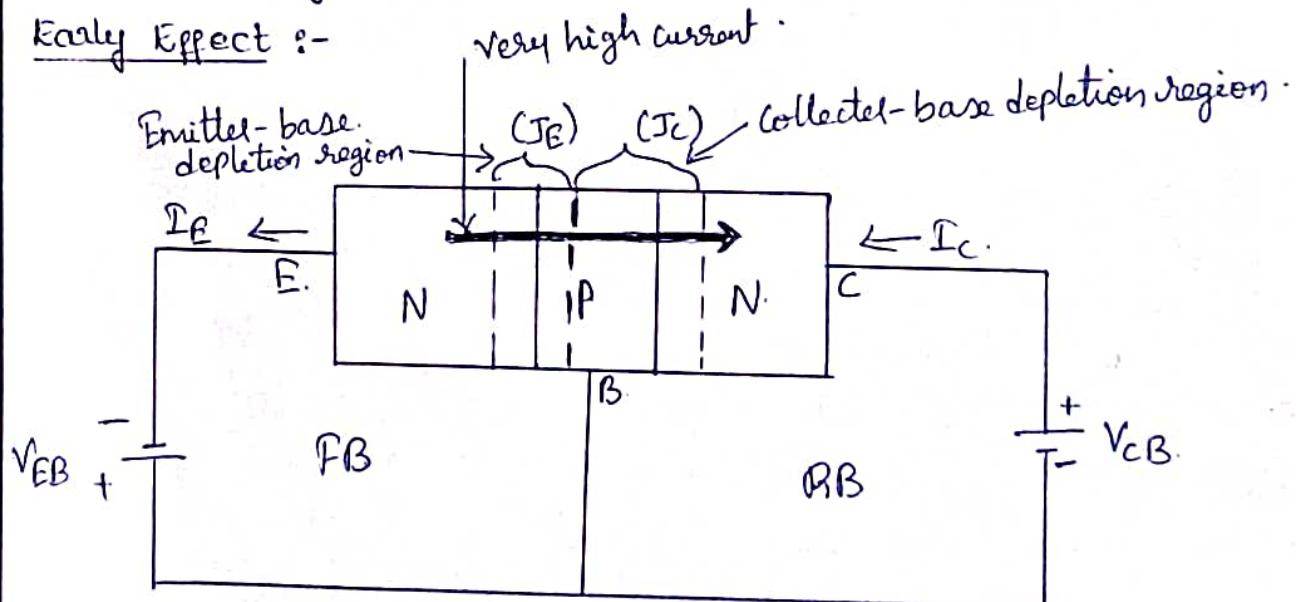
- \* OLP resistance ' $r_o$ ' is defined as the ratio of change in collector-base voltage ' $\Delta V_{CB}$ ' to the resulting change in collector current ' $I_c$ ' at constant emitter current ' $I_E$ '.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_c} / \text{constant } I_E.$$

- \* The O/P characteristic curve is divided into 3 regions namely,
  - (i) Saturation region
  - (ii) Active region
  - (iii) Cutoff region.

- i) In Saturation region, collector to base voltage ' $V_{CB}$ ' is -ve for a NPN transistor. It means that collector-base junction of a transistor is also forward biased in the saturation region. So a small change in  $V_{CB}$  results in a large value of ' $I_c$ ' current.
- ii) In active region, the emitter-base junction ' $J_E$ ' is forward biased & collector-base junction ' $J_C$ ' is reverse biased. The collector current is constant & is equal to the emitter current. ( $I_c \approx I_e$ ).
- iii) In cut-off region, both junctions of a transistor are reverse biased, hence only a small leakage current flows in the circuit.

Punch-Through effect or Base-width Modulation or Early Effect :-



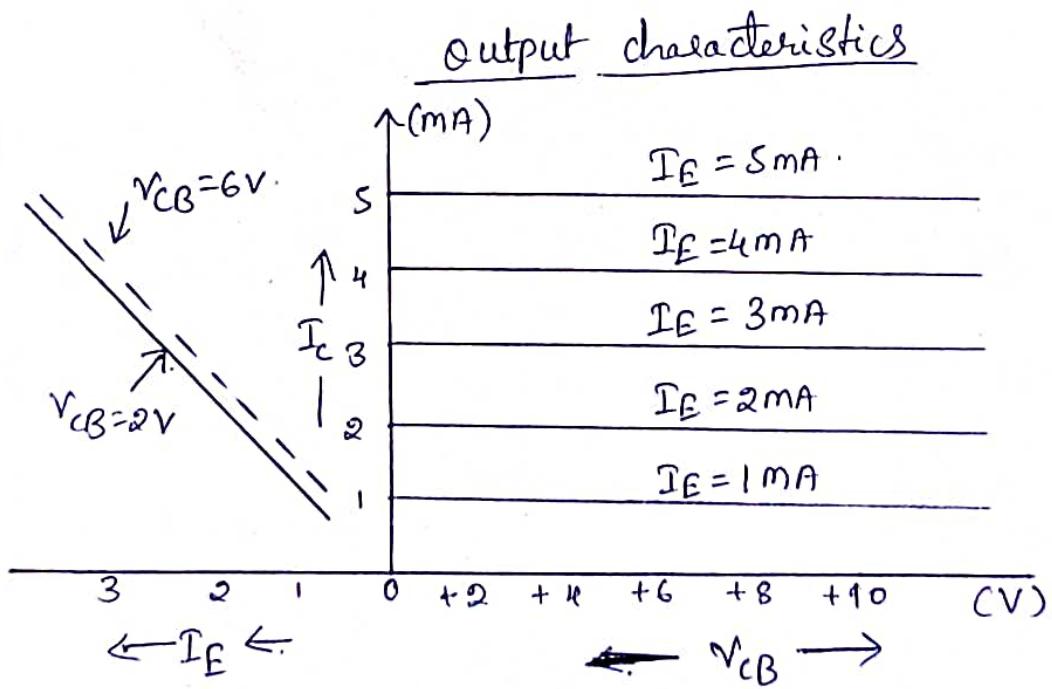
fig(4): Illustration of Punch through.

- \* When the reverse bias voltage  $V_{CB}$  in the C-B configuration exceeds the maximum values specified by the manufacturer, the collector-base depletion region may penetrate deep into the base until it comes into contact with the emitter-base-depletion region. This condition is called punch through & is shown in fig ①.
- \* This leads to the breakdown of the device & very large currents flow through the device (transistor). The excessive flow of current will damage the transistor.
- \* Maximum values of  $V_{CB}$  range b/w 25V & 80V.

### Current Gain :-

- \* The current gain characteristic is also called as forward transfer characteristic.
- \* It is a plot of the output current ' $I_C$ ' against variations in input current ' $I_E$ ' when  $V_{CB}$  is held constant.

fig:-



## Common Emitter Characteristics :- (NPN)

- \* Draw the input and output characteristic of CE circuit. Explain active, saturation, cut-off region.

June 10, 8M	Jan - 03, 9M	Jan - 04, 9M	June 04, 6M
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- \* Draw the common emitter circuit. Draw the input & output curves and explain the terms active region, cutoff region and saturation region.

June - 09, 8M	June 08, 8M	Jan 08, 7M	June 06, 5M	June 05, 7M
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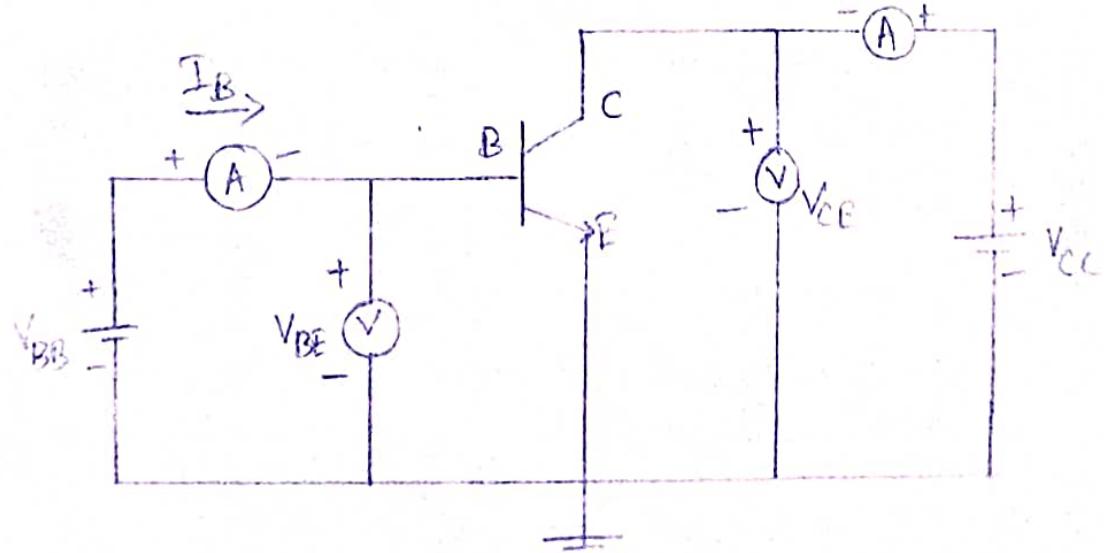
- \* Draw the input and output characteristic curve of a transistor in common-emitter configuration. Explain their nature and shape. What do their slope represents?

Jan - 07, 7M
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- \* Explain the input and output characteristics for a CE configuration BJT circuit. Discuss each region on the characteristics.

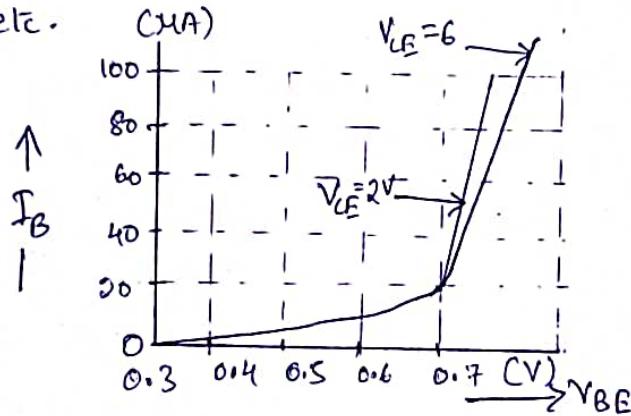
$I_C$

Jan - 11, 6M (OLD)
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fig① : circuit for determining transistor common emitter characteristics.

- \* These curves give the relationship b/w the base current  $I_B$  & the base emitter voltage  $V_{BE}$  for a constant collector emitter voltage  $V_{CE}$ .
- \* To obtain  $I_{IP}$  characteristic, the o/p voltage ' $V_{CE}$ ' is kept constant,  $I_{IP}$  voltage ' $V_{BE}$ ' is varied in small intervals & the corresponding change in  $I_{IP}$  current ' $I_B$ ' is recorded.
- \*  $I_B$  is then plotted against  $V_{BE}$  as shown in fig②. The experiment is repeated for other values of ' $V_{CE}$ ' say 2V, 6V, ... etc.



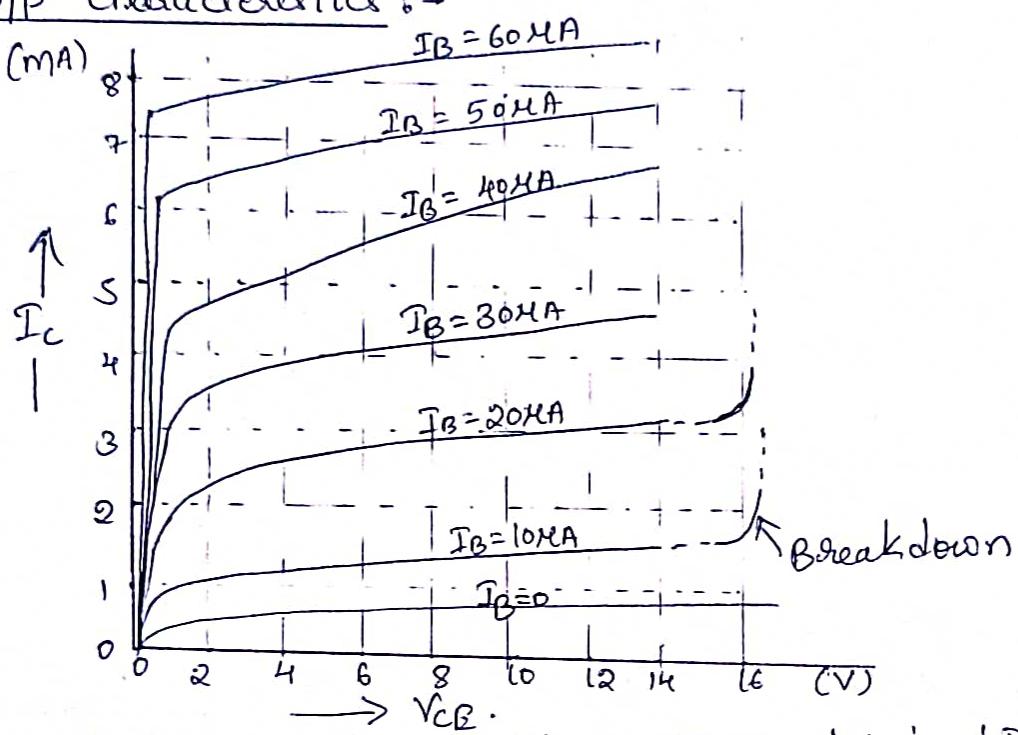
- \*  $I_{IP}$  resistance is defined as the ratio of change in base-emitter voltage ' $\Delta V_{BE}$ ' to the resulting change in base-current ' $\Delta I_B$ ' at constant collector emitter voltage.

$$R_I = \frac{\Delta V_{BE}}{\Delta I_B} \quad |_{V_{CE} \text{ constant}} \quad (600\Omega \text{ to } 400\Omega)$$

- \* fig ② shows that, for a given level of  $V_{BE}$ ,  $I_B$  is reduced when higher  $V_{CE}$  levels are employed. This is because higher ' $V_{CE}$ ' produces greater depletion region penetration into the base, reducing the distance b/w the CB & EB depletion regions.

- \* Thus more of the charge carriers from the emitter flow across the CB-Junction & less current flow from base terminal.

O/P characteristics :-



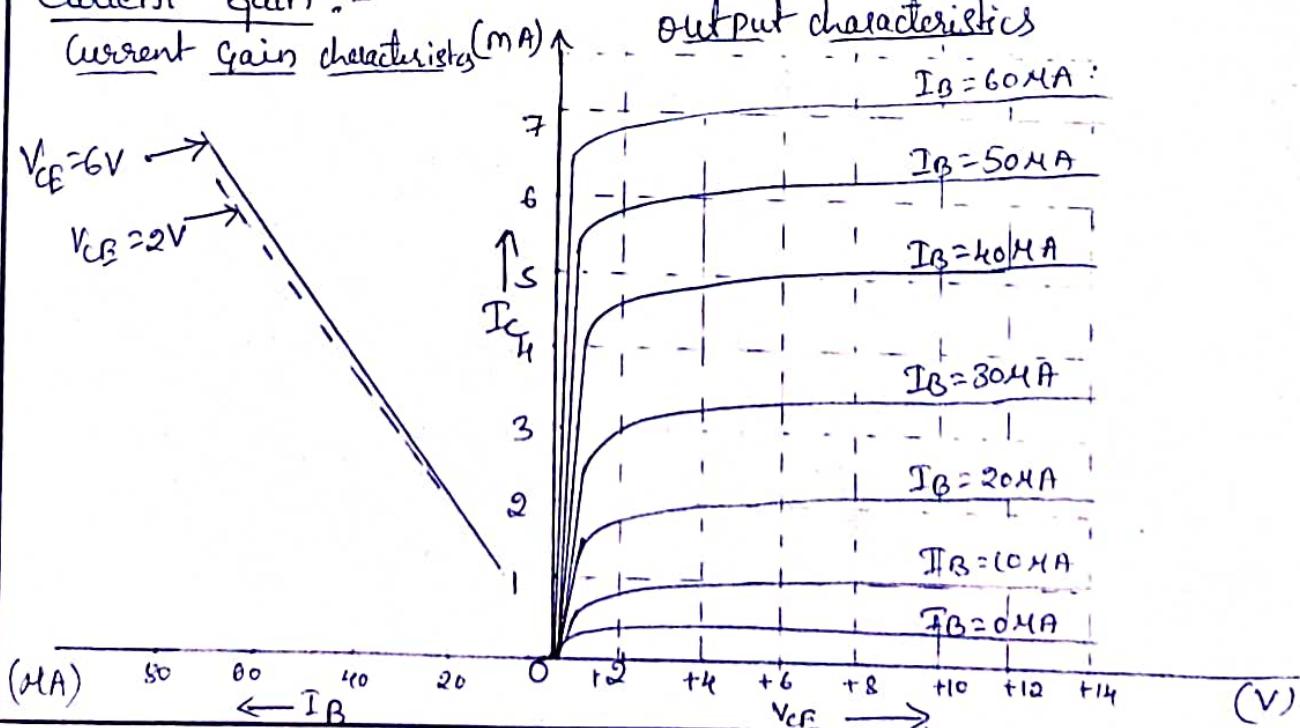
- \* By using base-emitter voltage ' $V_{BE}$ ', ' $I_B$ ' is maintained constant at several convenient levels.
- \* ' $V_{CE}$ ' is varied in suitable steps & at each step  $I_c$  value is recorded. The same procedure is repeated for different settings of  $I_B$ .
- \* If we plot a graph with ' $V_{CE}$ ' voltage along horizontal axis & the collector current ' $I_c$ ' along the vertical axis, we shall obtain a o/p characteristic as shown in fig ③.
- \* O/p resistance ' $r_o$ ' is defined as the ratio of change in collector to emitter voltage ' $\Delta V_{CE}$ ' to the resulting change in collector current ' $\Delta I_c$ ' at constant base current ' $I_B$ '.

$$r_o = \left| \frac{\Delta V_{CE}}{\Delta I_c} \right| \text{ constant } I_B$$

(10kΩ to 50kΩ)

- \* The o/p characteristics curve is divided into 3 regions namely:
  - i) Saturation region.
  - ii) Active region.
  - iii) cut-off region.
- i) In saturation region, when the collector to emitter voltage ' $V_{CE}$ ' is increased above zero, the collector current ' $I_c$ ' increases rapidly to a saturation value, depending upon the value of base current.
- \* It may be noted that collector current  $I_c$  reaches to a Saturation value when  $V_{CE}$  is about 0.5 V.
- i) In active region, the collector current is  $P_{de}$  times greater than the base current. Thus small I<sub>B</sub> current ' $I_B$ ' produces a large o/p current  $I_c$ .
- iii) In cutoff region, when base current is zero ( $I_B=0$ ), collector current is not zero ( $I_c \neq 0$ ), a small collector current exists called reverse leakage current ' $I_{CEO}$ '.

Current Gain :-



- \* Common emitter current gain characteristic shows the variation of  $I_c$  as a function of  $I_B$  with constant ' $V_{CE}$ ' i.e ' $V_{CE}$ ' is held at a convenient level &  $I_B$  is varied in suitable steps and at each step  $I_c$  value is recorded.  $I_c$  is then plotted as a function of  $I_B$ .
- \* A vertical line is drawn through a selected  $V_{CE}$  value & the corresponding levels of  $I_c$  &  $I_B$  are read along the line.

## Common Collector characteristics :- (NPN)

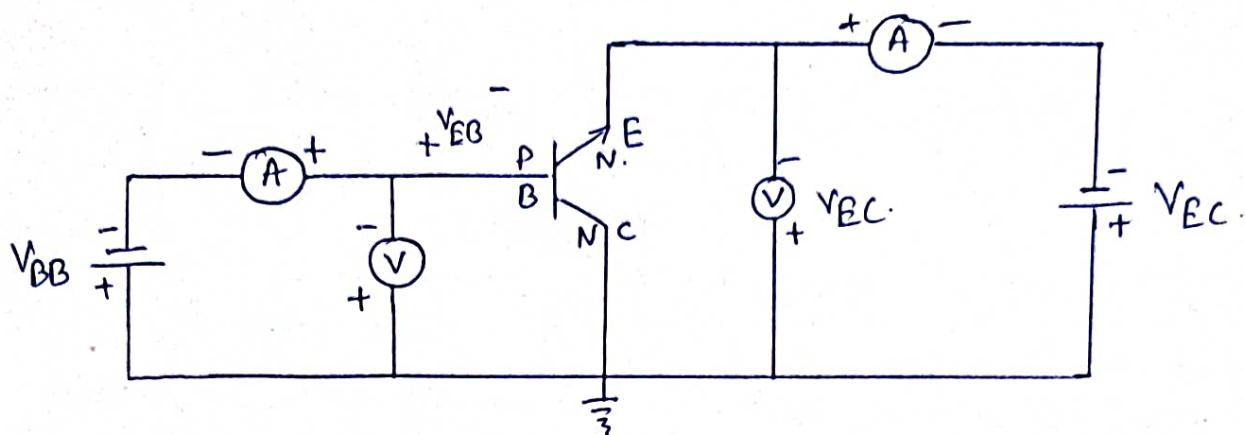


fig ①: circuit for obtaining common-collector characteristics.

### I<sub>B</sub>P characteristic:-

- \* In common-collector circuit, collector terminal is common to both I<sub>B</sub>P & O<sub>B</sub>P terminal.
- \* Common collector I<sub>B</sub>P characteristic shows the variation of  $I_B$  with  $V_{BC}$  at a constant  $V_{EC}$ .
- \*  $V_{EC}$  is set to a convenient value.  $V_{BC}$  is varied in suitable steps and at each step  $I_B$  value is recorded.
- \*  $I_B$  is then plotted against  $V_{BC}$  as shown in fig ②. The experiment is repeated for other values of ' $V_{EC}$ ' say 3V, 6V etc

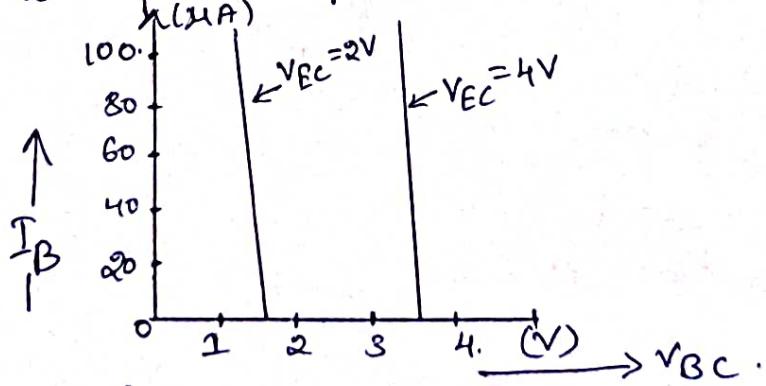


fig ②: I<sub>B</sub>P characteristic.

- \* fig ② shows the common collector I<sub>B</sub>P characteristics. This is quite different from either CB or CE I<sub>B</sub>P characteristics. The difference is due to the fact that the I<sub>B</sub>P voltage  $V_{BC}$ , is largely determined by the  $V_{EC}$  level.

Applying KVL from emitter to base ckt.

$$-V_{EC} + V_{EB} + V_{BC} = 0.$$

$$V_{BC} = V_{EC} - V_{EB} \rightarrow \textcircled{1}$$

$$\& V_{EB} = V_{EC} - V_{BC} \rightarrow \textcircled{2}$$

- \* At a constant  $V_{EC}$ , if  $V_{EC}$  is increased,  $V_{EB}$  reduces and as a result  $I_B$  decreases.

O/P characteristics :-

current gain characteristics (mA)

output characteristics

$$I_B = 60 \mu A$$

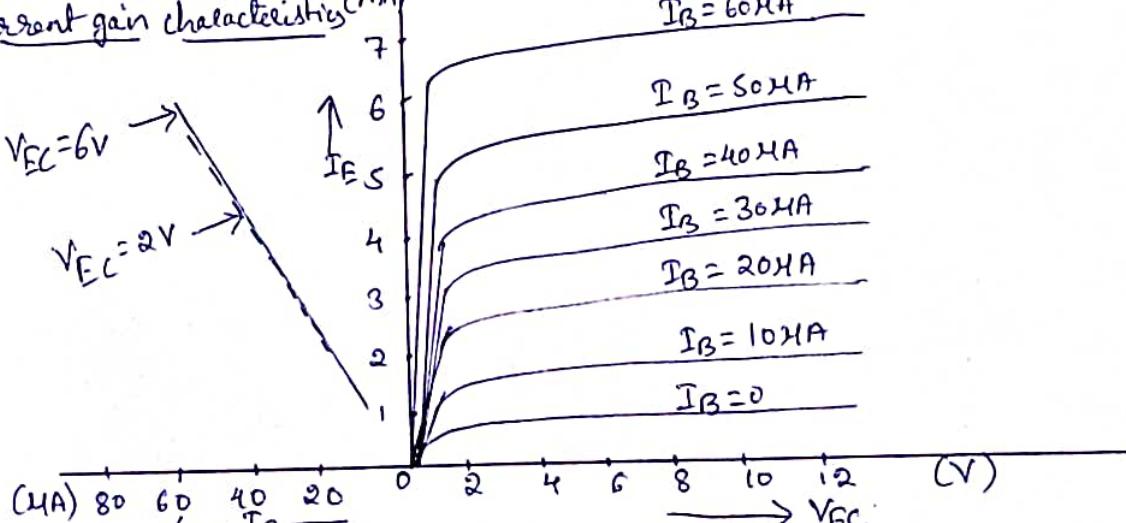


fig ③ : O/P characteristics.

- \* common-collector o/p characteristic shows the variation of  $I_E$  as a function of  $V_{EC}$  at a constant  $I_B$ .
- \*  $I_B$  is set to a convenient value,  $V_{EC}$  is varied in suitable steps and at each step  $I_E$  value is recorded. The same procedure is repeated for different settings of  $I_B$ .
- \* The common collector current gain characteristics are  $I_E$  plotted versus  $I_B$  for several fixed values of  $V_{CE}$ .
- \* The  $I_C$  is approximately equal to  $I_E$ , the common collector o/p characteristics & current gain characteristics are practically identical to those of the common-emitter circuit.

## Comparison of Transistor configurations:-

- \* Compare various BJT circuit configurations.

Jan 11, 4M (OLD)

Sl. No	Characteristic	Common Base	Common Emitter	Common Collector
1	Input Resistance	Very low ( $R_{in}$ )	Low ( $1k\Omega$ )	High ( $500k\Omega$ )
2	Output Resistance	Very high ( $1M\Omega$ )	High ( $40k\Omega$ )	Low ( $50\Omega$ )
3	Input current	$I_E$	$I_B$	$I_B$
4	Output current	$I_C$	$I_C$	$I_E$
5	Input voltage applied between	Emitter and Base	Base and Emitter	Base and collector
6	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and collector
7	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
8	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9	Voltage gain	Medium	Medium	Less than unity
10	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance Matching

## Introduction:

- A transistor is a semiconductor device that controls current with the application of a small electrical signal.
- Transistors may be roughly grouped into two major families: bipolar and field-effect. BJT utilize a small current to control a large current. But, FET utilizing a small voltage to control current.
- FETs are unipolar rather than bipolar devices. That is, the main current through them is comprised either of electrons through an N-type semiconductor (N-channel FET) or holes through a P-type semiconductor (P-channel FET).
- In a JFET, the controlled current passes from Source to Drain, or from Drain to Source as the case may be. The controlling voltage is applied between the Gate and Source. Current flowing through this channel widely depends on the input voltage applied to its Gate terminal.
- FETs generally of two types: 1) JFET (Junction Field Effect Transistors) and 2) MOSFET (Metal Oxide Semiconductor Field Effect Transistors).

**Junction Field Effect Transistors:** JFET is a voltage controlled three terminal uni-polar semiconductor device. The three terminals namely, Source (S), Gate (G) and Drain (D).

As the voltage applied to the Gate with respect to the Source ( $V_{GS}$ ), controls the current flowing between the Drain and the Source terminals. See fig.2.1. JFETs can be classified into two types (i) n-channel JFET and (ii) p-channel JFET, depending on whether the current flow is due to electrons or holes, respectively.

## Components of FET:

1. **Channel:** This is the area in which majority charge carriers flow. When the majority charge carriers are entered in FET, then with the help of this channel only they flow from source to drain.
2. **Source:** Source is the terminal through which the majority charge carriers are introduced in the FET.
3. **Drain:** Drain is the collecting terminal in which the majority charge carriers enter and thus contribute in the conduction procedure.

**4. Gate:** Gate terminal is formed by diffusion of a type of semiconductor with another type of semiconductor. It basically creates high impurity region which controls the flow of carrier from source to drain.

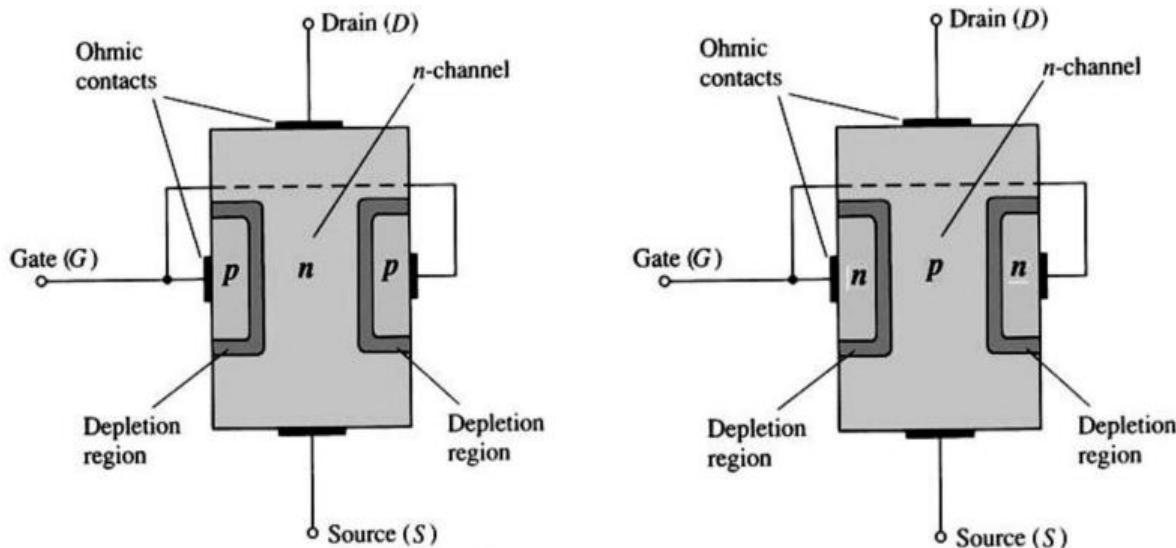


Fig 2.1: Constructional details of a) N-channel JFET b) P-channel JFET

### Working of N-channel JFET:

#### Case I: No voltage is applied to the device ( $V_{DS} = 0$ and $V_{GS} = 0$ ).

At this state, the device will be idle and no current flows through it ( $I_{DS} = 0$ ).

#### Case-II: When $V_{DS}$ is applied and $V_{GS} = 0$

As shown in fig.2.2 (a), the two PN junctions at the sides of the N channel establish depletion layers. The electrons will flow from Source to Drain through a channel between the depletion layers. The size of the depletion layers determines the width of the channel and hence current  $I_{DS}$ , conduction through the bar.

#### Case-III: When $V_{DS}$ is applied and $V_{GS} = -ve$

The depletion region width increases, which results in reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from Source to Drain is decreased.

If more ( $-V_{GS}$ ) is applied, further reduces the channel width until no current flows through the channel. At this - voltage at which the JFET channel is called as pinched-off voltage,  $V_P$ .

At this state, the  $I_{DS}$  current is restricted only by the channel-resistance. However, once the pinch-off occurs ( $V_{DS} = V_P$ ), the current  $I_{DS}$  saturates at a particular level  $I_{DSS}$ .

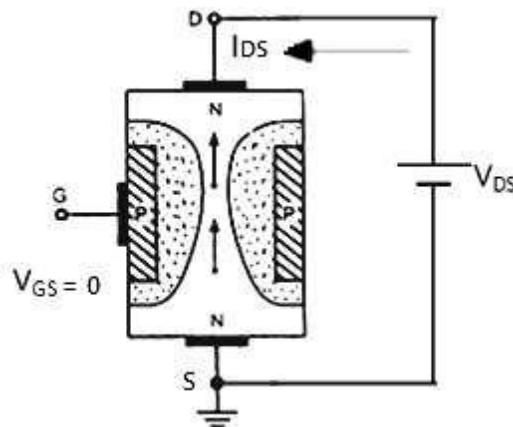


Fig 2.2 (a)

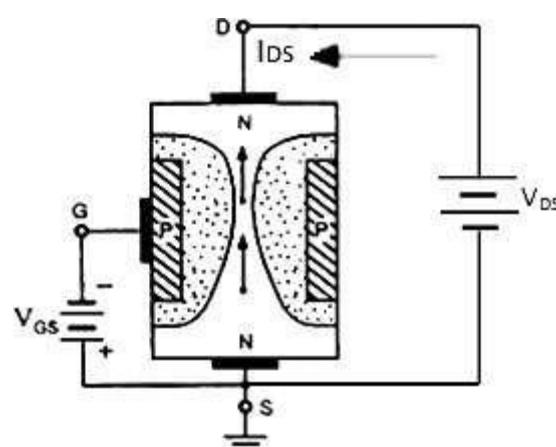


Fig 2.2 (b)

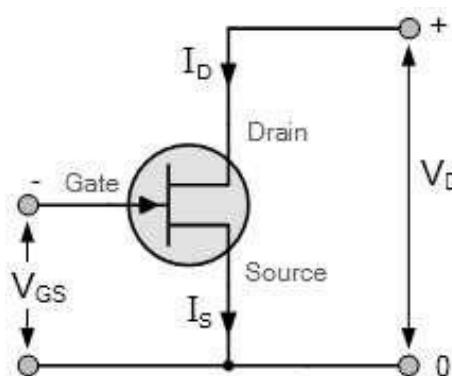


Fig 2.3: Circuit diagram of N-channel JFET

### Output characteristics (Drain) V-I curves of JFET:

The characteristics curves of a JFET shown in the fig.2.4, reveals four different regions of operation are given as:

- **Ohmic Region:** When  $V_{GS} = 0$  the depletion region of the channel is very small and the JFET acts like a voltage controlled resistor.
- **Cut-off Region:** This is also known as the pinch-off region where the Gate voltage,  $V_{GS}$  is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- **Saturation or Active Region:** The JFET becomes a good conductor and is controlled by the Gate-Source voltage, ( $V_{GS}$ ) while the Drain-Source voltage, ( $V_{DS}$ ) has little or no effect.
- **Breakdown Region:** The voltage between the Drain and the Source, ( $V_{DS}$ ) is high enough to cause the JFET's resistive channel to breakdown and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current  $I_D$  decreases with an increasing positive Gate-Source voltage,  $V_{GS}$ .

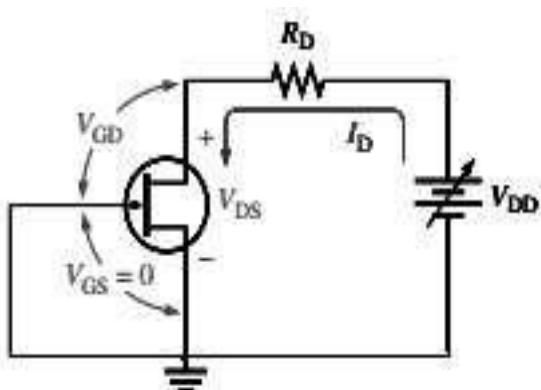
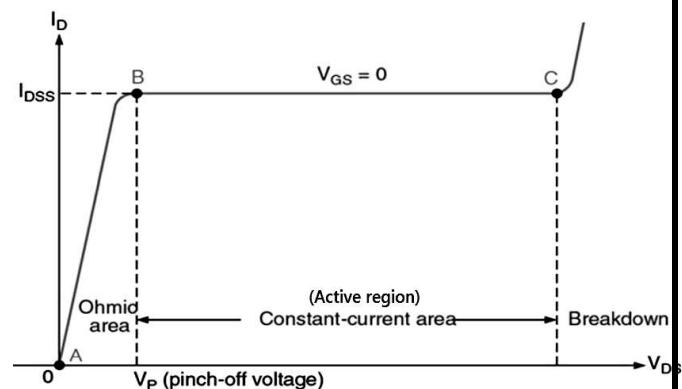


Fig 2.4 (a) JFET with  $V_{GS}=0V$  and a variable  $V_{DS}(V_{DD})$



(b) The drain Characteristics curve for  $V_{GS}=0$  showing pinch off voltage

The Drain current  $I_{DS}$  is zero when  $V_{GS} = V_P$ . For normal operation,  $V_{GS}$  is biased to be somewhere between  $V_P$  and 0. Then we can calculate the Drain current,  $I_D$  for any given bias point in the saturation or active region as follows:

### **1. Drain current in the Active region:**

Drain current ( $I_D$ ) at the active region can be calculated as follows:  $I_D$  lies between (pinch-off) zero to  $I_{DSS}$ .

$$I_D = I_{DSS} \left( 1 - \frac{v_{GS}}{V_P} \right)^2$$

### **2. Drain-Source Channel Resistance $R_{DS}$ :**

Similarly, if we know drain source voltage  $V_{DS}$  and drain current  $I_D$ , we can calculate the drain-source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where:  $g_m$  is the “trans conductance gain” since the JFET is a voltage controlled device and which represents the rate of change of the  $I_D$  with respect to the change in  $V_{GS}$ .

### **3. Amplification Factor: ( $\mu$ )**

It is given by

$$\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}} \text{ at } I_D \text{ constant}$$

### Transfer characteristics of JFET:

The transfer characteristics can be determined by observing different values of  $I_D$  with variation in  $V_{GS}$  provided that the  $V_{DS}$  should be constant as shown in the fig.2.5.

Notice that the bottom end of the transfer characteristic curve is at a point on the  $V_{GS}$  axis equal to  $V_{GS}(\text{off})$ , and the top end of the curve is at a point on the  $I_D$  axis equal to  $I_{DSS}$ .

This curve shows that

- i)  $I_D = 0$ ; when  $V_{GS} = V_{GS}(\text{off})$
- ii)  $I_D = I_{DSS}$  when  $V_{GS} = 0$
- iii) The transfer characteristic curve is expressed approximately as

$$I_D \approx I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

Hence, JFETs are often referred to as square-law devices.

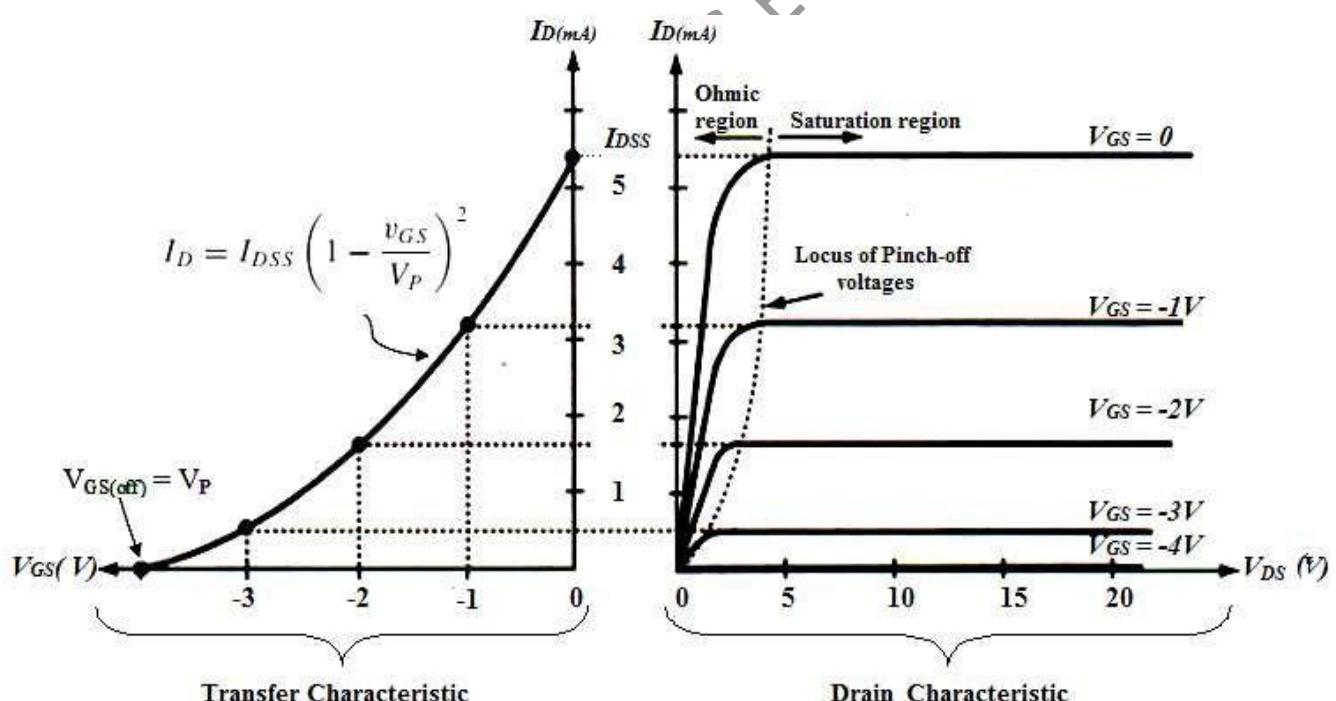


Fig 2.5 Transfer and Drain characteristics

### Comparison of BJT and FET:

BJT	JFET
Bipolar junction transistor	Unipolar junction transistor
Input impedance is very less	Input impedance is very large
Current control device, preferred for low current applications	Voltage controlled device, preferred for low voltage applications
More noisy	Less noisy
Frequency variations effect its performance	High frequency response
Temperature dependent device	Better heat stability
Cheaper than FET	Costly than BJT
Bigger in size than FET	Smaller in size than BJT
More gain	Less gain
High output impedance because of high gain	Low output impedance because of less gain
High voltage gain	Low voltage gain
Low current gain	High current gain
Switching time is medium	Switching time is fast
Consumes more power	Consumes less power

### Metal Oxide Semiconductor Field Effect transistor (MOSFET):

- The MOSFET, different from the JFET, has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide ( $\text{SiO}_2$ ) layer shown in the fig.2.6.

- The MOSFET is widely used for switching and amplifying electronic signals. Also, it is a core of ICs and it can be designed and fabricated in a single chip because of smaller silicon chip area.

The two basic types of MOSFETs

- Enhancement MOSFET (E-MOSFET) and
- Depletion MOSFET (D-MOSFET). Of the two types, the enhancement MOSFET is more widely used.

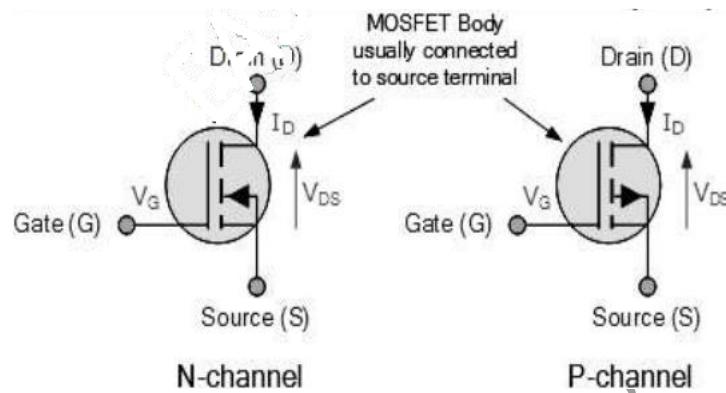


Fig.2.6 MOSFET circuit symbols

The depletion mode MOSFETs are generally ON at ( $V_{GS} = 0V$ ). The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs. See fig. 2.7.

**Case I:** When there is no Gate voltage ( $V_{GS} = 0$ ), as in fig. 2.7, maximum current flows ( $I_D = I_S = I_{DSS}$ ).

**Case II:** When  $V_{GS} = -ve$  with respect to the substrate, the Gate repels some of the electrons out of the N-channel.

This creates a *depletion region* in the channel, as illustrated in fig.2.8, and, therefore, increases the channel resistance and reduces the Drain current,  $I_D$ . The more negative the gate, the less the Drain current.

In this mode of operation, the device is referred to as a *depletion-mode MOSFET*. Heretoo much negative Gate voltage can pinch-off the channel. Then device is said to be OFF.

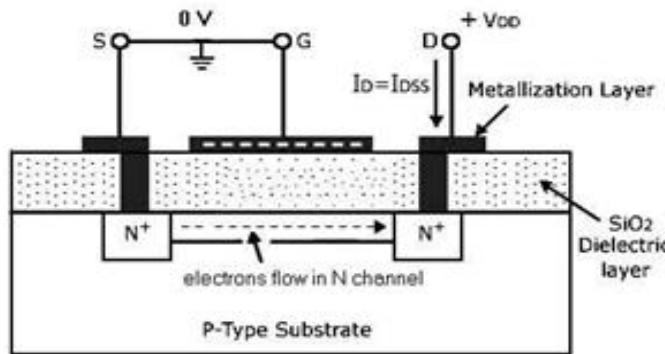


Fig.2.7 MOSFET in depletion mode with gate voltage zero

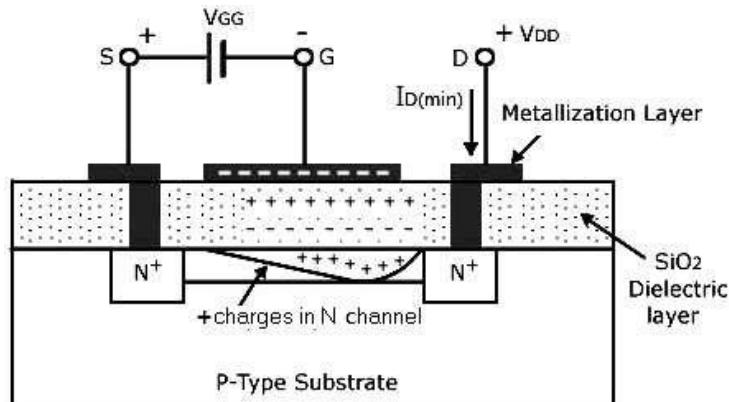


Fig.2.8 MOSFET in depletion mode with gate voltage negative

**Case III:** When  $V_{GS} = +ve$ , Gate attracts the negative charge carriers from the P-substrate to the N- channel and thus reduces the channel resistance and increases the drain current,  $I_D$ . The more positive the Gate is made, the more Drain current flows. In this mode of operation, the device is referred to as an enhancement-mode MOSFET. This is depicted in the fig. 2.9.

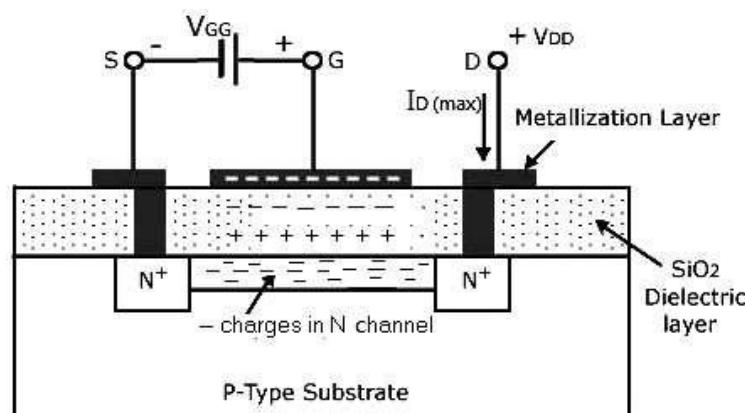


Fig.2.9 MOSFET in depletion mode with gate voltage positive

Transfer and Drain characteristic of depletion MOSFET is shown in the fig.2.10.

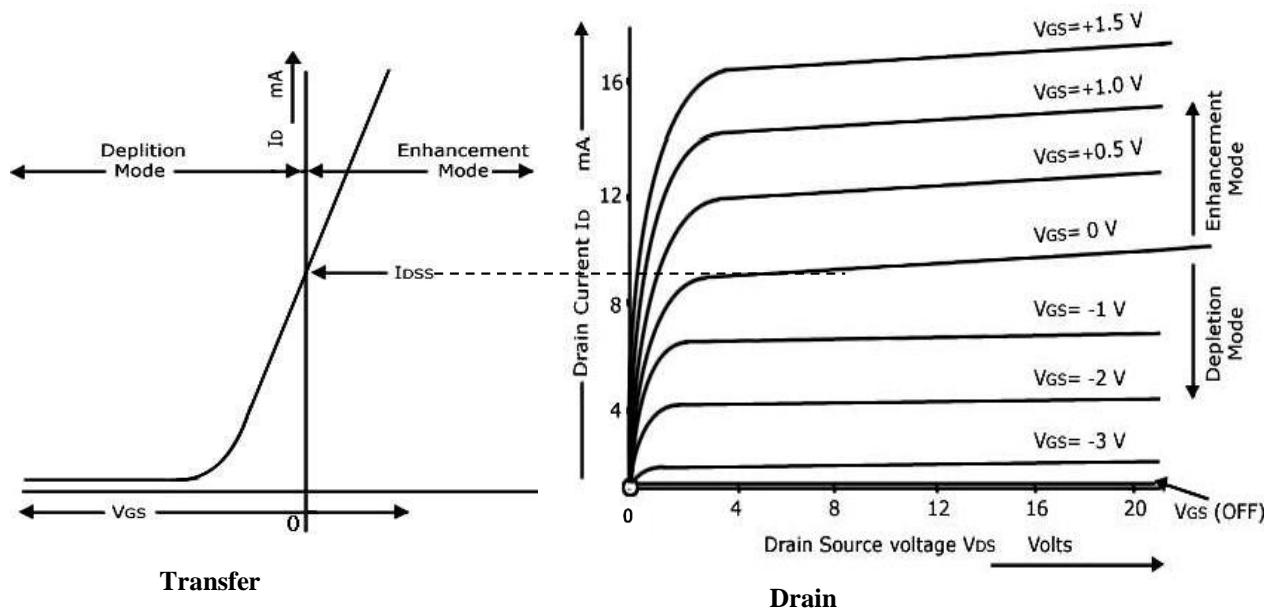


Fig. 2.10 Transfer characteristic and Drain characteristic of depletion MOSFET

### **Enhancement Mode:**

The construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of an N-channel between the drain and source terminals.

The minimum value of  $V_{GS}$  is required to form the induced N-channel, that turns the E-MOSFET ON is called threshold voltage [ $V_{GS\ (th)}$ ]. For  $V_{GS}$  below  $V_{GS\ (th)}$ , the drain current  $I_D = 0$ .

- (i) **When  $V_{GS} = 0\text{ V}$ ,  $V_{DS} = +\text{ve}$ :** There is no channel induced between Source and Drain. The p- substrate has only a few thermally produced free electrons (minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when  $V_{GS} = 0\text{V}$ .
- (ii) **When  $V_{GS} = V_{GS(th)} = +\text{ve}$ , and  $V_{DS} = +\text{ve}$ :** The free electrons developed next to the  $\text{SiO}_2$  layer and induced an N channel, as shown in the fig.2.11. Now a Drain current  $I_D$  starts flowing. E-MOSFET is turned ON. Beyond  $V_{GS\ (th)}$ , if the value of  $V_{GS}$  is increased, the induced N channel becomes wider, resulting large  $I_D$ . If the value of  $V_{GS}$  decreases not less than  $V_{GS\ (th)}$ , the channel becomes narrower and  $I_D$  will decrease.

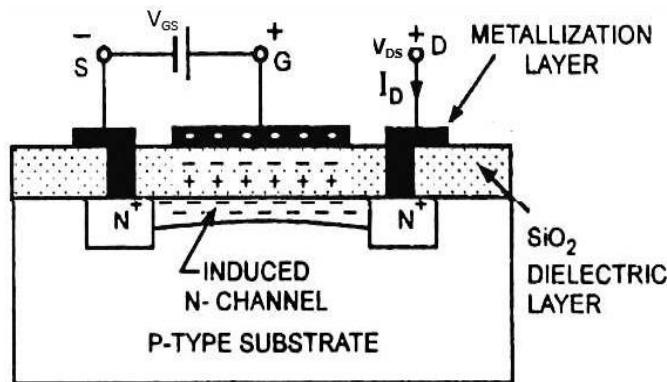


Fig. 2.11 MOSFET in enhancement mode with gate voltage positive

Since the conductivity of the channel is enhanced by the positive bias on the Gate, so this device is also called the enhancement MOSFET or E- MOSFET.

#### Characteristics of E-MOSFET:

**Drain Characteristics curve:** fig.2.12 (b), have almost vertical and almost horizontal parts. The vertical components of the curves correspond to the *ohmic region*, and the horizontal components correspond to the *saturation region* (constant current). Note the following worthy points:

- $I_D$  depends on different values of  $V_{GS}$  (from 0V to  $+V_{GS(\max)}$ ).
- When  $V_{GS} = 0$ , even for large increase in  $V_{DS}$ ,  $I_D = 0$ . This is said to be cut-off region. (MOSFET off state).

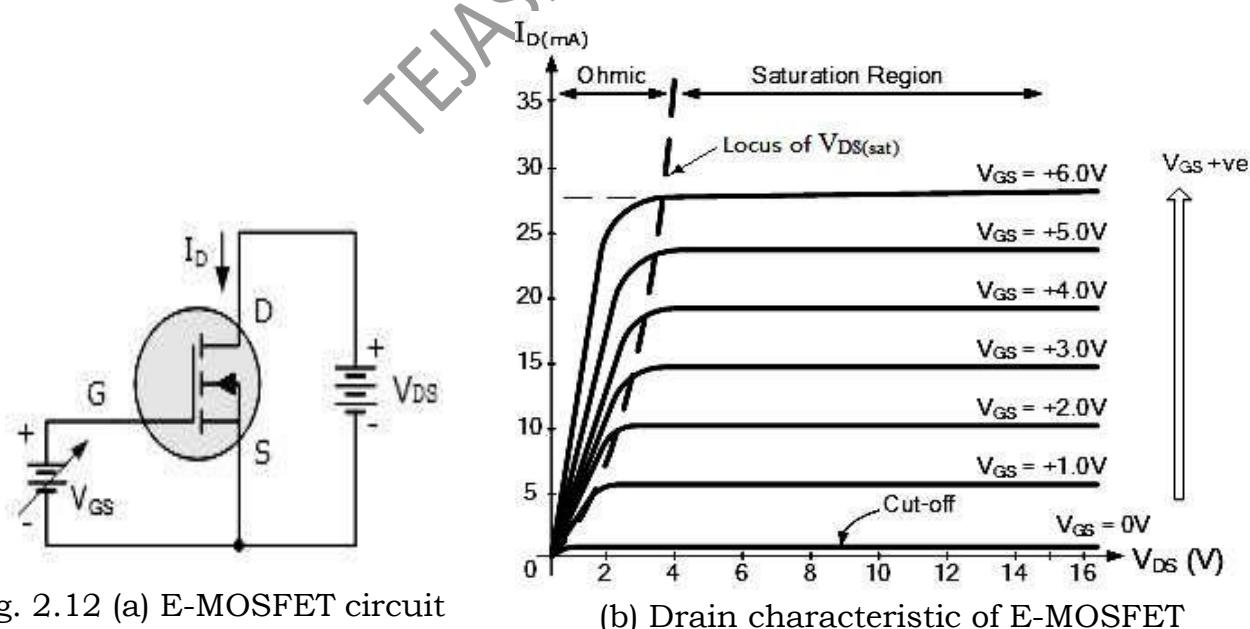


Fig. 2.12 (a) E-MOSFET circuit

(b) Drain characteristic of E-MOSFET

### Transfer Characteristics curve:

- i. When  $V_{GS} < V_{GS(th)}$ , then  $I_D = 0$ . This is because under this state, the channel will not be connecting between the drain and the source terminals. This is called as *cut-off region*. (MOSFET off state). The transfer curves of MOSFET is shown in the fig.2.13.
- ii. When  $V_{GS} > V_{GS(th)}$ , then  $I_D$  flows through the device, initially (Ohmic region) and then saturates to a value (*saturation region*). That means,  $I_D$  is controlled by the Gate voltage,  $V_{GS}$ .
- iii.  $I_D$  can be obtained by analytical expression:

$$I_D = k (V_{GS} - V_{GS(th)})^2$$

where

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \quad \text{A/V}^2$$

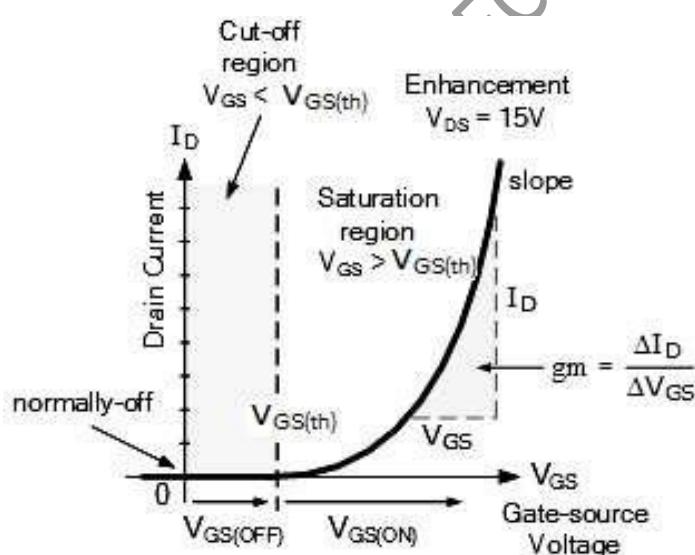


Fig.2.13 Transfer characteristic of E - MOSFET