L1 dTLBs

4KB pages: 64-entry, 4-way set-associative L1 TLB;
1 cycle access;
9 cycle miss penalty.

2MB pages: 32-entry, 4-way set-associative L1 TLB;
1 cycle access;
9 cycle miss penalty.

1GB pages: 4-entry, fully-associative L1 TLB;
1 cycle access;
9 cycle miss penalty.

L1 iTLBs

4KB pages: 128-entry, 8-way set-associative L1 TLB;
1 cycle access;
9 cycle miss penalty.

2MB pages: 16-entry, fully-associative L1 TLB;
1 cycle access;
9 cycle miss penalty.

PTWs

Supports 4 concurrent TLB misses.

Unified L2 TLBs

4KB/2MB pages: 1536-entry, 12-way set associative L2 TLB;
14 cycle access.

1GB pages: 16-entry, 4-way set- associative L2 TLB;
1 cycle access;
9 cycle miss penalty.

Others

MMU $: 32-entry, fully-associative;
1 cycle access.

nTLB: 16-entry, fully-associative; 1 cycle access (from microbenchmark).