BITS Pilani
Pilani Campus

Mechatronics (Merged - DEZG516/DMZG511/ESZG511)

Lecture

Microprocessors and micro-controllers

Introduction

- E.g. Traffic signal at a junction
- Solution – combination or sequential logic integrated circuits.

- If a complicated system e.g. dishwasher
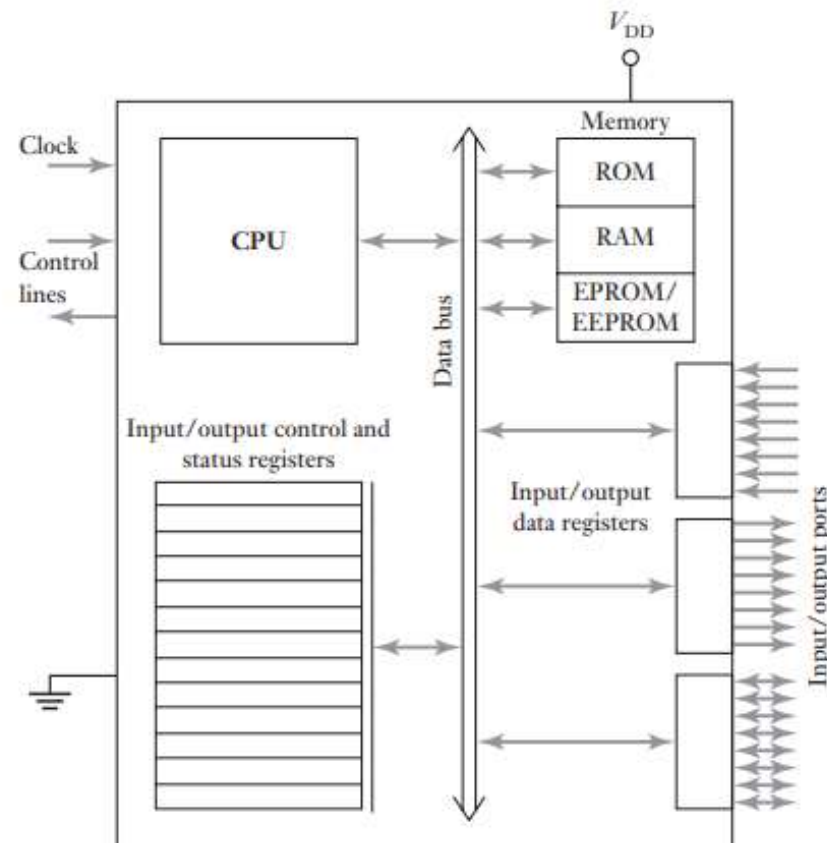- Solution – Self starting , No human intervention micro processor system.
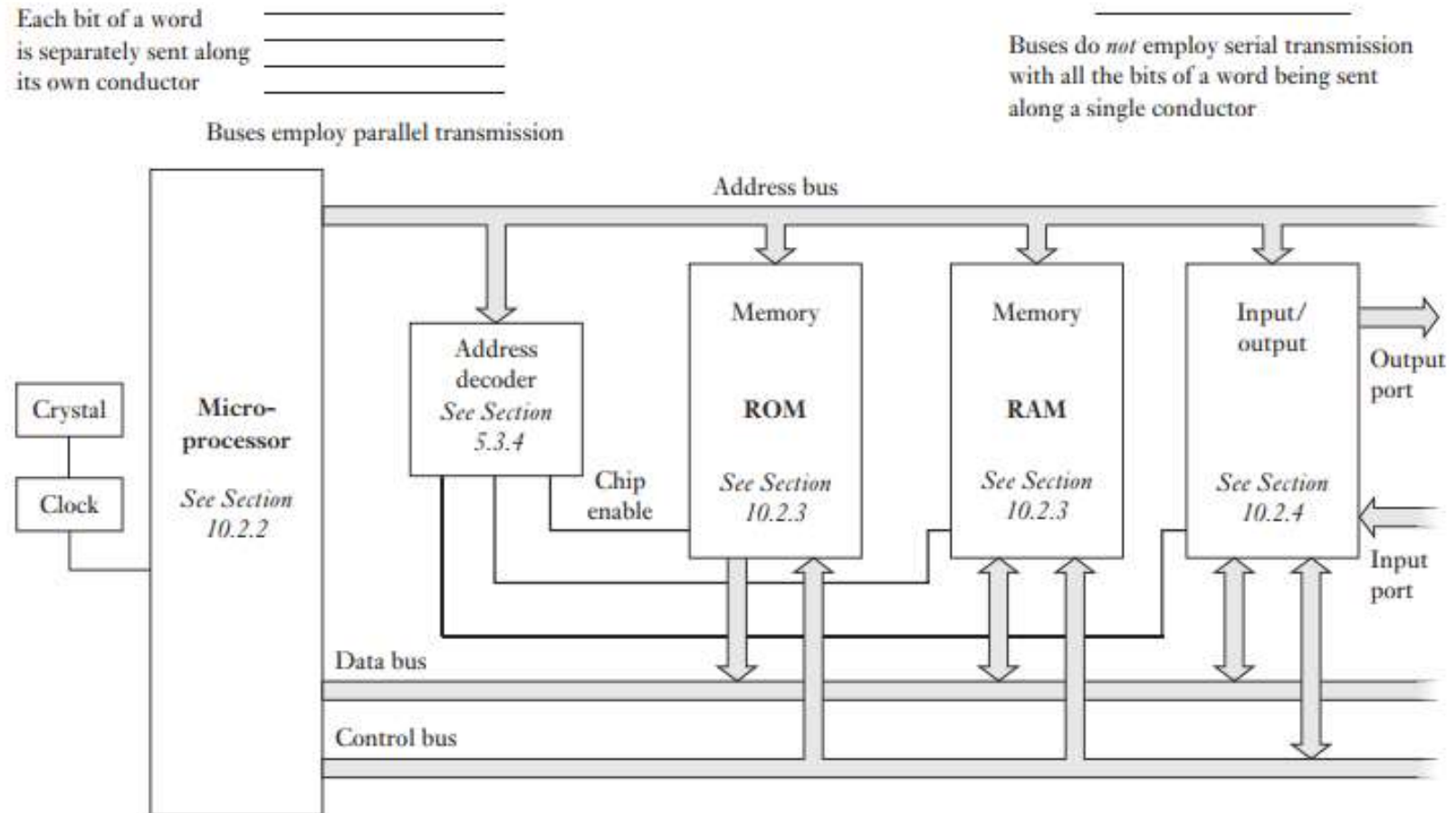
Micro Processor

- Many variables to control.

- Complex sequence of operations.

- Combination of hard wired configuration with Logic ICs and software.

Micro Controllers

- These are micro processors which have memory and various input / output arrangements all on one chip are called Micro Controllers.

General form of micro processor

Each bit of a word is separately sent along its own conductor

Buses employ parallel transmission

Buses do *not* employ serial transmission with all the bits of a word being sent along a single conductor

Address bus

Crystal

Clock

Micro-processor

See Section 10.2.2

Address decoder

See Section 5.3.4

Chip enable

Memory

ROM

See Section 10.2.3

Memory

RAM

See Section 10.2.3

Input/output

See Section 10.2.4

Output port

Input port

Data bus

Control bus

Figure 10.1 General form of a microprocessor system and its buses. All the components share the same data bus and address bus. This arrangement is known as the von Neumann architecture.

Components of Micro Processor

- Buses
  - Digital signal transmission lines.
  - No. of parallel conductors along with electrical signal, which is shared by all chips in the systems.

- Types of Buses
  - Data bus (processing function of CPU)
  - Address bus
  - Control bus

Address	Data contents
0000	
0001	
0010	
0011	
0100	
etc.	
1111	

Figure 10.5 Address bus size.

Components of Micro Processor

- Micro Processor CPU
  - Processes data
  - Fetching information from memory, decoding and executing them.

- Types
  - Arithmetic logic unit (ALU)
  - Registers
  - Control Unit

Types of registers

- Accumulator register
- Status register, or condition code register or flag register
- Program counter register (PC) or instruction pointer (IP)
- Memory address register (MAR)
- Instruction register (IR)
- General-purpose registers
- Stack pointer register (SP)

Components of Micro Processor
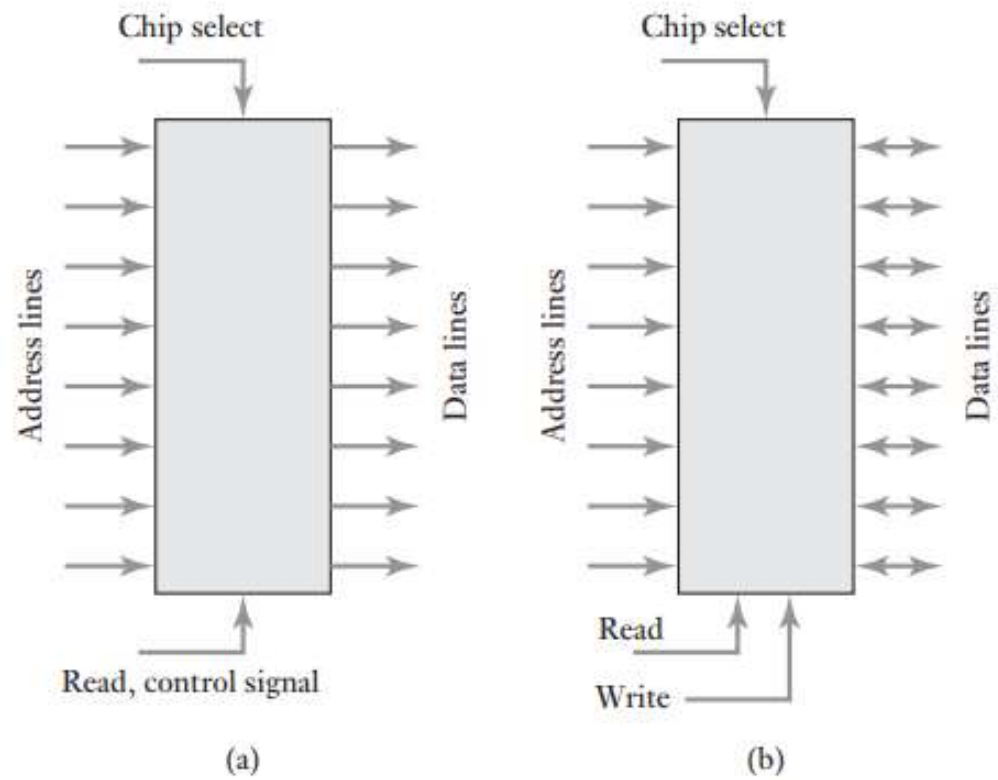
- Memory
  - Read-only memory (ROM)
  - Programmable ROM (PROM)
  - Erasable and programmable ROM (EPROM)
  - Electrically erasable PROM (EEPROM)
  - Random-access memory (RAM)
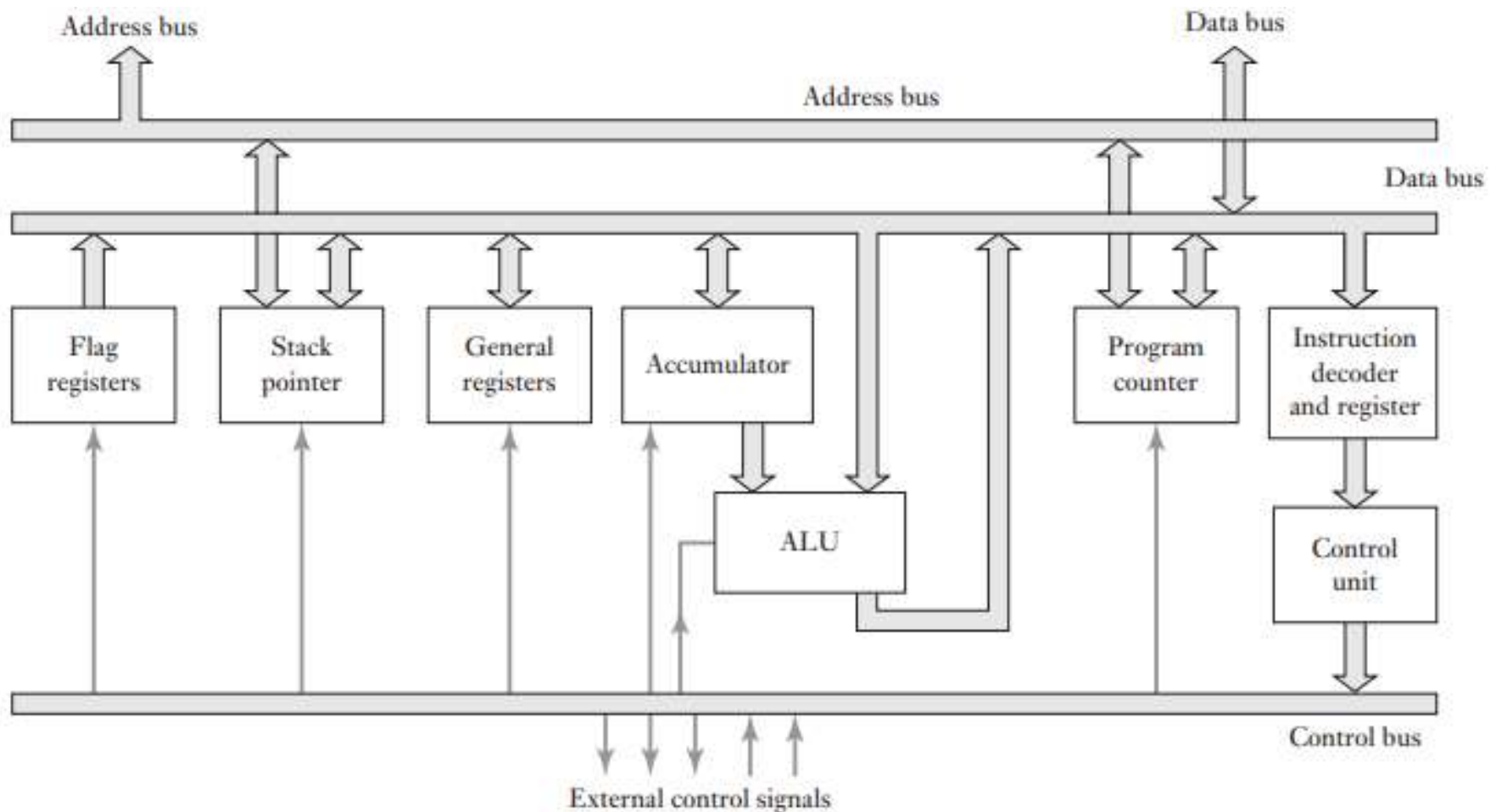
Figure 10.6 (a) ROM chip, (b) RAM chip.
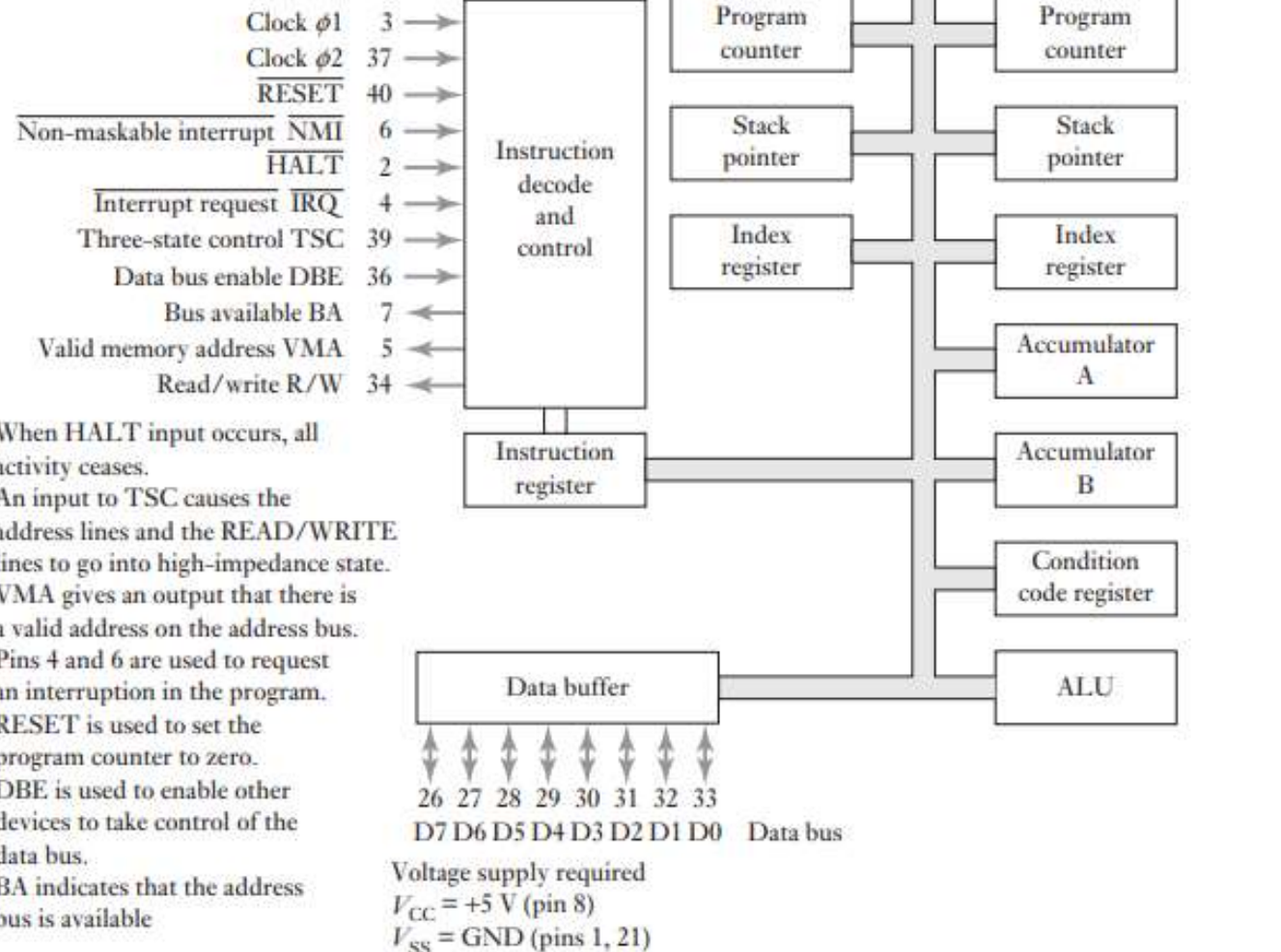
Components of Micro Processor

- Input / output devices

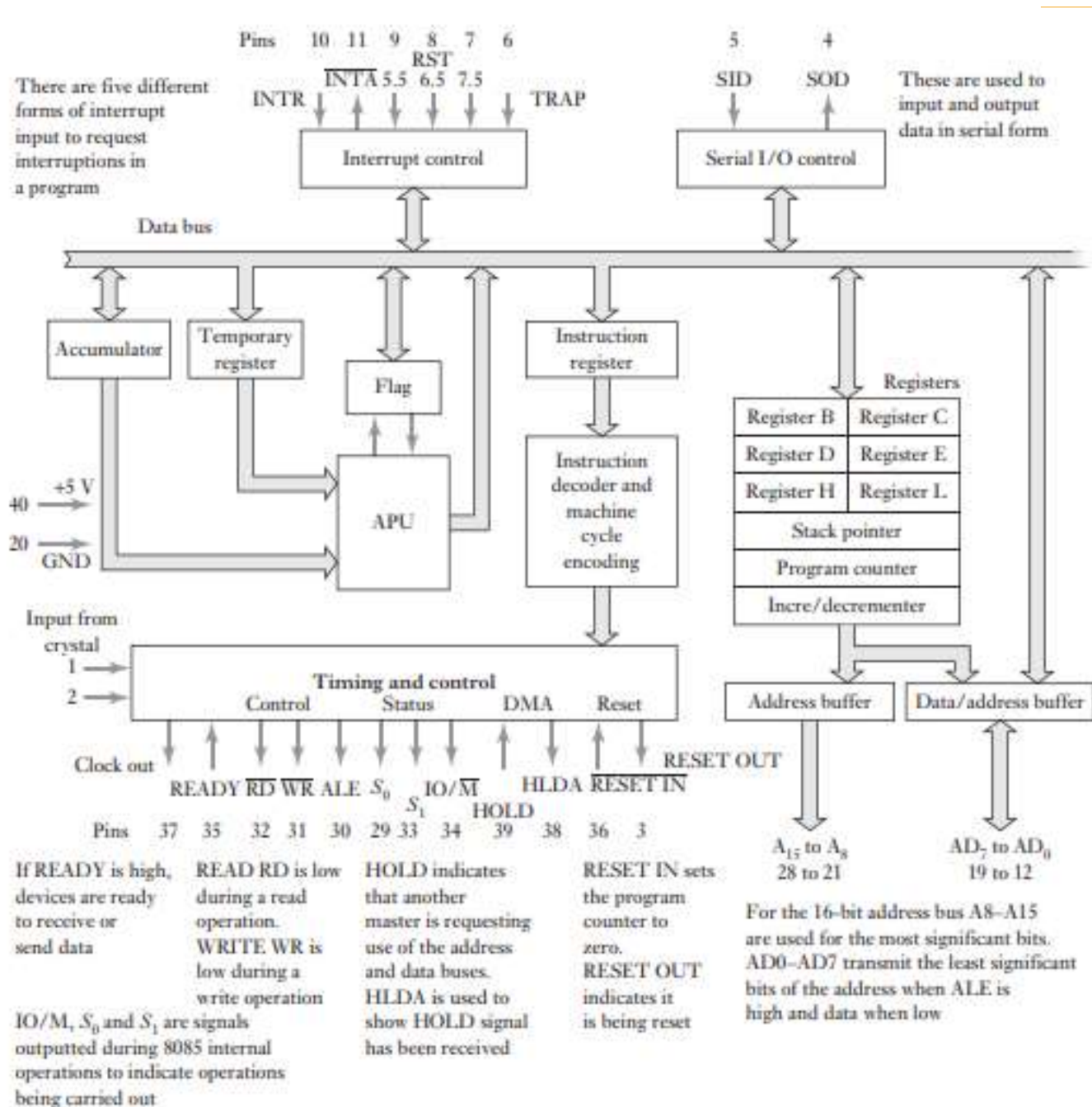# Internal Architecture of micro processor

Figure 10.2 General internal architecture of a microprocessor.

Buffers to generate sufficient current for external devices and prevent unwanted interactions between such devices and the microprocessor

Address bus

| A15 | to | A8 | | A7 | to | A0 |

25 24 23 22 20 19 18 17 Pin numbers 16 15 14 13 12 11 10 9

Output buffers

Output buffers

Clock ϕ1 3
Clock ϕ2 37
$\overline{\text{RESET}}$ 40
Non-maskable interrupt $\overline{\text{NMI}}$ 6
$\overline{\text{HALT}}$ 2
Interrupt request $\overline{\text{IRQ}}$ 4
Three-state control TSC 39
Data bus enable DBE 36
Bus available BA 7
Valid memory address VMA 5
Read/write R/W 34

Instruction decode and control

Program counter

Program counter

Stack pointer

Stack pointer

Index register

Index register

Accumulator A

When HALT input occurs, all activity ceases.
An input to TSC causes the address lines and the READ/WRITE lines to go into high-impedance state.
VMA gives an output that there is a valid address on the address bus.
Pins 4 and 6 are used to request an interruption in the program.
RESET is used to set the program counter to zero.
DBE is used to enable other devices to take control of the data bus.
BA indicates that the address bus is available

Instruction register

Accumulator B

Condition code register

Data buffer

ALU

26 27 28 29 30 31 32 33
D7 D6 D5 D4 D3 D2 D1 D0   Data bus

Voltage supply required
V_{CC} = +5 V (pin 8)
V_{SS} = GND (pins 1, 21)

Figure 10.3 Motorola 6800 architecture.

Figure 10.4 Intel 8085A architecture.

Thank You.