CSEE 4280: Advanced Digital Design

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Final Project Abstract

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Roles and Responsibilities

Abhi	Documentation
Trent	Documentation

Github Link

https://github.com/abhibogga/CSEE4280Workspace/tree/main/final_Project

Abstract

For the CSEE4280 final project, the team has decided on making the "Car Calculator"—a device designed to allow users and vendors to analyze driving data across any given trip. The Car Calculator will read a car's real-time data, including intake valve temperature, coolant temperature,

oil temperature, and active RPMs. This data will be gathered through the car's OBD-II port, a standard interface for communicating with a car's ECU. To convert the OBD-II data to UART serial data, the team will use an ELM237 IC. The FPGA will display this live data on seven-segment displays while simultaneously storing it on a microSD card. The microSD card feature enables easy data transfer; for instance, companies can analyze customer driving patterns by simply accessing the "trip data" stored on the card. Additionally, the system will visualize the data through a readable graph on any VGA-compatible monitor, offering a comprehensive view of trip performance.

The Car Calculator aims to be a deployable real-world product. Potential use cases include insurance companies leveraging driving data to offer lower rates to safe drivers and amateur racing teams analyzing throttle input relative to speed. Since most amateur racing teams modify consumer cars that still contain an OBD-II port, this product would be highly compatible. The system will operate as an embedded device within the user's car, continuously reading and processing data. The FPGA will read serial data in parallel, store it in a FIFO, and pass it through additional logic for storage in ROM (such as the microSD card) and real-time display on seven-segment displays. The FPGA's parallel processing capabilities are essential, enabling simultaneous data reading, display updates, and storage without performance bottlenecks—something a traditional CPU would struggle to achieve. This parallelism ensures low-latency data processing, high reliability, and real-time performance.

The primary design goals for this project include accurate real-time data acquisition from the ECU via the OBD-II port, efficient data storage in RAM or ROM, and dynamic data visualization through a VGA port. The system prioritizes real-time performance, data integrity, and scalability. To ensure reliability, error-handling mechanisms will be implemented to detect and manage corrupted data from the OBD-II port. Additionally, the VGA display will provide user-friendly graphical representations of key metrics. Essential components include an OBD-II to RS232 cable, an ELM237 IC, a UART to micro-USB cable, and the Nexus-A7 100t FPGA board. To optimize efficiency, work will be divided between the two team members: Abhi will manage the process from ECU data acquisition to FPGA integration, while Trent will focus on the FPGA-to-monitor data visualization via the VGA port. This division ensures that both team members can work concurrently, maintaining project momentum and enabling smooth integration of system components.