PREMIER UNIVERSITY CHITTAGONG

Department of Computer Science & Engineering

Report No : 03

Course Code : EEE 314

Course Title : Control Systems Laboratory

Name of the report : Designing an ON-Timer and OFF-Timer and Logic gate operation using PLC.

Date of Performance : 20/10/2019

Date of Submission : 16/11/2019

Submitted by	**Remarks**
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Objective:

- To design an ON-Timer and OFF-Timer.
- To design a NOR logic gate.
- To design a NAND logic gate.

Instrument Requirement:

- PLC SIMATIC S7-1200
- CPU 1212C DC/DC/DC
- ON-Timer
- OFF-Timer
- Normally open switch
- Normally close switch

Ladder Diagram:

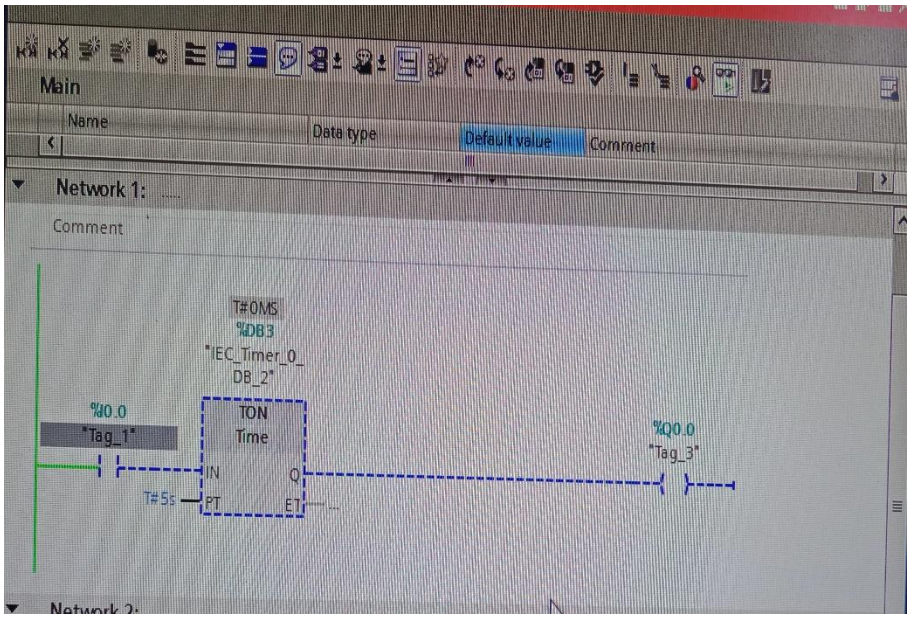


Fig 1: The Ladder diagram of ON-Timer.

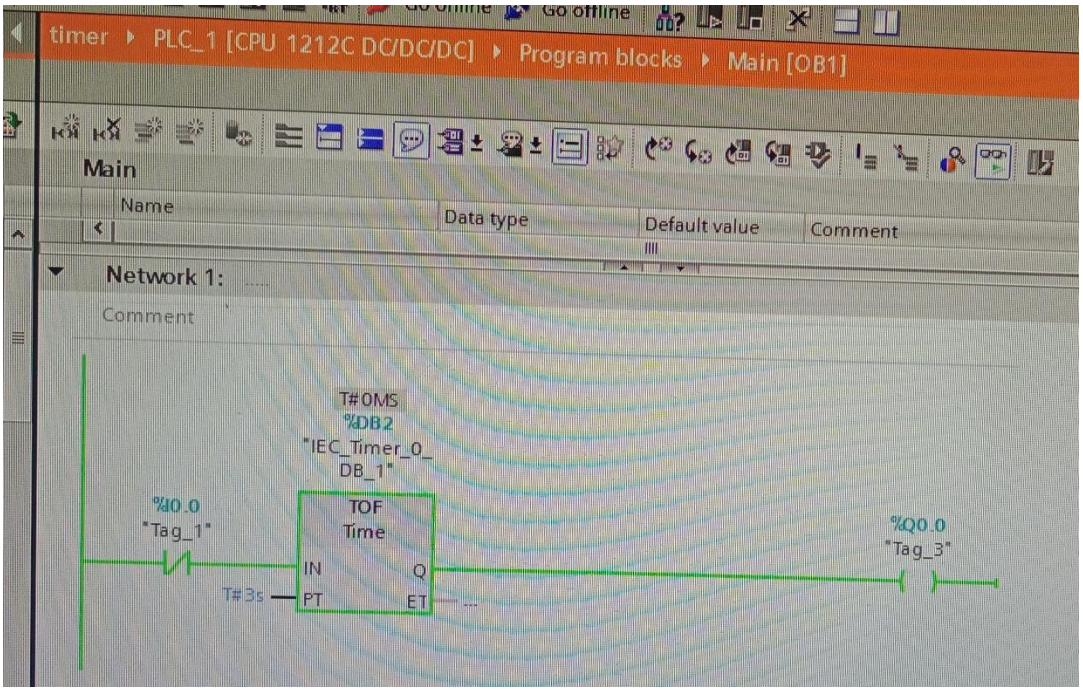
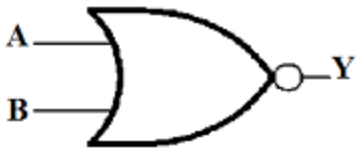


Fig 2: The Ladder diagram of OFF-Timer.

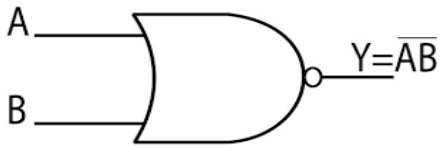
Logic Diagram of NOR Gate:



Inputs		Output
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

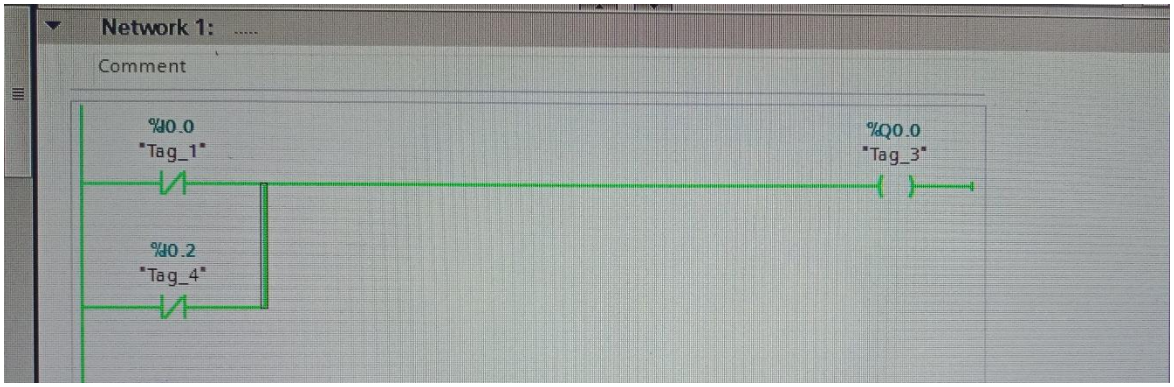
Ladder Diagram of NOR Gate:

Logic Diagram of NAND Gate:



Inputs		Output
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

Ladder Diagram of NAND Gate:



Discussion:

ON-Timer and OFF-Timer

A timer is one of the most essential and useful entity. The role of PLC timer is to control and to operate the device for a specific duration. With the timer, we can perform any specific operations for a particular time span. We also can set the timer with simple PLC programming instructions. Every PLC having different timer functions. Timers are used to provide programming logic and to decide when to turn on or off the circuit. It has both normally open (NO) or normally closed (NC) contact.

TON is called on delay timer. It helps to start momentary pulses and activated the output contact based on the delay time. In the Programming, when an On-delay timer is energized (True), it delays turning ‘on’ the timer’s output. This output will be ‘on’ until the timer’s preset time value is reached.

TOF is called Off-delay timer**.** It helps to switch off the output or system after a certain amount of time. In PLC programming, when the off-delay timer is energized (True), it immediately turns ‘on’ its output. The output will be ‘on’ till it reaches the setting time. When it reaches preset time, the output turns ‘off’. Due to the turning ‘off’ condition, the timer is de-energized (False).

NOR Gate:

NOR Gate is operated OR Gate followed by the NOT Gate. When both inputs are low then the output will be high. Otherwise, the low output will occur if both inputs are high.

NAND Gate:

NAND gate is operated as an AND gate and followed by the inverter. In NAND Gate, the output will be low when both inputs are high. For all other cases, the output will be high.
