CS4100: Computer System Design
Lab Assignment 3

Deadline: 20th Sept 2015

The objective of this project is to understand the scheduling policies in DRAM. DRAMSim simulator is used. https://github.com/dramninjasUMD/DRAMSim2

1) Implement Read over Write scheduling in the Transaction Queue (TQ). High and low watermarks are 24, 6 respectively. Compare the average read latency with FR-FCFS scheduling with and without Read over Write scheduling in TQ for both open page and close page policies.
2) Implement a new command scheduling algorithm and compare the average read latency with FR-FCFS for both open page and close page policy. Read over Write should be enabled in TQ.

Parameters for Simulation:
8 GB main memory with 2 channels.
Device Ini File - DDR3_micron_32M_8B_x4_sg125
Cycles - 4500000
Traces - k6_aoe_02_short, mase_art
Read TQ - 32
Write TQ - 32
Command Queue size - 64
Queuing Structure - per_rank
Scheduling Policy - rank_then_bank_round_robin (FR-FCFS policy).
Choose the address mapping best suited for open page and close page policy.

Teams will be ranked based on the average read latency (lower the better).