PCA: Assignment3

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Q1

Following are the results obtained for the caches with the given configuration on a 4-core processor with 2GHZ processor frequency:

IL1 & DL1: Delay description for Data(R/W) and Tag components are summarized as follows: 1.26907 ns

Delay-components(ns)	**Data(R/W)**	**Tag Comparison**
H-tree input delay	0.032889	0
Decoder + wordline delay	0.381636	0.115967
Bitline delay	0.663435	0.0530674
Sense Amplifier delay	0.00894838	0.00254624
H-tree output delay	0.182162	0.0308792
Total	1.26907	0.20246

L2-Cache: Delay description for L2 cache with the configuration(cache-size: 256KB, 8-way, 64B block, LRU policy) is as follows:

Delay-components(ns)	**Data(R/W)**	**Tag Comparison**
H-tree input delay	0.0789287	0
Decoder + wordline delay	0.386641	0.133863
Bitline delay	1.13705	0.108453
Sense Amplifier delay	0.00894838	0.00257713
H-tree output delay	0.309035	0.0337437
Comparator delay	0	0.0347248
Total	1.9206	0.278637

L3-Cache: Delay description for L3 non-inclusive cache using UCA with 1 bank and the configuration as(L3-Cache: 4MB shared, 64B block, 16-way associative, and non-inclusive)

Delay-components(ns)	**Data(R/W)**	**Tag Comparison**
H-tree input delay	0.181005	0
Decoder + wordline delay	0.645706	0.316044
Bitline delay	1.29647	0.310651
Sense Amplifier delay	0.00894838	0.00257713
H-tree output delay	0.529933	0.0401816
Comparator delay	0	0.0347248
Total	2.66207	0.669453

for bank count 4, i.e. 1MB per core:

Delay-components(ns)	**Data(R/W)**	**Tag Comparison**
H-tree input delay	0.299223	0.0234102
Decoder + wordline delay	0.386641	0.190739
Bitline delay	1.13705	0.2168
Sense Amplifier delay	0.00894838	0.00257713
H-tree output delay	0.493949	0.0394726
Comparator delay	0	0.0327059
Total	2.43368	0.496409

Q2: