A Short Note on Intel's Skylake and IBM's POWER8 Microarchitectures

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Abstract

The aim of the report is to discuss the main characteristics of Intel's Skylake and IBM's Power8 microarchitectures and present a short comparison between these and their earlier versions.

IBM POWER8

POWER stands for **P**erformance **O**ptimization **W**ith **E**nhanced **R**ISC. No BIOS configuration setup, everything has to be configured and booted via Flexible Service Processor(FSP) software. Power8 can be scaled to more than 4 sockets and uses a Single Chip Module(SCM) which contains a single processor chip using 22nm technology with upto 12 functional core. In addition, it can spawn 8 threads/core, has L3-cache of 8MB/core and L4-cache of 16MB/core and memory bandwidth of 192GBs per socket. It incorporates and on-chip controller which eliminated the need for a separate module to handle power management and thermal monitoring, error handling for off-chip accelerators etc. using Coherently Allocated Processor Interface(CAPI), integrated PCIe function, L4-cache persistent fault handling, dynamic substitution of unassigned memory for DIMMs called out for repair and has single 1-rank DIMM containing sufficient DRAMs to support two 128-bit words. Integrated I/O Hub Logic into the processor module which eliminates the need for external I/O hub controllers, PCIe adapters can be removed/replaced without the need to shut the system or terminate the partitions. Power8 comes with 64K data cache, 32K instruction cache, can handle 10 issues, 8 dispatch and 16 execution at a time, has enhanced prefetching and larger issue queues(4x16-entries), provides larger global completion and load/store reorder. It has improved branch prediction and unaligned storage access over Power7. From the virtual addressing perspective accelerator can work with same memory addresses that the processors use, pointers de-referenced same as the host application, removes OS or device driver overhead. Hardware managed cache coherence enables the accelerator to participate in "locks" as a normal thread and lowers latency over I/O communication. PCIe(gen3) is used to transport the encapsulated messages.

Intel's Skylake

Skylake microarchitecture uses 14nm process nodes. The Skylake IA core is designed to allow for more operations to be dispatched, queued and retired in a single clock and extract Instruction Level Parallelism(ILP) from code. Similar to Intel's previous generation processors, Skylake-**K/H** will have 16 **PCIe** 3.0 lanes to use for directly attached devices to the processor, whereas these PCIe lanes

have been removed from Skylake-**U/Y** processors which rather use chipset PCIe lanes. The Skylake-**S/H** are connected to the chipset by the four-lane **DMI 3.0** interface which is an upgrade over the previous generation DMI 2.0 and boosts the speed from 2GB/sec to ∼3.93GB/sec but this upgrade requires the motherboard traces between the CPU and chipset to be shorter(7 inches rather than 8) to maintain the signal speed and integrity and allows **chipset connectivity**. Prior to Haswell, voltage regulation was performed by the motherboard. This was deemed inefficient for power consumption and for Haswell/Broadwell Intel decided to create a fully integrated voltage regulator(FIVR) in order to reduce the motherboard cost and power consumption. This had an unintended side-effect - while it was more efficient, it also acted as a source of heat generation inside the CPU with high frequencies. As a result overclocking was limited by temperatures and the quality of FIVR led to a large variation in the results. For Skylake, the voltage regulation is moved back into the hands of the motherboard manufacturers which will result in cooler processors depending on how the silicon works but will result in slightly more expensive motherboards. Intel removed FIVR to deliver the best performance across a broader range of thermal design powers. The Skylake-S processors use new socket, LGA 1151, while the soldered down models use a combination of BGA 1515(Skylake-Y), BGA 1356(Skylake-U), and BGA 1440(Skylake-H). Skylake is a dual memory channel architecture, supporting two memory modules per channel. Skylake processors will support both DDR3L and DDR4 memory modules(RAM) where DDR3L is different than DDR3 and operates at low voltage. Below is the comparison of the instruction window of skylake with other Intel processors.

	Sandy Bridge	haswell	Skylake
Out-of-order window	168	192	224
In-flight loads	64	72	72
In-flight stores	36	42	56
Scheduler Entries	54	60	97
Integer Register File	160	168	180
FP Register File	144	168	168
Allocation Queue	28/thread	54	64/thread

Skylake allows dispatch of six micro-ops at a time, better from four in Haswell. It comes with improved **branch-predictor**, faster **prefetch** and increased in-flight buffers that enable front-end(μ-op allocation and up) to perform better. Skylake provides dedicated servers and IP configurations, extracts more instruction-level parallelism. On the front-end, the divider is improved, but the floating point multiply has increased in latency over Broadwell but same as Haswell. Execution units' power is shut down when not in use, L2 cache is reduced from 8-way to 4-way associative model which saves some power but loses performance, allows each thread in core to retire four μ-op in one cycle. From security perspective, Skylake supports Intel® Software Guard Extension(Intel® SGX) technology, which supports new instruction and flows to create and isolate enclaves(a terms which means that a a program can be run in its own environment and cannot interact outside of it and any attempt by other programs to access the memory it resides in, fails) from malware and privileged software attacks, to ensure that the physical memory access falls within the bounds of the memory allocated to the calling process, it supports Intel® Memory Protection Extensions(Intel® MPX) implementation which tests memory(both stack and heap) buffer boundary prior to memory access. Skylake consists of integrated System Agent(SA), on package PCH and eDRAM. Its Package Control Unit(PCU) acts as power management logic and controller firmware, tracks internal statistics and is an interface to higher power management hierarchies such as OS, BIOS, EC, graphics driver etc. Power of System(Psys) feature provided in Skylake CPUs and controlled by software implementations allows the CPU to track and control the CPU power based on total platform power consumption. Autonomous algorithm conserves energy by lowering frequency for low computation demands.