CS305
Computer Architecture

Hardware Implementation of MIPS: Preliminaries

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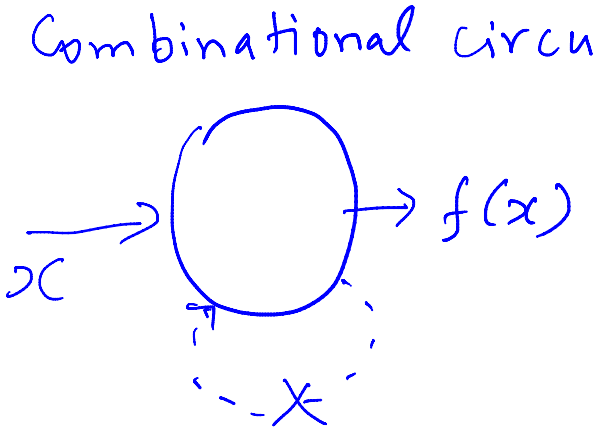
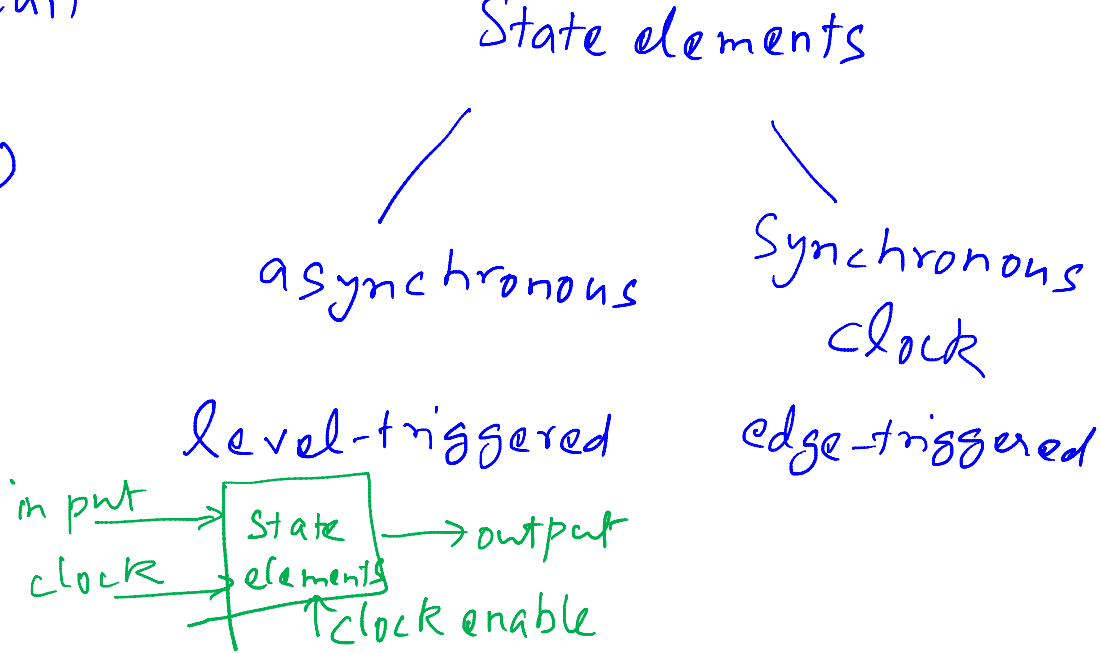
Recall: Combinatorial vs Sequential Circuits

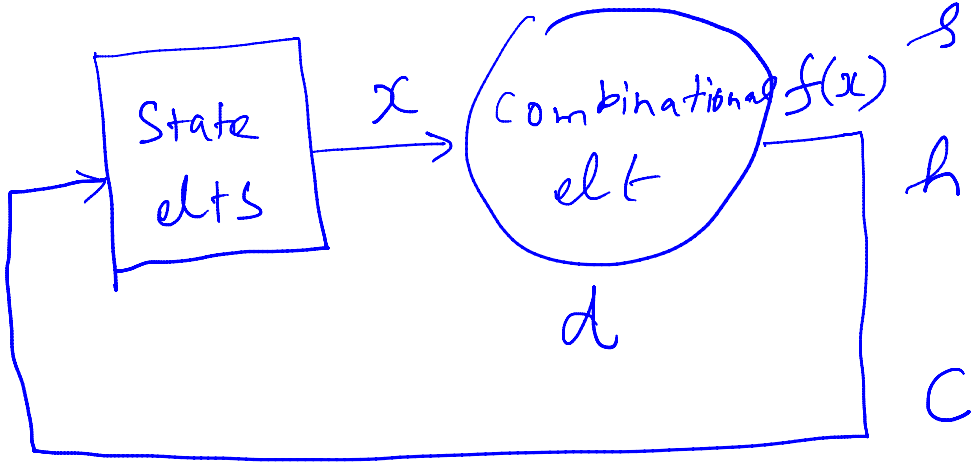
Combinatorial circuit



Sequential circuit



Sequential + Combinational Circuit

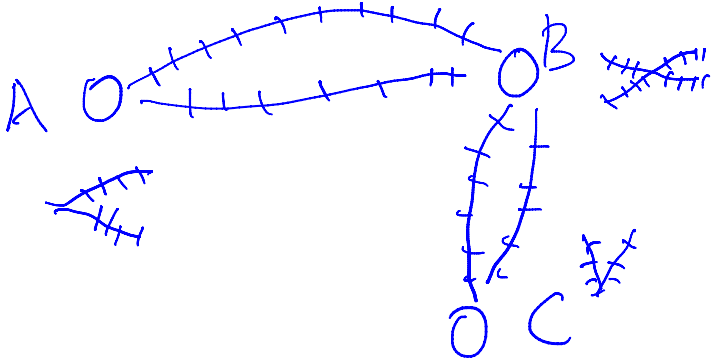


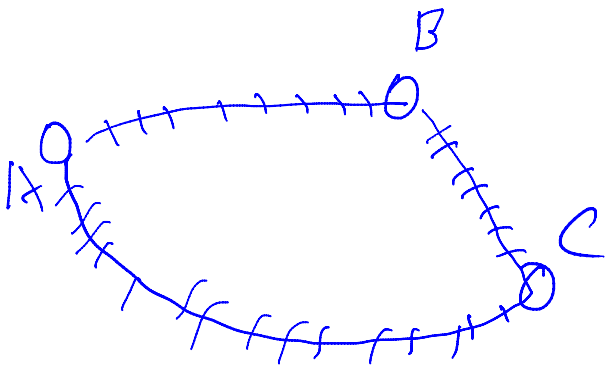
Setup time

hold time

$C > d + s + h$

Control Path, Data Path Analogy





Datapath

- platforms
- rail lines

Control path / signals

- trains should not collide
- no deadlock

Control Path, Data Path in MIPS Implementation

Data path

- state elts
- combinational elts
- interconnections

Control path

- when to write
- what to write

Summary

- Synchronous (clocked) sequential circuit, edge-triggered
- Increasing complexity:
  - Single-cycle implementation
  - Multi-cycle implementation
  - Pipelined implementation
- **DRAW** circuit diagrams to **LEARN** effectively
  - Not enough to look at drawings