Problem Set – 3
Solutions

CS 230, Autumn 2023

1.

```
 li $t0,
   3 li $t2,
   7
   slt $t3,  $t0,  $t
   beq $t3, $zero, else
   add $t1, t0, $t2;

   else:
        add $t1, $t0, $t0
```

2.

a. There are 64 registers. We need $\lceil log_2(64) \rceil$ = **6 bits** to label each register.

b.

Three Address Instructions

There are 3 6-bit registers and 30 operations. Therefore, we have $30 * \mathbf{2}^{18}$ combinations.

Two Address Instructions

There are 2 6-bit registers and 40 operations. Therefore, we have $40 * \mathbf{2}^{12}$ combinations.

One Address Instructions

There is 1 6-bit register and 60 operations. Therefore, we have $60 * \mathbf{2}^{6}$ combinations.

Total number of combinations $= (30 * \mathbf{2}^{18}) + (40 * \mathbf{2}^{12}) + (60 * \mathbf{2}^{6})$
$= 62750 * \mathbf{2}^{7}$

Total bits needed to represent all combinations = $log_2(62750 * \mathbf{2}7) = 23$

Since we have 32 bits instructions, it is possible to encode all operations.

3.

Each instruction = 32 bit

Number of instructions which are supported = 70

Maximum value by unsigned operand = 8191

Formula:

Opcode	Register 1 (R)	Register 2 (R)	Immediate Operand

In bits,

Opcode + R + R + Immediate Operand = 32

Calculation

Number of bits needed for opcode = $\lceil \log_2(70) \rceil$ = 7 bits

The maximum value of unsigned immediate operand = 8191

$2^n - 1 = 8191$

$2^n = 8192 = 2^{13}$

$\therefore$ n = 13 bits

7 + R + R + 13 = 32

2R = 12

$\therefore$ R = 6 bits.

Maximum registers that a processor has = 2^6 = 64.

4.

Code line	**Live Variables**
	-
`int a, b, c, d, e, f, g, h, i, j, k, l, m, n, o;`	
	b, c, e, g, i
`a = b * c;`	
	a, e, g, i
`d = a - e;`	
	d, g, i

`f = d + g;`	
	f, i
`h = f * i;`	
	h

a. Before line 2, 5 variables are live. We need 5 registers to store value of each variable. We also need an additional register for variable '*a*' to store the value of the expression *b*c*. Therefore, **5 registers** are needed. The compiler can reuse registers, assigned to a variable if it is not live. Since MIPS has 10 temporary registers, there will not be spill to memory.
b. The minimum number of registers required is 5. MIPS has 10 temporary registers, so no extra register is needed.

5.

REGISTER NAME:	T0	T1	T2	T3	S0
REGISTER VALUE:	4	7	3	4	10