CS305
Computer Architecture

Exceptions in the Pipeline

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How to Handle Exceptions in the Pipeline?

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
`SLL R2, R2, 3`	IF	ID	EX	MEM	WB			
`LW R4, 4(R5)`		IF	ID	EX	MEM	WB		
`ADD R1, R2, R3`			IF	ID	EX	MEM	WB	
`SW R4, 4(R20)`				IF	ID	EX	MEM	WB

Suppose LW has a misaligned memory address exception

Q: When is the exception detected?

A: End of CC4

Q: What should happen?

A: Flush pipeline, but SLL must be allowed to complete!

Steps in Exception Handling

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
`SLL R2, R2, 3`	IF	ID	EX	MEM	WB			
`LW R4, 4(R5)`		IF	ID	EX	MEM	WB		
`ADD R1, R2, R3`			IF	ID	EX	MEM	WB	
`SW R4, 4(R20)`				IF	ID	EX	MEM	WB

- Flush ➔ zero out latches
  - IF/ID, ID/EX, EX/MEM; **do not** flush MEM/WB (SLL)
- Load "appropriate" PC value onto EPC
  - PC–8 in this case
  - What if BEQ instead of ADD ?
- Load appropriate value onto Cause register
- PC = 0x8000 0180

Complexity-1: Multiple Exceptions

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
`SLL R2, R2, 3`	IF	ID	EX	MEM	WB			
`LW R4, 4(R5)`		IF	ID	EX	MEM	WB		
`Invalid opcode`			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

Q: Example of multiple exceptions?

A: Invalid opcode following LW

Q: What should happen?

A: Instruction causing earlier exception takes precedence

Complexity arises due to sheer number of such possibilities

Complexity-2: Out-of-Order Completion

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
`MUL R1, R2, R4`	IF	ID	MUL1	MUL2	MUL3	MUL4	MUL5	MEM
`ADD R4, R5, R6`		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

- MUL exception in CC7
- ADD is done by then!
- Need to “rollback” (Charlie Chaplin in pipeline)
- Solution is well beyond scope of this course

Complexity-3: Partially Changed Machine State

- Classic example: string copy instruction in Intel
- Say, half way through string copy, some other instruction causes exception
- What a mess!

Conclusion

- Exceptions and non-uniformity: enemies of pipelines
- Advanced topics:
  - Out-of-order completion
  - Super-scalar processors: multiple instruction issue per cycle
  - Data driven architectures
- Next: memory systems