CS305
Computer Architecture

Bus Protocols

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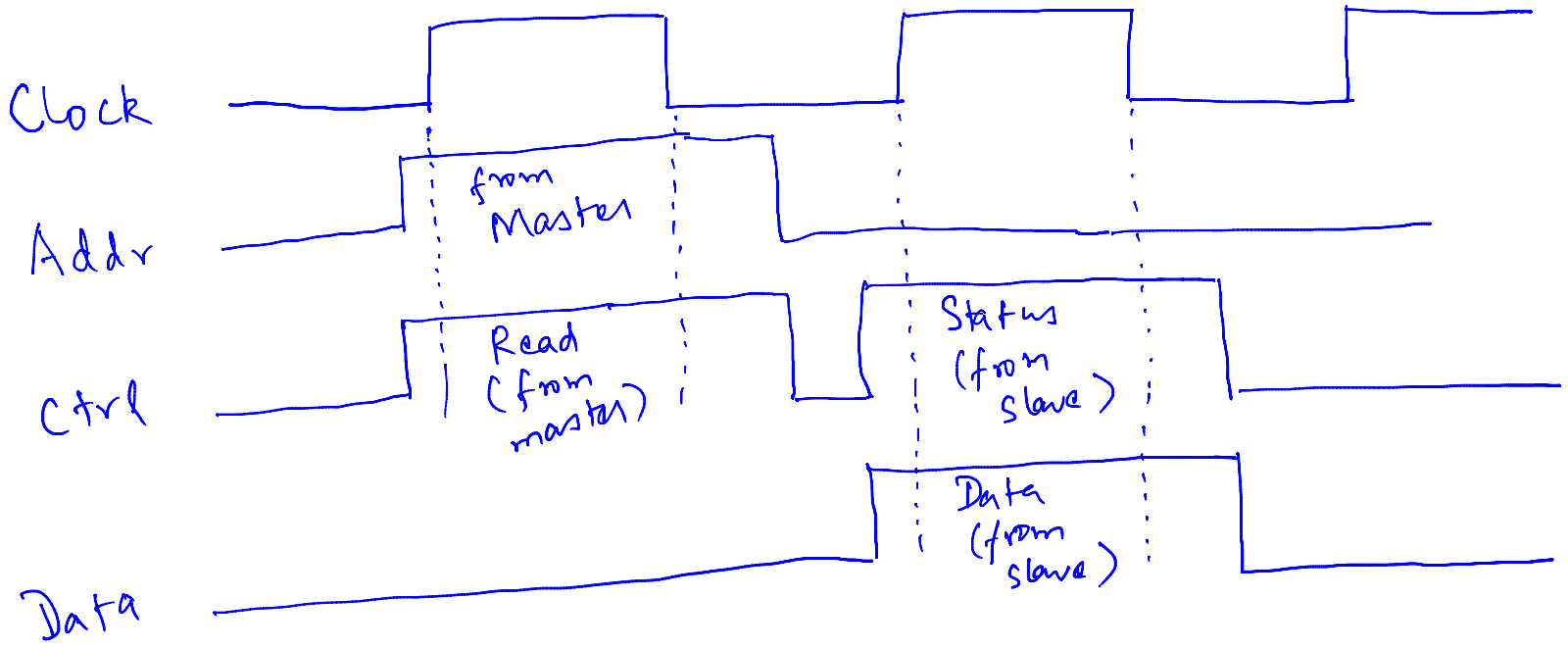
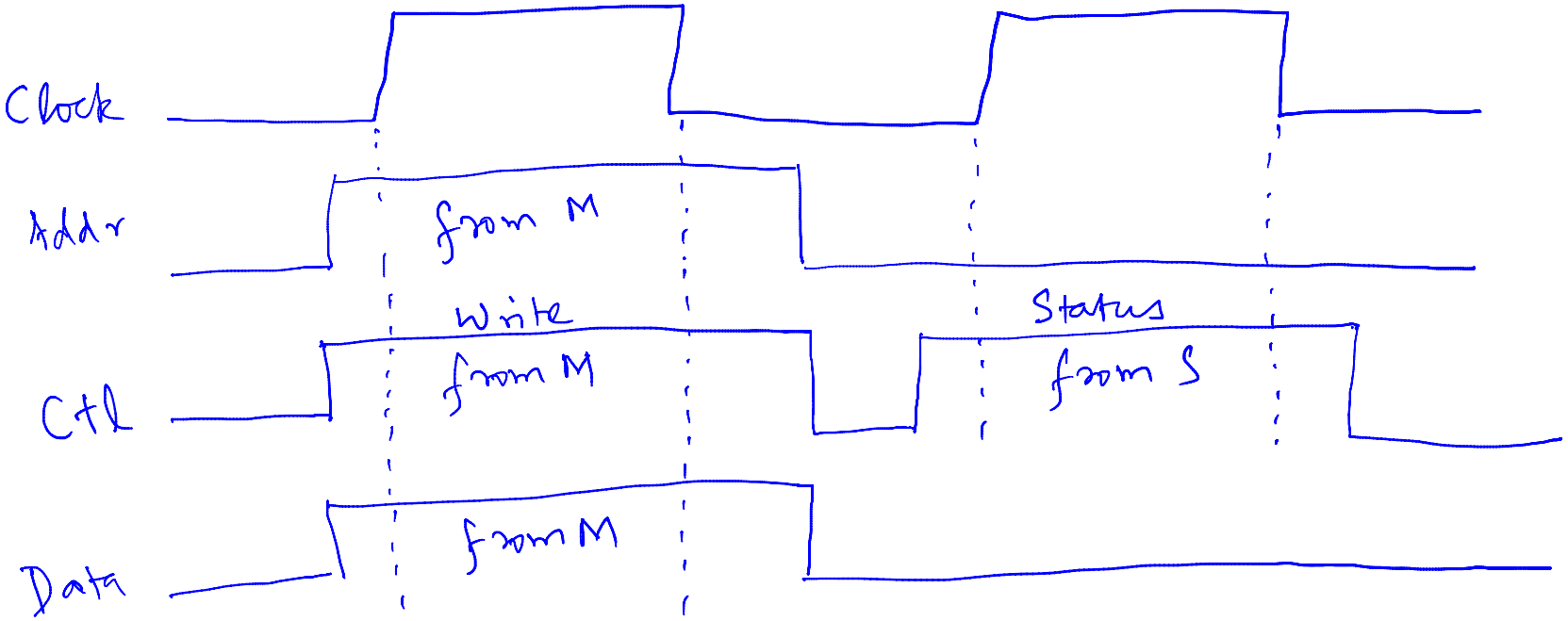
Bus Protocol or Timing

- Two types: synchronous, asynchronous
- Synchronous: use a clock line
- Asynchronous: no clock line

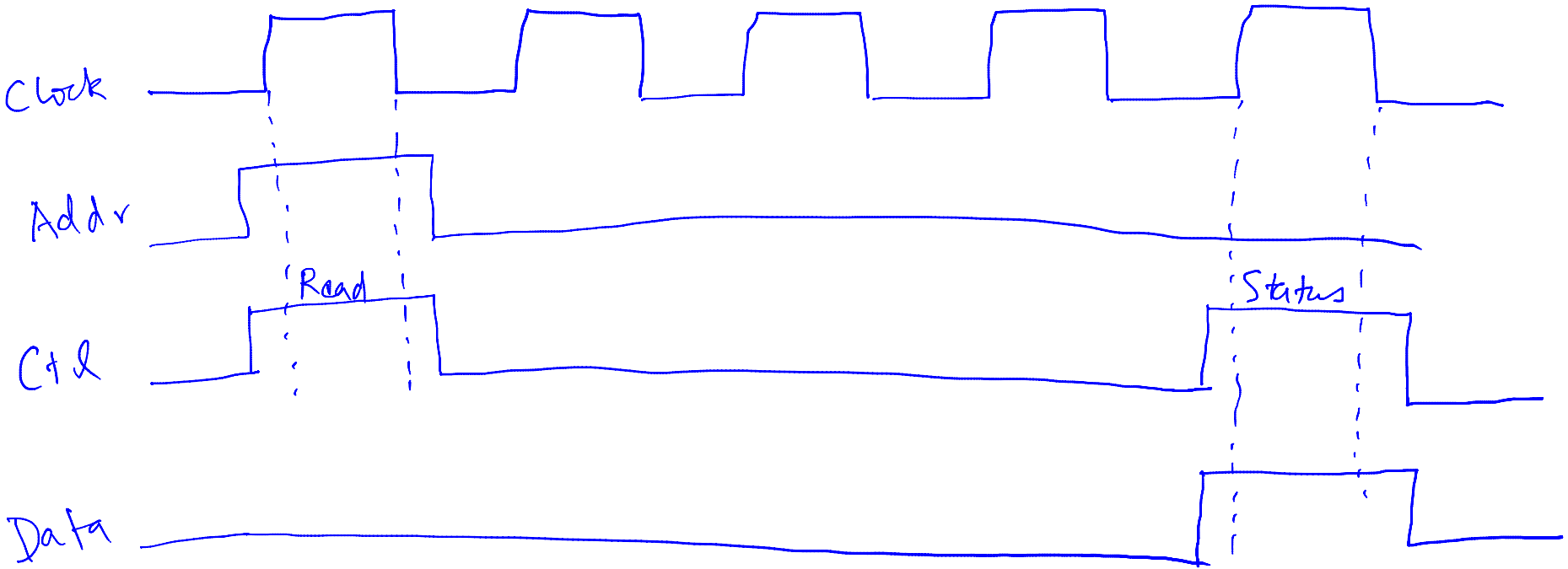
An Example Timing Diagram: Mem Read



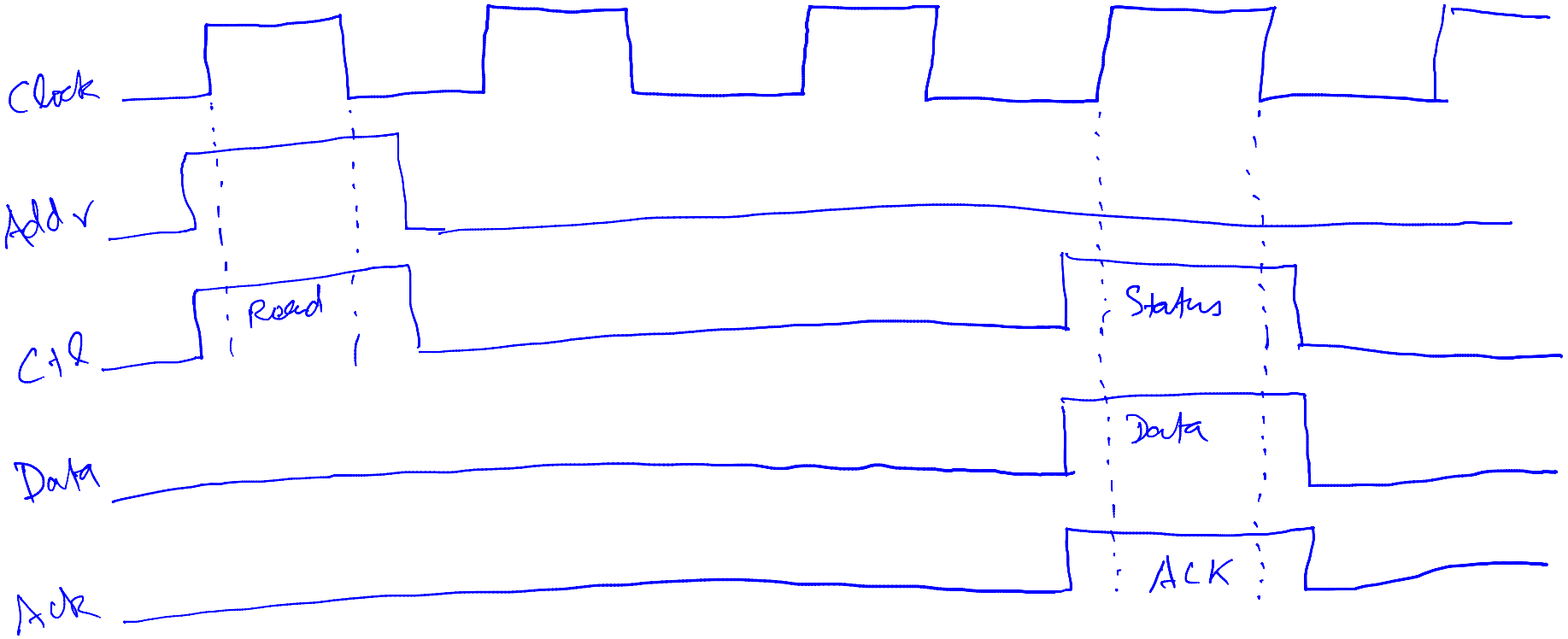
An Example Timing Diagram: Mem Write



Memory Read Taking 4 Cycles



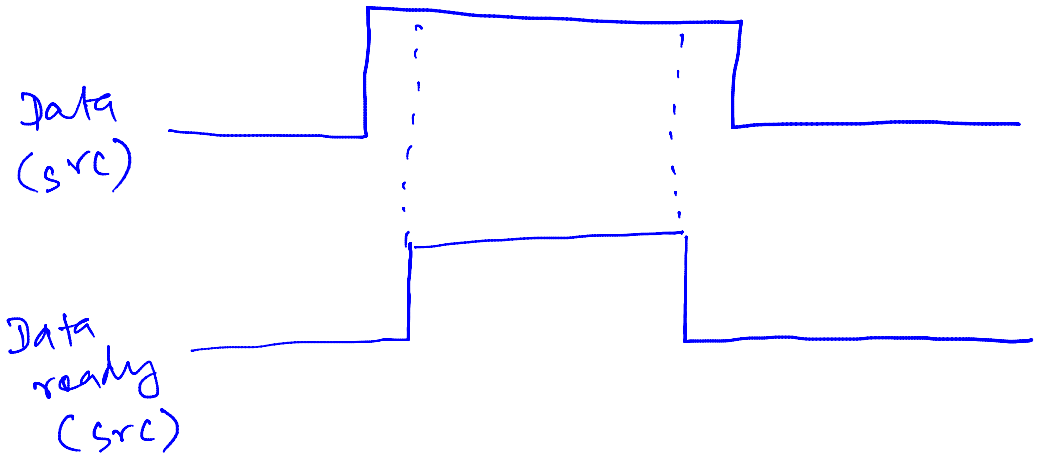
Memory Read Taking Variable #Cycles



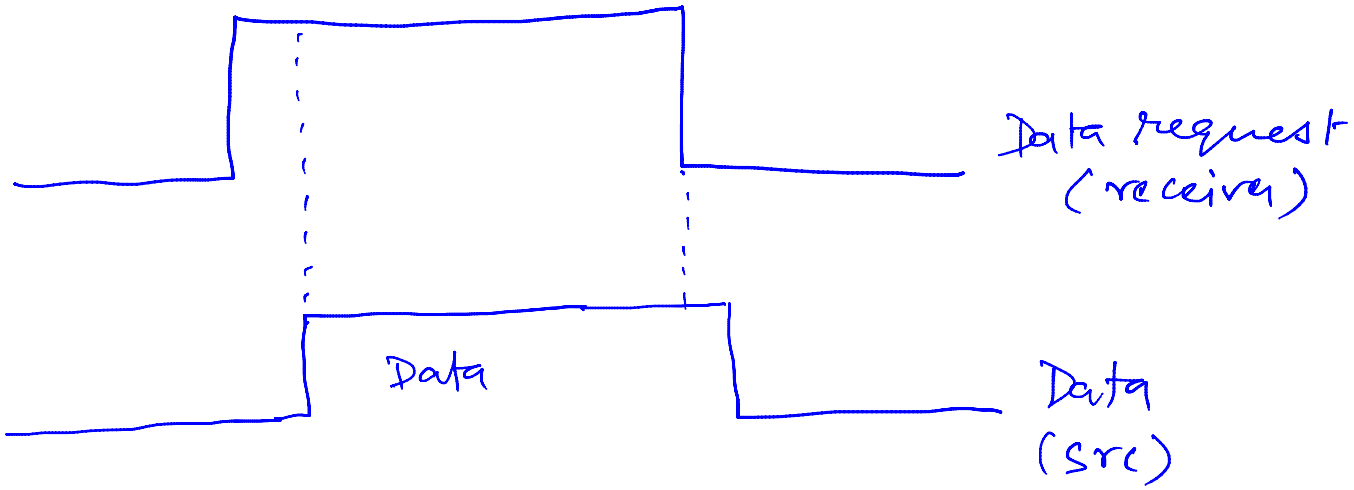
Asynchronous Transactions

- One-way
- Two-way handshake, or interlocked

One-Way Source Initiated



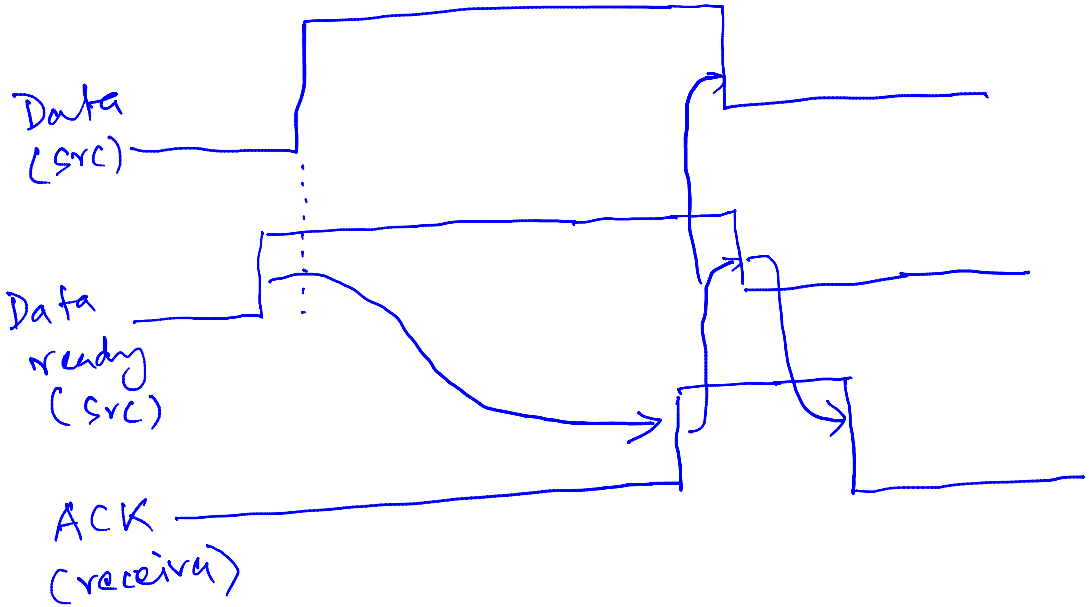
One-Way Receiver Initiated



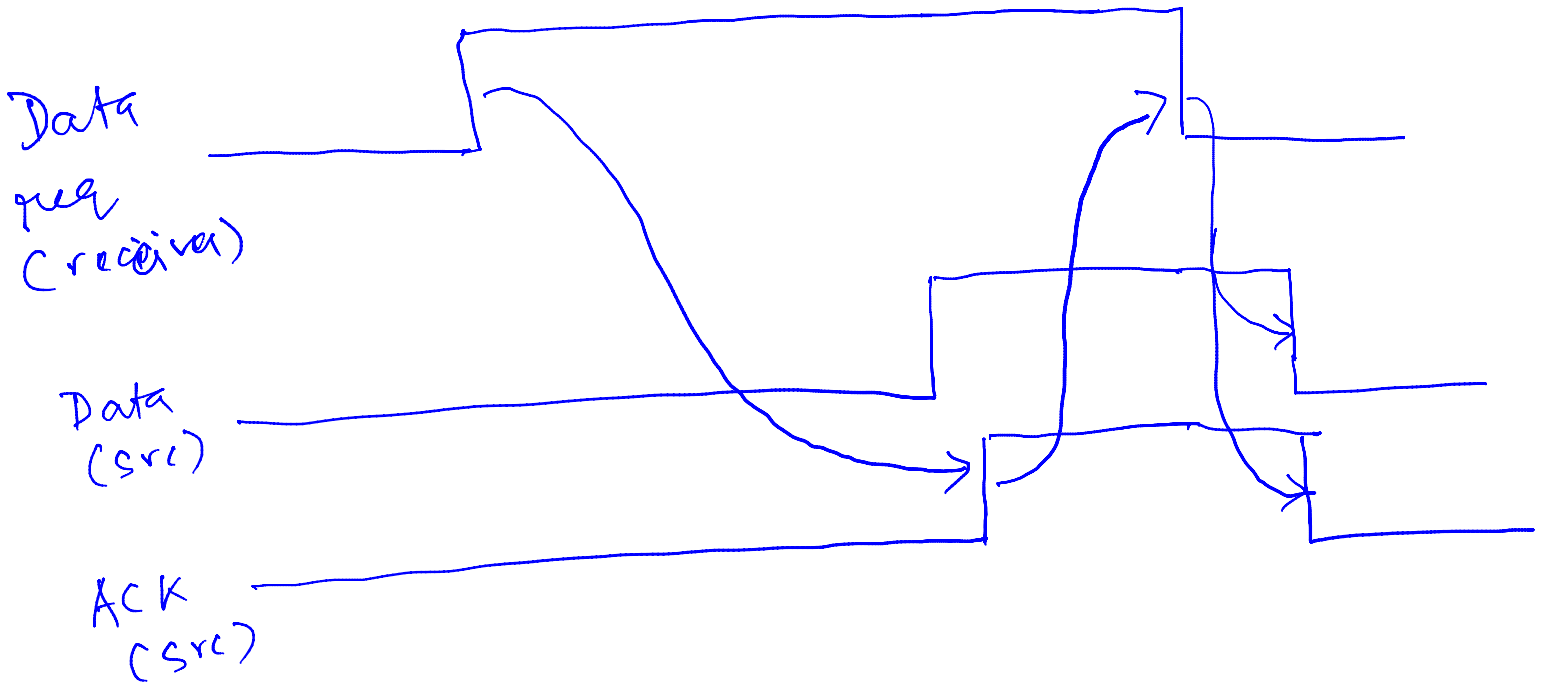
One-Way Asynchronous Transactions: Remarks

- Data ready, data request lines also called “strobe” lines
  - Cause data to flow onto the bus
  - “Strobes” the data from/to bus
- Disadvantages:
  - Destination or source may not be ready, or may be slow
  - Transaction results in error
  - Worse, no one knows about it!
- Two-way: use ACK line

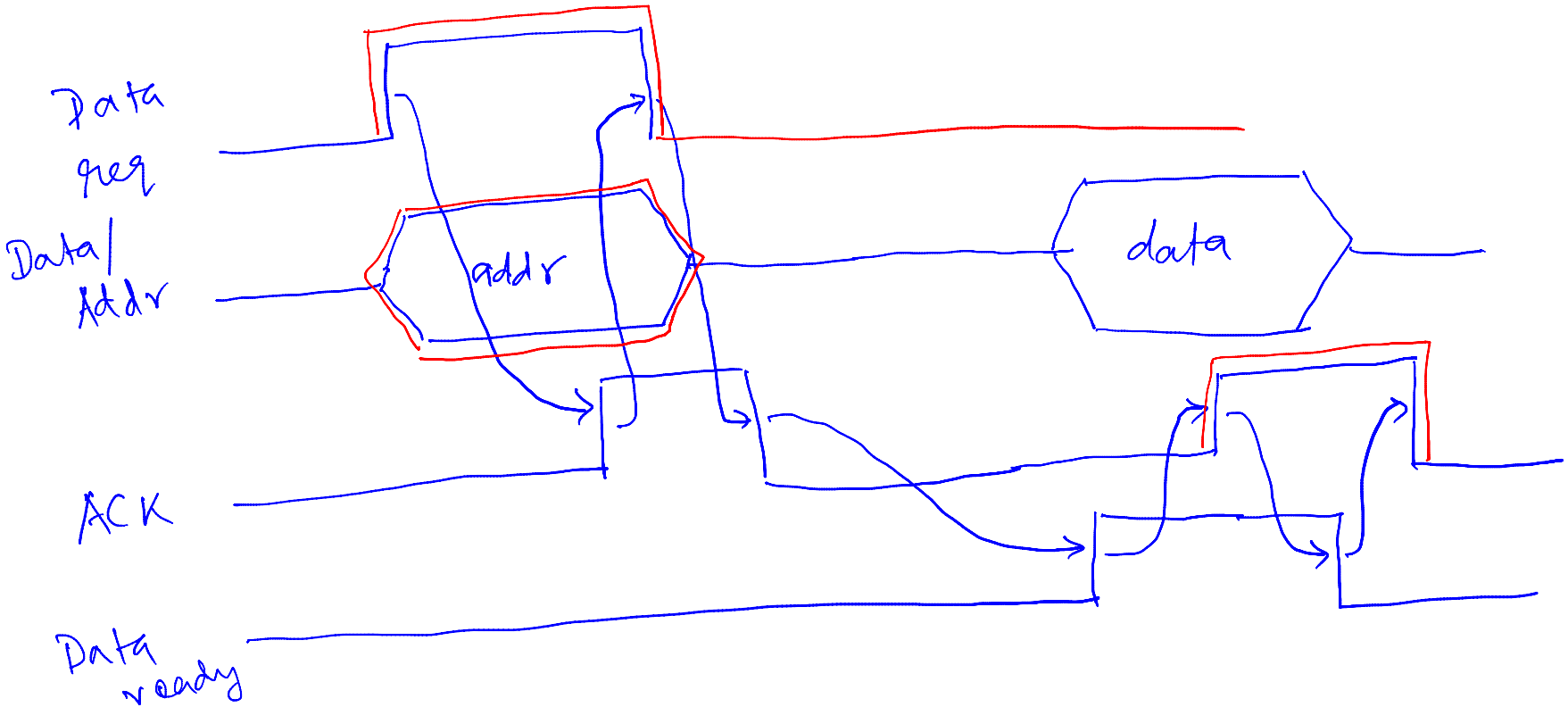
Two-Way Source Initiated



Two-Way Receiver Initiated



A Memory-Read Transaction



Synchronous vs Asynchronous Transactions

Synchronous

- Simple protocol
- Extra clock line
- Bus length restricted for fast clocks (sync error grows with distance)
- Not all devices may be able to operate at same speed: clock operates at speed of slowest device

Asynchronous

- Protocol somewhat complex
- No extra clock line
- No bus length restriction due to clock line
- Can interface with slow as well as fast devices