Q1. block size = 16 words.
miss rate = 0.25 % = 1/400 = r
CPI w/o miss = 2.5

DRAM Latency : a : comm ador : 2
b : accers : 20
c : comm data : 2

assuming : no early start policy
X - wide mem ⇒ bus size = X ~~words~~
Granuality of access is X

w/o interleaving
$$CPI = 2.5 + r * \frac{blocksize}{X} * (a+b+c)$$

with interleaving
$$CPI = 2.5 + r * \left(a+b+c * \frac{blocksize}{X}\right)$$

(a) X = 1 w/o interleaving $CPI = 2.5 + \frac{1}{400} \cdot \frac{16}{1} \cdot (24)$
$= 2.5 + 0.96 = \underline{3.46}$

with inter: $CPI = 2.5 + \frac{1}{400}(22 + 16(2)) = 2.5 + 0.135$
$= \underline{2.635}$

(b) X = 2
w/o interleaving: $CPI = 2.5 + \frac{1}{400} \cdot 8 \cdot (24) = 2.5 + 0.48$
$= \underline{2.98}$

with inter : $CPI = 2.5 + \frac{1}{400}(22 + 8*2) = 2.5 + 0.095$
$= \underline{2.595}$

(c) X = 4 w/o int : $CPI = 2.5 + \frac{1}{400} \cdot 4 \cdot (24) = 2.5 + 0.24 =$
$= \underline{2.74}$

with int : $CPI = 2.5 + \frac{1}{400} \cdot (22 + 4*2) = 2.5 + 0.075$
$= \underline{2.575}$

(d) Y = 8 w/o int : $CPI = 2.5 + \frac{1}{400} \cdot 2 \cdot (24) = 2.5 + 0.12$
$= \underline{2.62}$

with int : $CPI = 2.5 + \frac{1}{400}(22 + 2*2) = 2.5 + 0.065$
$= \underline{2.565}$

Q2. Half of instr. have data access

processor	cache type	block size (word)	instr miss rate (imr)	data miss rate (dmr)
P_1	DM	1	4 %	6 %
P_2	DM	4	2 %	4 %
P_3	2-way set	4	2 %	3 %

cache miss penalty = 6 + block size (words)

measured CPI (P_i) = 2.0.

(a) measured CPI = ideal CPI + $\left(imr + \frac{dmr}{2}\right)$ * miss penalty.

for P1

$2 = \text{ideal CPI} + \frac{4}{100} \times 7 = \text{ideal} + 0.49$

ideal CPI = 1.51

(b).

P_2: miss penalty = 6 + 4 = 10

$imr + \frac{dmr}{2} = 4\%$

$CPI = 1.51 + \frac{4}{100} * 10 = 1.91$

for P_3

(c) not enough data to compute effect of associativity on hit time → CPI and overhead via block eviction policy

[→ assuming there to be negligible for this prob.

P_3: miss penalty = 6 + 4 = 10.

$imr + \frac{dmr}{2} = 3.5\%$.

$CPI = 1.51 + \frac{3.5}{100} \times 10 = 1.86$

. P_3 is the fastest.

Note: number of blocks in set must be 3 x 2^k so that number of sets in cache is a power of 2, and also number of words in block is a power of 2

Q3. Cache size = 3K

- to calculate offset ~~# of~~ blocksize must be power of 2

(a) for D.M. and 2-way set ~~#blocks/sets must be~~ # sets in cache is not power of 2 hence both not possible with simple bit extrations.

(b) fully associative max blocksize = 1K words

(c) blocksize = 1K words = $4 \times 2^{10} = 2^{12}$ bytes.

mem addr field