

# CS305

## Computer Architecture

### Data Hazards in the Pipeline

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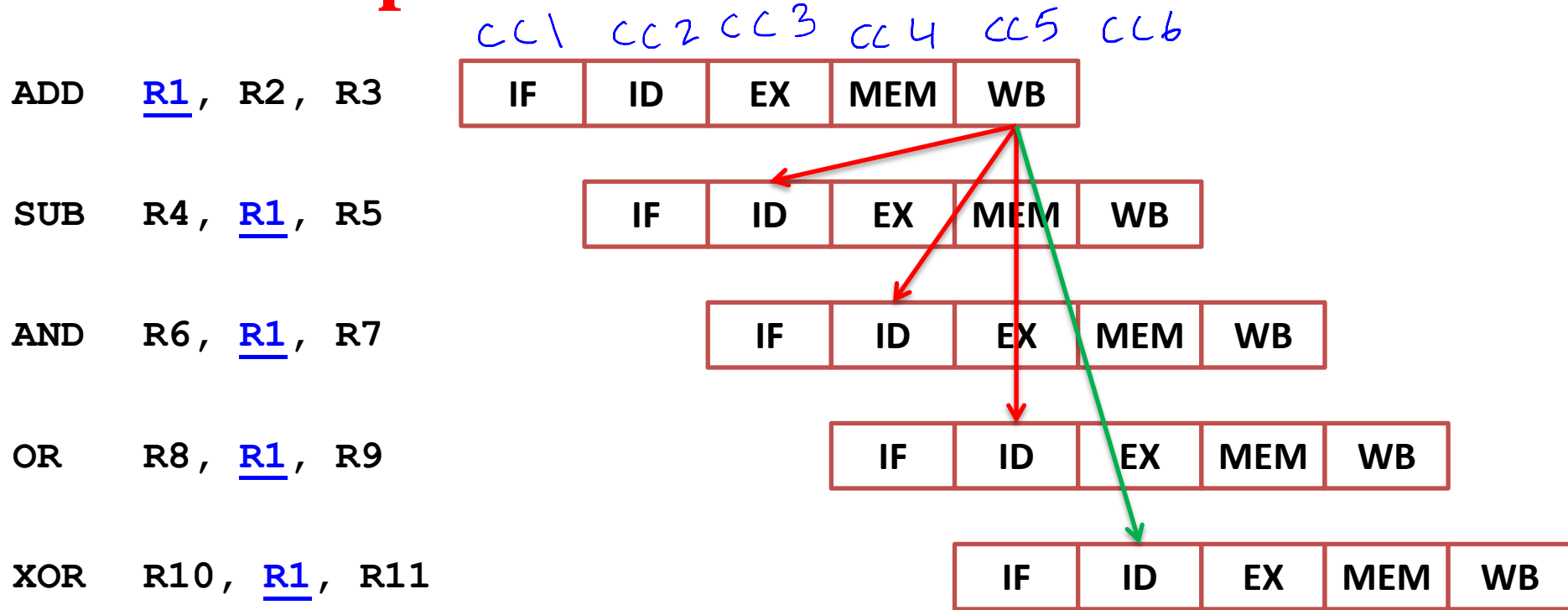
Structural  
→ Data  
Control

<http://www.cse.iitb.ac.in/~br>

# Data Hazards

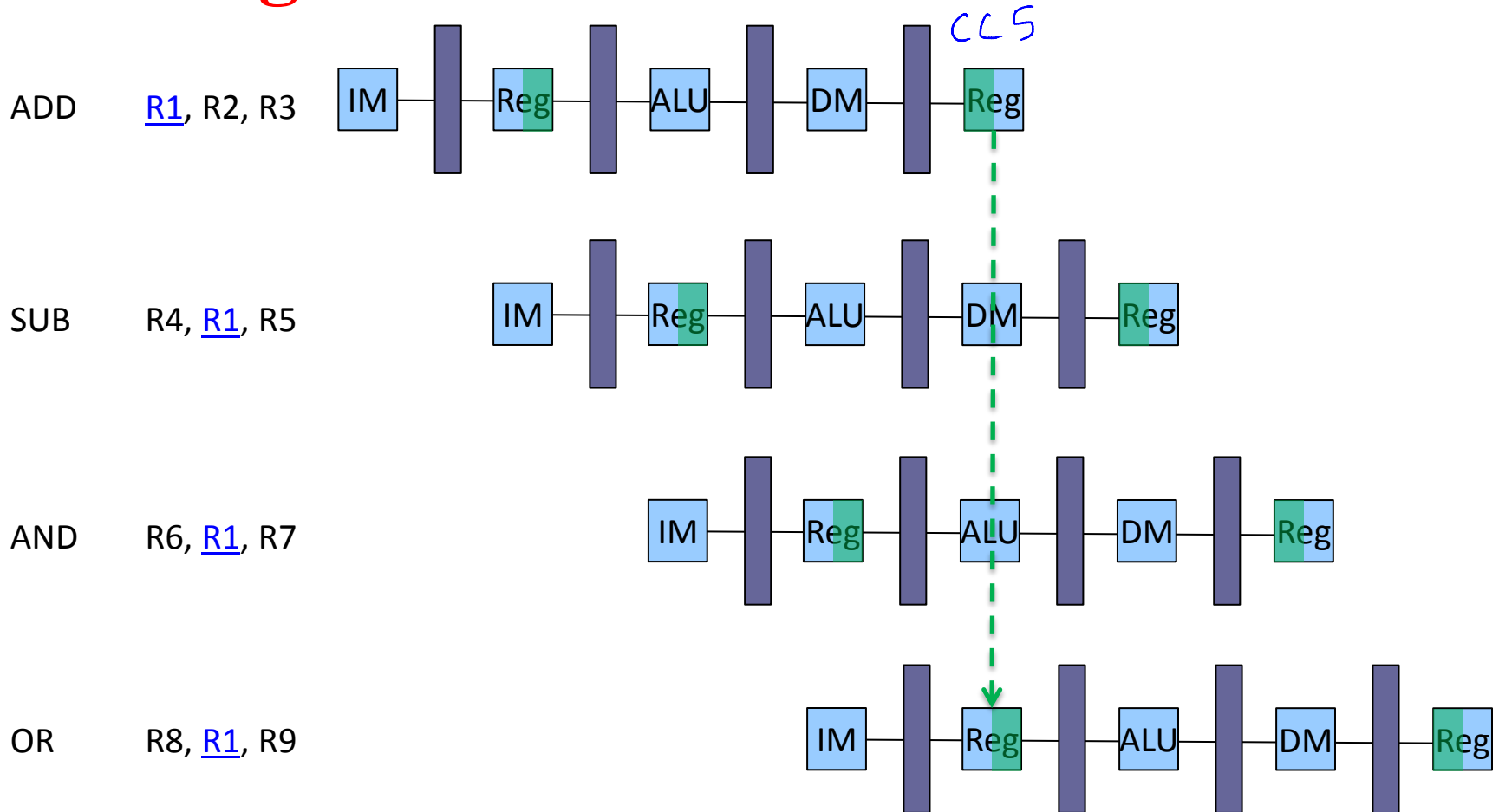
- Data dependence across instructions → data hazard
  - Register dependence
  - Memory dependence
- Example (DLX instruction set):
  - ADD R1, R2, R3
  - SUB R4, R1, R5
  - AND R6, R1, R7
  - OR R8, R1, R9
  - XOR R10, R1, R11
- All instructions after ADD depend on R1

# Pipeline With Data Hazards

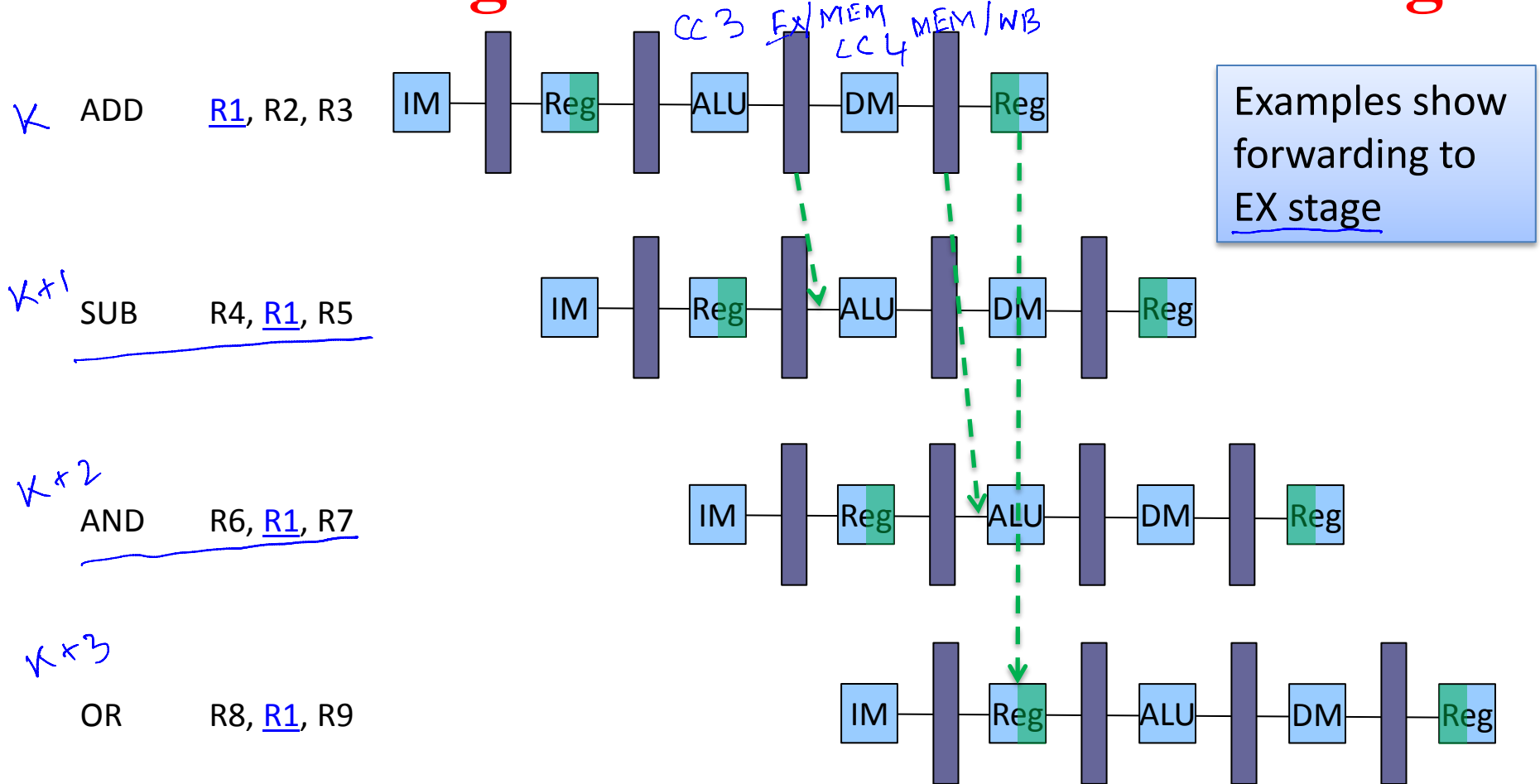


Data hazard: normal pipelined execution will produce **WRONG** result!  
Solution? Can stall. Can we do better?

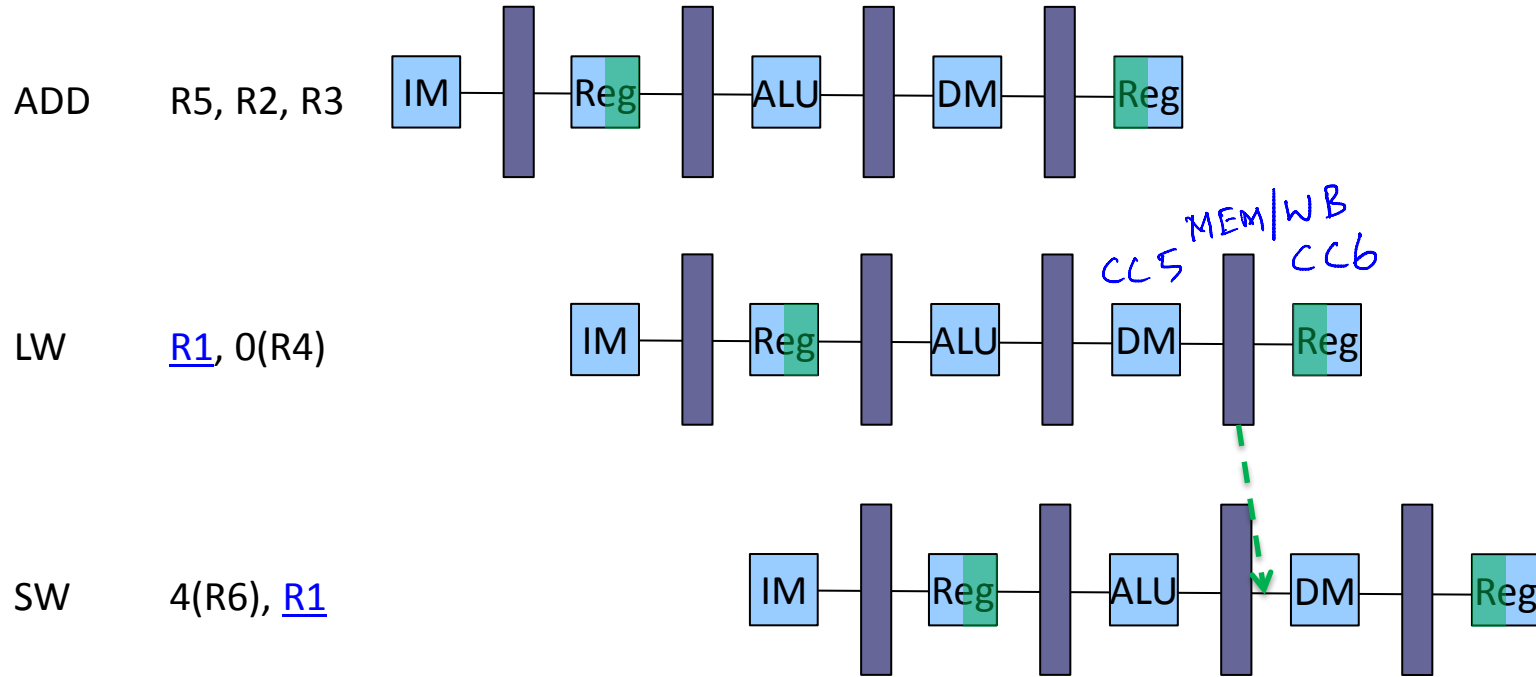
# Register File: Reads after Writes



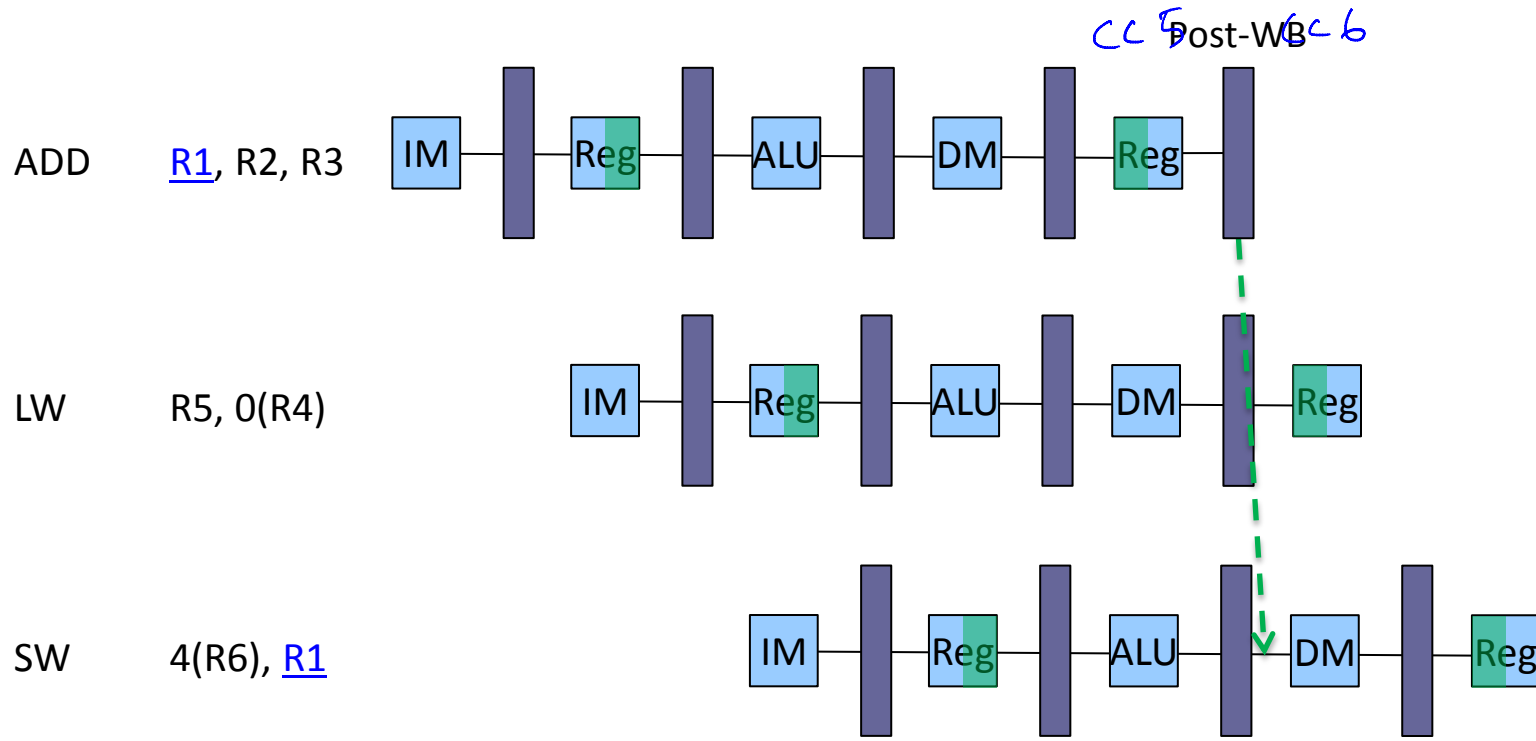
# Minimizing Stalls via Data Forwarding



# Data Forwarding to MEM Stage



# Data Forwarding to MEM Stage (continued)



# Memory Data Hazards

- Not possible in MIPS
  - Memory operations always happen in order

→ SW R1, X  
→ LW R2, X



# Data Hazard Classification

- **Read after Write (RAW):** use data forwarding to overcome
- **Write after Write (WAW):** arises only when writes can happen in different pipeline stages

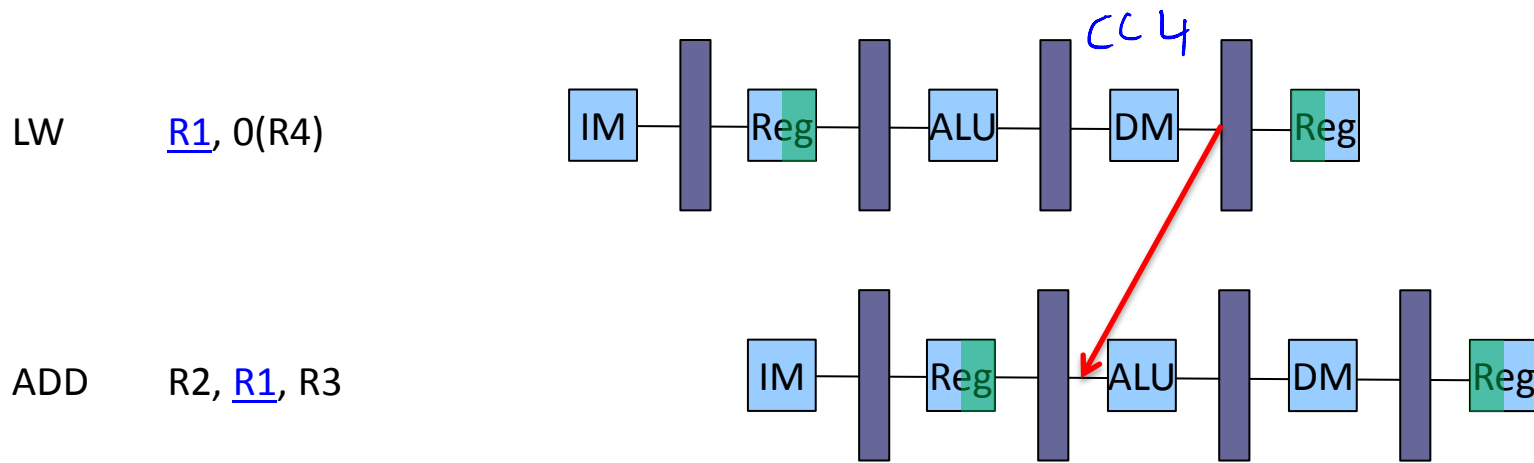
	CC1	CC2	CC3	CC4	CC5	CC6
LW <u>R1</u> , 0 (R2)	IF	ID	EX	MEM1	MEM2	WB
ADD <u>R1</u> , R2, R3		IF	ID	EX	WB	

- Has other problems as well: structural hazards

- **Write after Read (WAR):** rare

	CC1	CC2	CC3	CC4	CC5	CC6
SW R1, 0 ( <u>R2</u> )	IF	ID	EX	MEM1	MEM2	WB
ADD <u>R2</u> , R4, R3		IF	ID	EX	WB	

# Data Dependence Requiring a Stall




**All data forwarding, stalling require control logic  
(reason for complexity in control)**

# Compiler's Role in Avoiding Stalls


```
a = b + c;  
d = e + f;
```

## Naïve compiler



```
LW    R1, b  
LW    R2, c  
ADD   R4, R1, R2  
SW    a, R4  
LW    R10, e  
LW    R11, f  
ADD   R12, R10, R11  
SW    d, R12
```

## Clever compiler



```
LW    R1, b  
LW    R2, c  
LW    R10, e  
ADD   R4, R1, R2  
LW    R11, f  
SW    a, R4  
ADD   R12, R10, R11  
SW    d, R12
```

CPI without clever code scheduling =  $1 + F_{\text{loads-causing-stalls}}$

# Summary

- Data hazard: data dependence
  - MIPS: only RAW dependence in registers
  - Still, can have stall
- Need control logic for:
  - Data forwarding
  - Stalling