CS305
Computer Architecture

Virtual Memory and Caches

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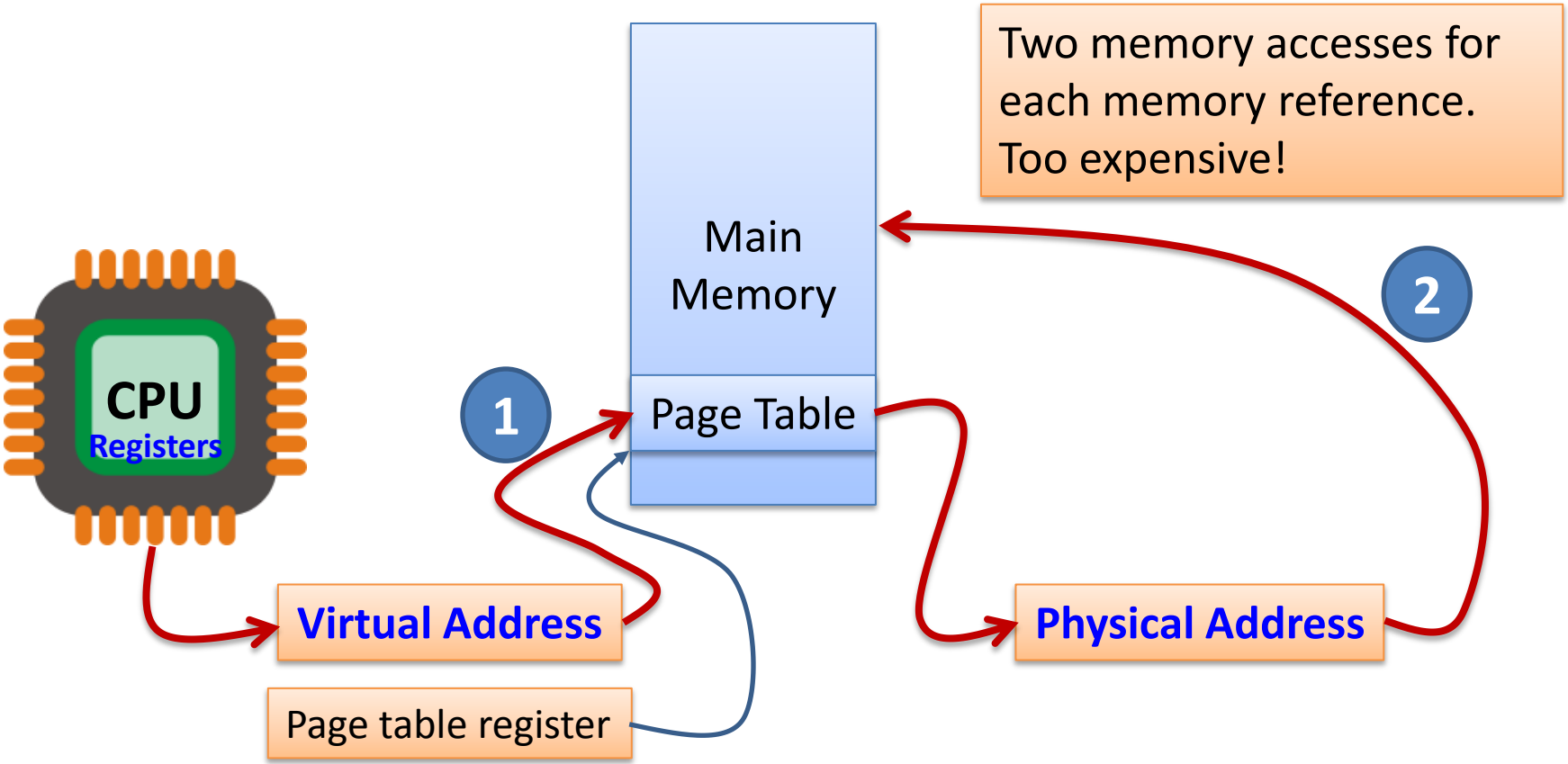
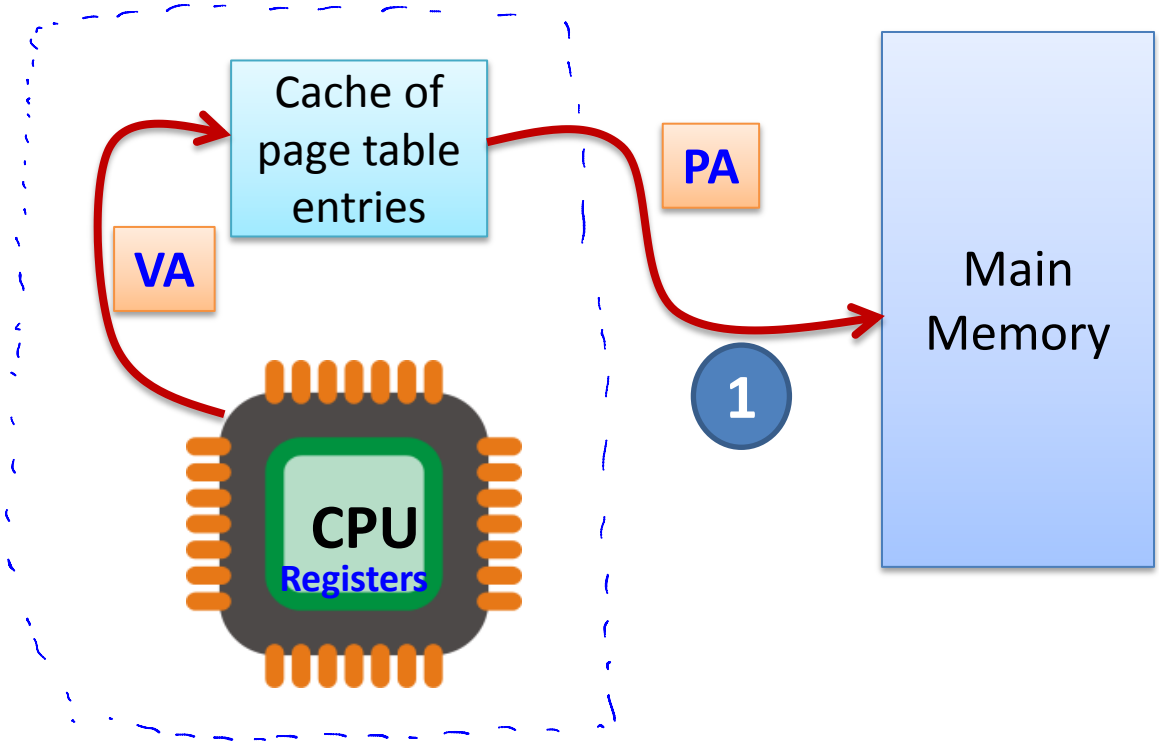
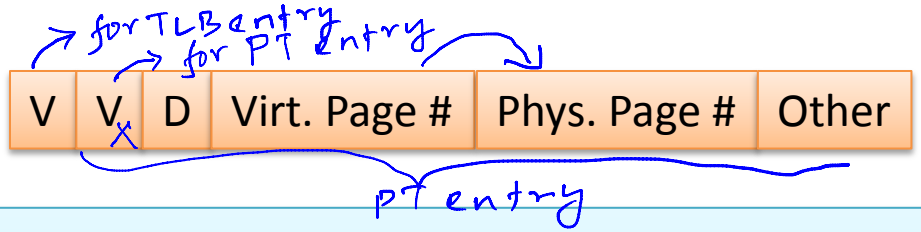
What Happens on a Memory Reference?



Solution: Caching!



Translation Look-aside Buffer (TLB)



- TLB is on-chip
- Unified or separate
- Fully associative and small, or larger with lower associativity
- Cache replacement policy: can't be as sophisticated as for pages
- Some typical parameters:
  - TLB size: 16-512 entries
  - Block size: 1-2 entries (4-8 bytes each)
  - Hit time <= 1 cycle, TLB access = 1 pipeline stage, if hit time = 1 cycle
  - Miss penalty = 10-100 cycles, miss rate = 0.01-1%
- TLB miss may be handled in hardware or software

Possible Sequence of Events

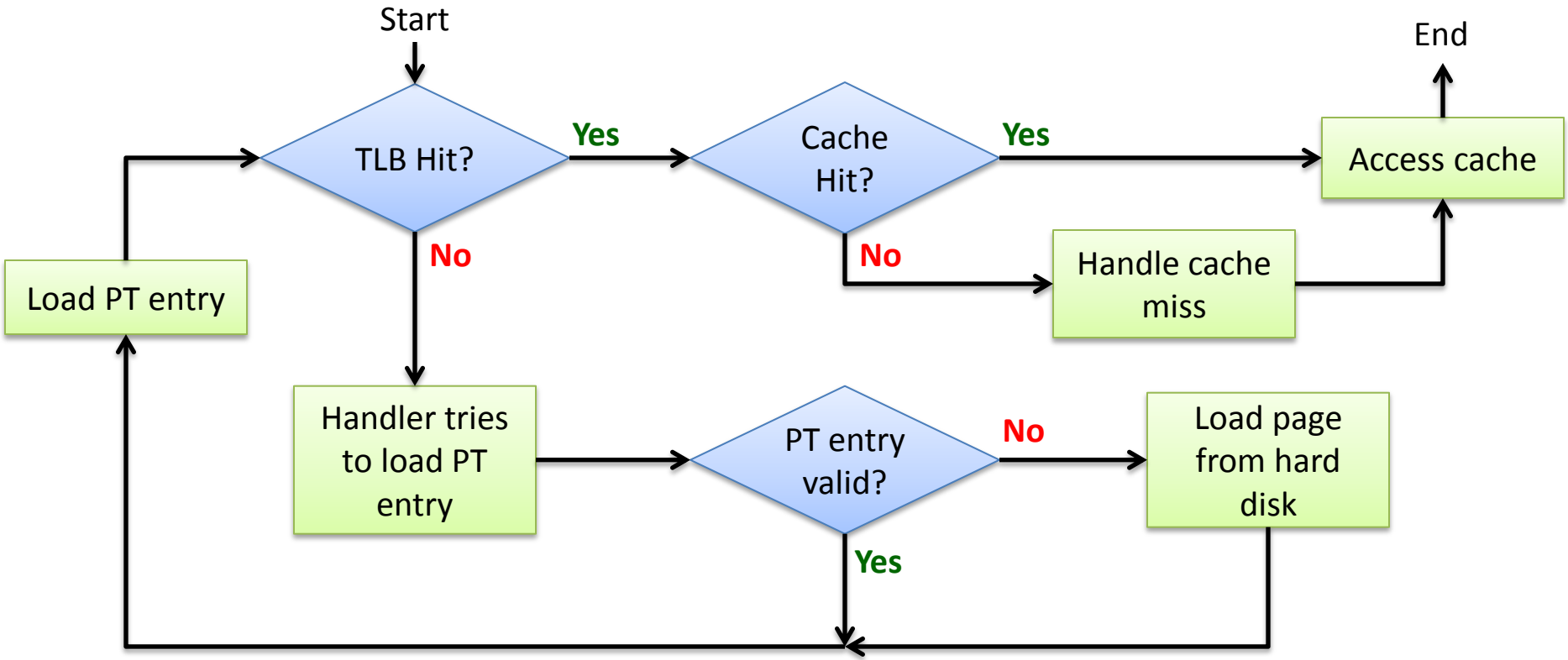


Table of Possibilities

TLB	PT	L1	Remarks
Hit	Valid	Hit	Best case
Hit	Valid	Miss	Only cache miss
Miss	Valid	Hit	Only TLB miss
Miss	Valid	Miss	TLB miss, then cache miss
Miss	Invalid	Miss	Worst case
x	Invalid	Hit	Not possible
Hit	Invalid	x	Not possible

Putting it all Together: A Numeric Example

64-bit VA space, 16GB main memory, 32KB page size
Page table entry: mapping, 16-bit disk addr, bits: valid, used, dirty, write protection
TLB has 16 entries

Q: Compute page table size, indicate fields of VA, PA

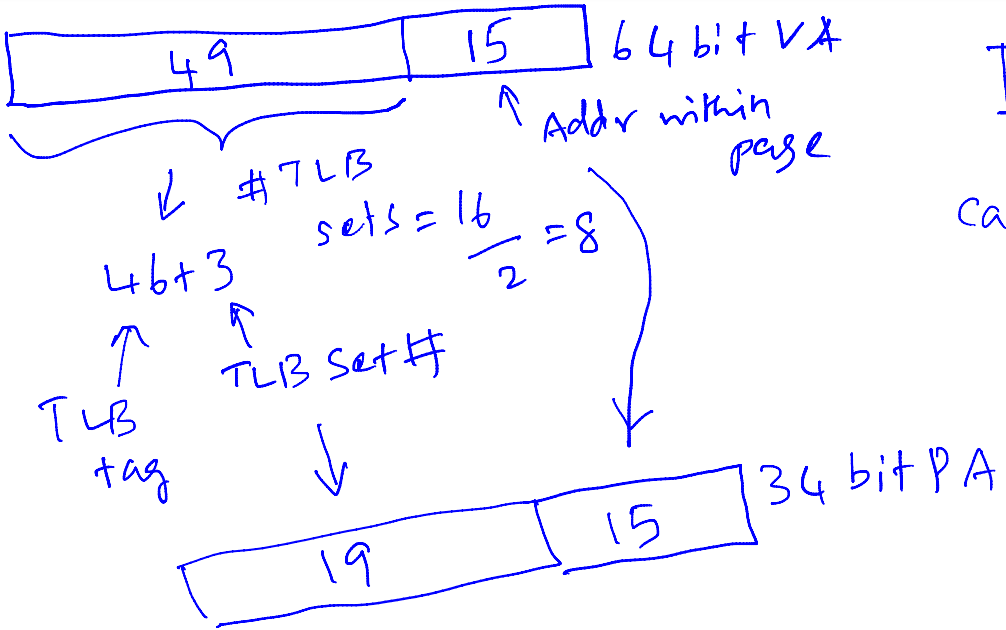
A: # virtual pages = $2^{64}/2^{15} = 2^{49}$, # physical pages = $2^{34}/2^{15} = 2^{19}$
Page table entry size = 19 bits for physical page # + 16 + 4 = 39
Page table size = 2^{49} x 39 bits

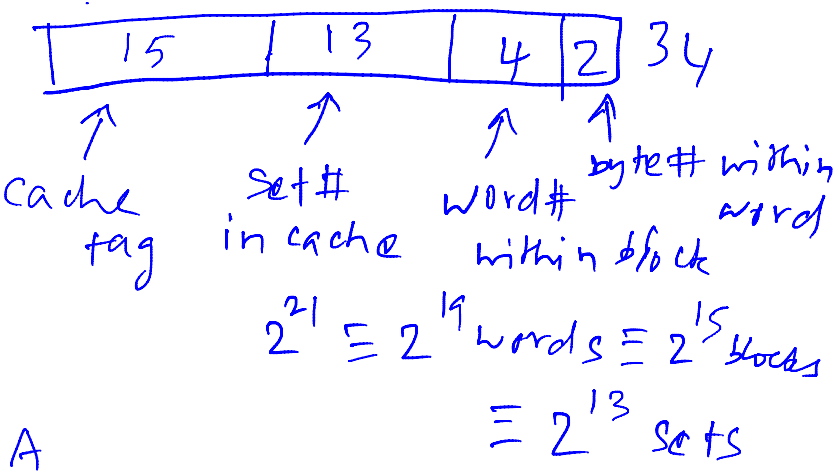
Q: Compute TLB size

A: TLB has 49 bit virt page #, 19 bit phys page #, use bit (for page), use bit (for TLB), valid bit (for TLB), write protect bit (for page), dirty bit (for page), dirty bit (for TLB)
Total = (49+19+6) x 16 = 74 x 16 = 1184 bits

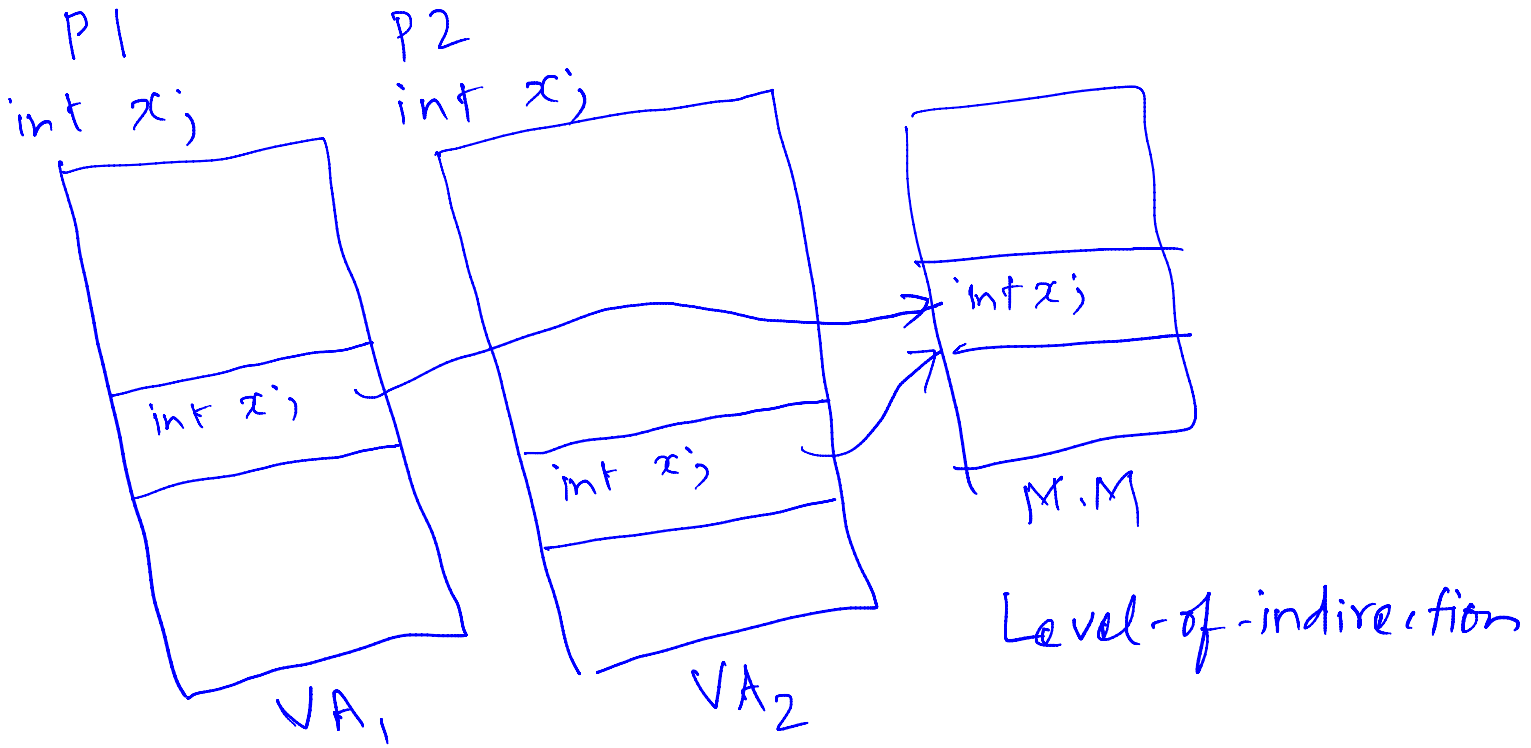
Numeric Example (Continued)

TLB is 2-way set associative
L1 cache: 2MB, 16-word block, 4-way set associative
Show bit manipulations during a particular memory access

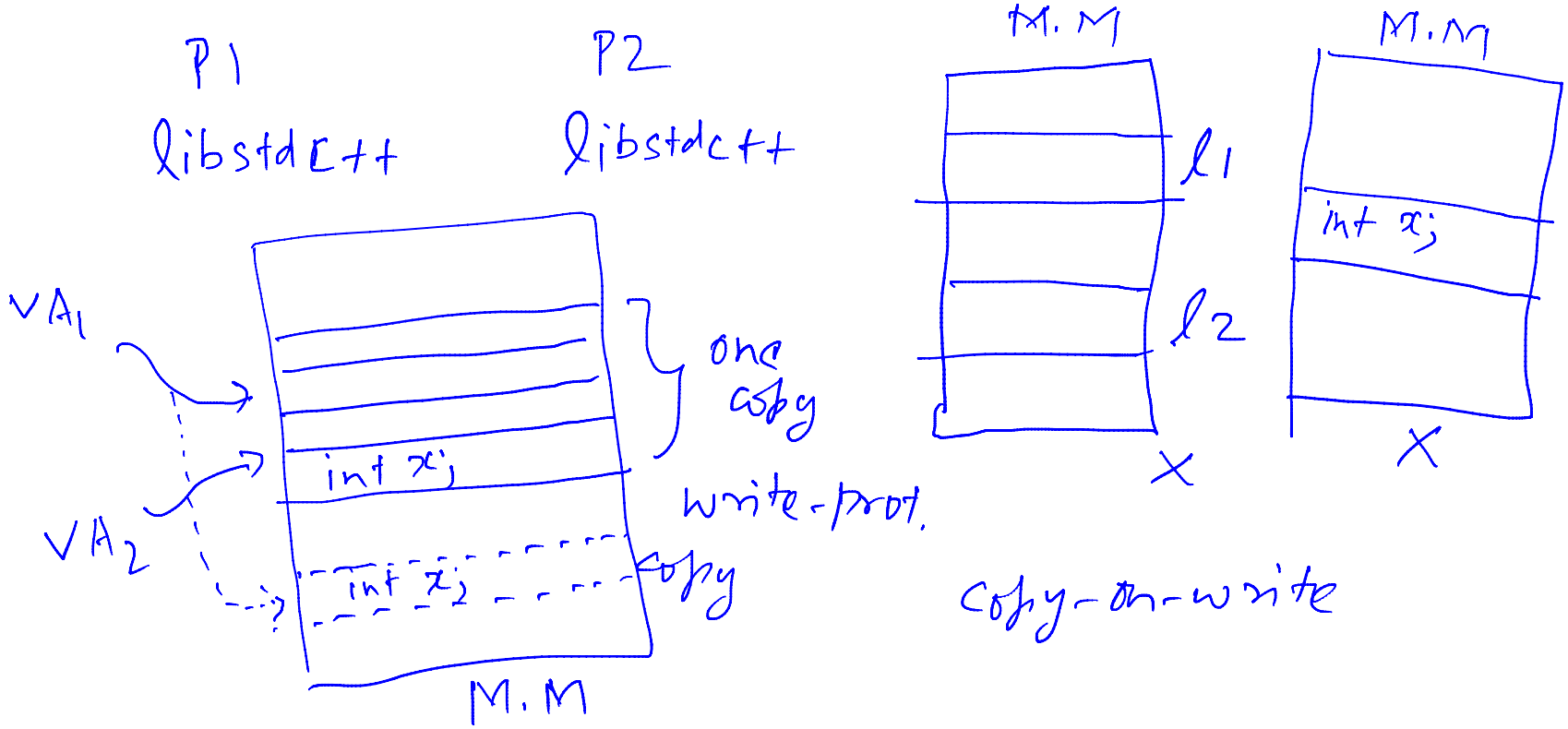




Shared Memory Using Virtual Memory



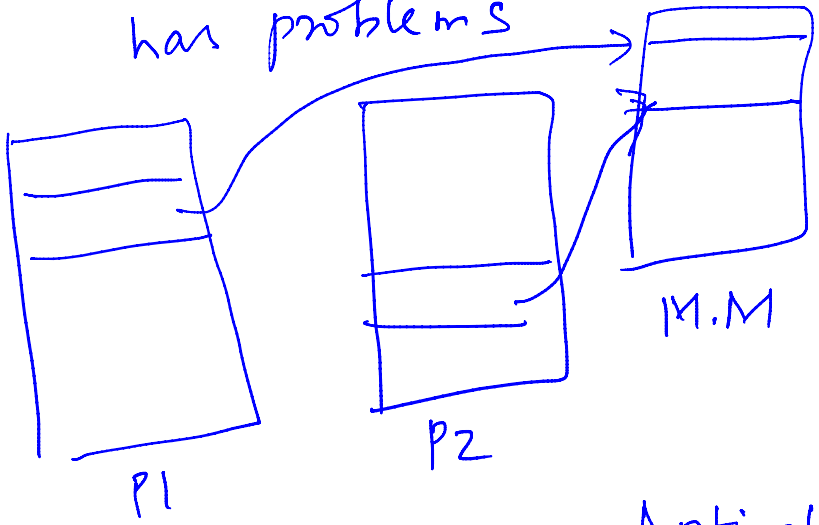
Copy-on-Write Using Virtual Memory



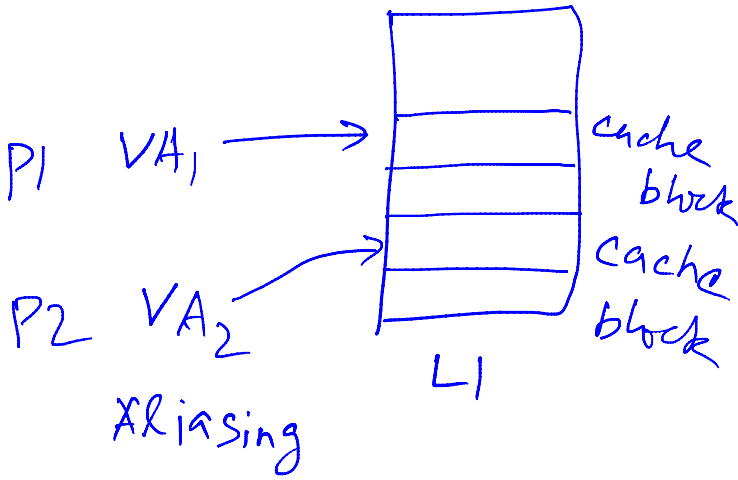
Virtually Addressed Caches

(+) cache hit ⇒ VA→PA translation unnecessary

(−) shared mem has problems



Anti-aliasing



Aliasing

Summary

- TLB: cache for PT entries
- Caches in the memory system: TLB, L1, L2, L3, MM
  - Others too: disk is cache for network access, web proxy is cache for server content
- Features using VM: shared memory, copy-on-write
- Next: hardware and OS interaction for VM