Q1 diff blu regesters and L1 cache as eache Solutions provided by Swatej

- · CPU con only directly across regiesters (as it is post of CPU) register memory is much smaller three faster across
- · Data loaded in registers is dictated by program . Unike UI cache. This is the main/important/conceptual difference
- Q2. Cache is SRAM, smaller, dozer to CAU hence making it farter than main memory (DRAM)

		11.	nemony =  ck sdze =  e memony =  mad  mad	23 6100	1/2 DM s caclus [7/2]1.
word	Ħ	cach	e # tag	hit Imiss	12/2/1/2
2		١	0	miss	0 1 2 3 4 5 6 7
3		١	0	hit	tags * * * *
11		15	0	miss	1 1 0 0 *
16		٥	1	miss	
21	(0	2	•	miss	
13	6	6	0	ćzím	
64	32	0	4	miss	
	24	0	उ	miss	,
19	9	1	1	miss	
u	5	5	0	hit	
3		١	0	mi ss	
	11	3	(	miss	
	2	2	0	miss	
	13	5	١	miss	
	3	3	6	miss	

miss

Q4 main memory = 1024 words. = 2 words Size # blods in = 29 # blocks in cardre = 23 would be some as Q3 since the soq, 9's some just tay size would be larger by 2 675. 7 05. manin manong = 32 MB = 210. 210. 25 = 225 bytes Cache size = 5/2 KB = 210, 29 = 219 bytes.

block size = 16-word = 29. 22 = 26 bytes. to blocks in cache = 2 19/26 = 213 Assuming an need walid, durty into. 25-(13+6) merron

block H In cache tag

o hits companator

2

b



