# CS305
# Computer Architecture

## Extending the Single Cycle MIPS Implementation

reg-reg
lw, sw
beq

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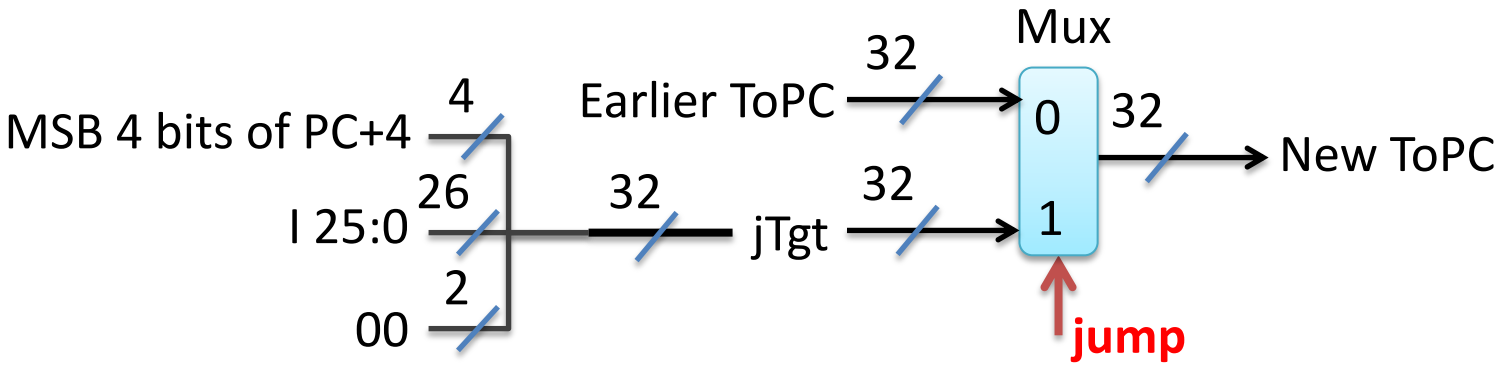
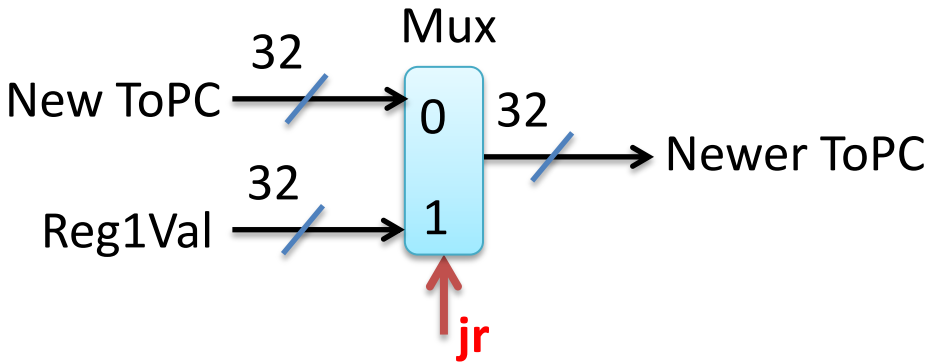
# Data Path, Control Path Extensions to Support `j`



# Main Control Unit Truth Table Enhancement

| | RegDst | RegWr | ALUSrc | Mem-Rd | Mem-Wr | Mem2-Reg | Bran-ch | ALU-Op2 | Jump |
|---|---|---|---|---|---|---|---|---|---|
| Reg-Reg | Rd (0) | 1 | Reg2Val (0) | 0 | 0 | ALUOut (0) | 0 | 10 | 0 |
| lw | Rt (1) | 1 | SgnExt-Imm (1) | 1 | 0 | MemOut (1) | 0 | 00 | 0 |
| sw | x | 0 | SgnExt-Imm (1) | 0 | 1 | x | 0 | 00 | 0 |
| beq | x | 0 | Reg2Val (0) | 0 | 0 | x | 1 | 01 | 0 |
| j | x | 0 | x | 0 | 0 | x | x | x | 1 |

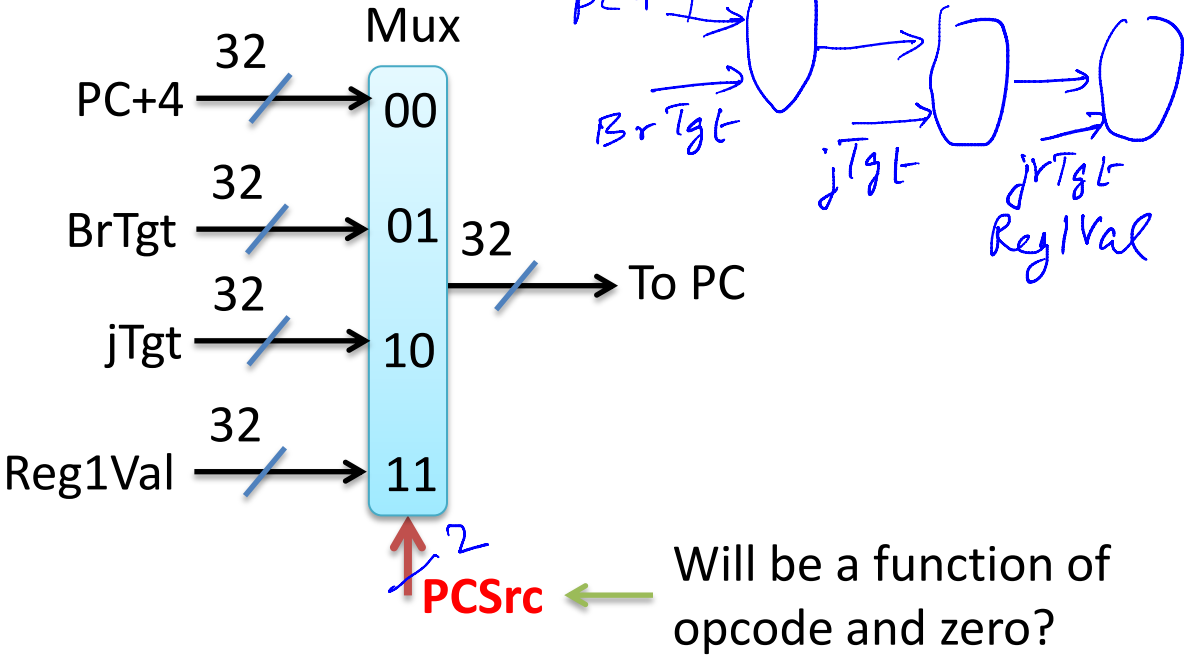
# Further Data Path, Control Path Extensions to Support `jr`



# Main Control Unit Truth Table Enhancement

| | Reg-Dst | Reg-Wr | ALUSrc | Mem-Rd | Mem-Wr | Mem2-Reg | Bran-ch | ALU-Op2 | Jump | Jr |
|---|---|---|---|---|---|---|---|---|---|---|
| Reg-Reg | Rd (0) | 1 | Reg2Val (0) | 0 | 0 | ALUOut (0) | 0 | 10 | 0 | 0 |
| lw | Rt (1) | 1 | SgnExt-Imm (1) | 1 | 0 | MemOut (1) | 0 | 00 | 0 | 0 |
| sw | x | 0 | SgnExt-Imm (1) | 0 | 1 | x | 0 | 00 | 0 | 0 |
| beq | x | 0 | Reg2Val (0) | 0 | 0 | x | 1 | 01 | 0 | 0 |
| j | x | 0 | x | 0 | 0 | x | x | x | 1 | 0 |
| jr | x | 0 | x | 0 | 0 | x | x | x | x | 1 |

# Alternate Data Path, Control Path Modification to Support `j, jr`



# Summary

- The data-path and control-path can be extended to support further instructions
  - In some cases, original data-path, control-path must be modified
- Understand general principle before proceeding
  - Identify hardware component(s) for instruction
  - String them together, enhance data-path, control-path
  - Enhance/modify main control unit (truth table)