CS230: Digital Logic Design and Computer Architecture
Tutorial 10, [Mon 28 Oct, Tue 29 Oct]

1. Consider a virtual memory system with virtual byte address = 40-bits, physical byte address = 36-bits, and page size = 16 KB.

   (a) Draw a diagram to show the virtual-to-physical address mapping. Show the various fields of the virtual and physical addresses.

   (b) In the default page table scheme, what is the total size of the page table for each process? Assume that a page-table entry has a 32-bit disk address, in addition to 4 meta-data bits (the valid, write protection, dirty, and use bits), apart from the fields necessary for the virtual address to physical address mapping.

2. **Multi-level page tables:** A computer has a 32-bit virtual address space, and a 24-bit physical address space. It has 8KB pages. Suppose a 2-level page table arrangement is used. It is convenient to arrange the second level page tables to be of the same size as a page. With this arrangement, and assuming that each page table entry is of length 4 bytes, answer the following. Show brief calculations/steps/explanations.

   (a) How many memory accesses will a jal instruction produce?

   (b) How many memory accesses will a lw instruction produce?

   (c) What is the size of the per-process first-level page table?

   (d) Draw a diagram to show how a virtual address is translated to a physical address in this arrangement.