CS230 **Name:** _____
Quiz-II
13th March 2023
Time Limit: 120 minutes **Roll No.:** _____

"Once I learn how to use Google, isn't that all the education I really need?"

Google, nah, it is old. Now, it is the time for ChatGPT.

This exam contains 12 pages and 3 questions. Maximum points: 50

Tips:
All the questions are compulsory.
Be concise and cognizant and write your answers inside the boxes provided.
There will be a penalty for verbosity.
Do not spend too much or too little time on any particular question.
Use additional sheets for the rough work.
Make sure you have done all the calculations correctly. Later, we wont be able to entertain any "just two becomes three else all are correct, give me marks" kind of cribs.

"I promise I will write this exam honestly and ethically"
Your Signature:

`You must be kidding!!`

1. (24 points) [`50 minutes`] True/False questions. Respond with T or F with few lines of justification. Response without a justification will lead to zero points and no cribs will be entertained.

   (1.1) (2 points) Four multiply by four divided by four is four :)

4

(1.2) (2 points) If a processor receives an interrupt while executing an instruction pointed by PC, then after handling interrupts, the interrupt handler goes to the PC, again.

False, it will go to PC+4

(1.3) (2 points) A 5-stage pipelined simulator simulating millions of instructions has the following code flow.

```
main ()
{
while(true)
{
fetch ();
decode ();
execute ();
memory ();
writeback ();
cycle++;
}
}
```

Yashwant claims that the simulator correctly simulate a pipelined processor. Defend whether Yashwant is right or wrong and why.

False, the order should be other way around :)

(1.4) (2 points) A program has four instructions that can occupy a branch delay slots, which are as follows in the program order:
I1: ADD R2,R7,R8
I2 : SUB R4, R5, R6
I3 : ADD R1, R2, R3
I4 : STORE Memory [R4], [R1]
BRANCH to Label if R1== 0
I1 can occupy the branch delay slot without affecting the program semantics (the output of the program will still be the same). Note that for I1, I2, and I3, R2, R4, and R1 are the destination registers. For I4, the content of R1 is getting stored into a memory address that is pointed by R4.

False, We cannot move I1 as I3 is taking the value of I1

(1.5) (2 points) Branch predictor is probed in the fetch stage of the instruction pipeline and a BTB hit indicates that a PC is a branch PC.

Yes, so that control hazard penalty should be zero.

(1.6) (2 points) Variable length ISAs complicate the decode stage of the pipeline but alignment helps in much simpler pipeline designs.

Yes, as the decoder circuit gets complicated and alignment helps in reducing memory accesses and all.

(1.7) (2 points) For a local history branch predictor where the Branch History Table has 1024 entries, each 3 bits in length, and the Pattern History Table consists of a standard 2-bit predictor. The total storage required for the entire PHT is 8 bits. You are not supposed to assume anything else from the question.

False, Answer 16 bits, 3 bits of BHT entry will lead to eight entries each of two bits, so 16 bits

(1.8) (2 points) A hypothetical pipeline that uses predict-not-taken branch prediction has a 3-cycle branch misprediction penalty. On average, if 65% of all branches are taken on this design while running a hypothetical program, then the CPI will be 3.05.

False, Answer: 2.95
1+ 0.65*3 = 2.95

(1.9) (2 points) A 10-stage pipelined CPU sees 20% of instructions as branches. The CPU uses a 1-bit branch predictor with 50% accuracy. Assuming the target information is computed in the EX stage of the pipeline, The speedup that can be achieved with this 10-stage pipelined CPU compared to a single-cycle non-pipelined CPU is 9.22.

False, Answer: 10/(1+0.2*0.5*2) = 10/1.2 = 8.33, assuming 2 stage penalty, if they assume EX stage is Kth stage, then the penalty should be K-1 cycle and not 2 cycles. We will also give full marks if the answer says "not enough data".

(1.10) (2 points)
```
int i=0;
while(1)
{
if(i%2)
cout << welcome to quiz-2 << endl;
i++;
}
```

The accuracy of the last-time (one-bit) branch predictor that starts with the TAKEN state, while predicting the outcome of the "if" statement is 0.5.

False, it will be zero.

(1.11) (2 points) RAW hazards can be completely eliminated by bypassing/forwarding whereas control hazards cannot be eliminated with 100% for branch prediction accuracy with BTB hit rate of 100%.

False, should be other way

(1.12) (2 points) Instruction pipelining improves instruction throughput but at the cost of latency per instruction.

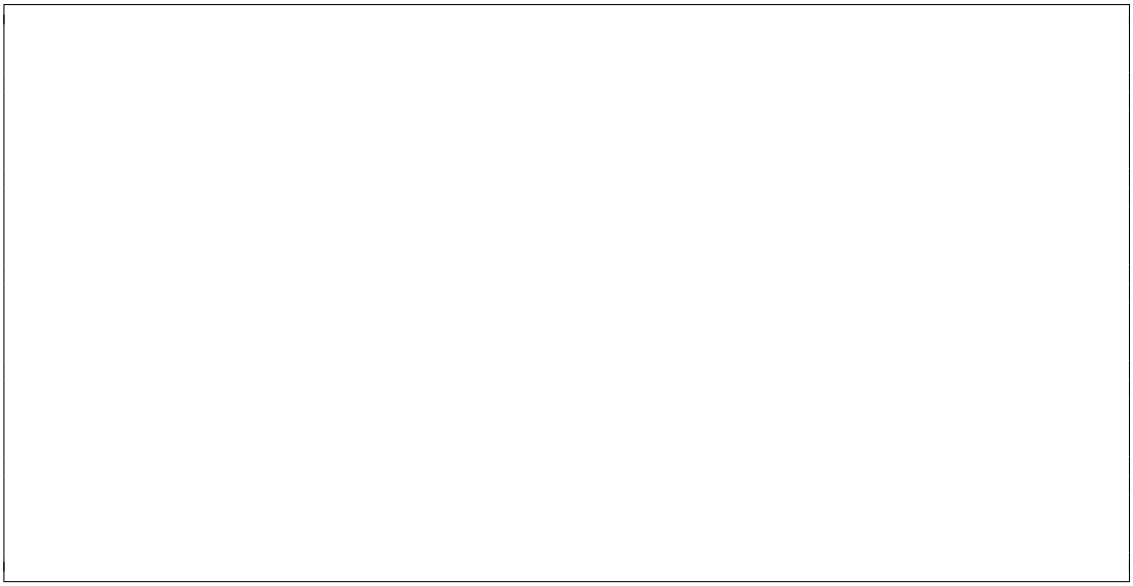
True

Oh man, so many questions :(I just do not like writing these exams. Anyways, run Forest run :)

`Exaaaaaaammmmmmm!!`

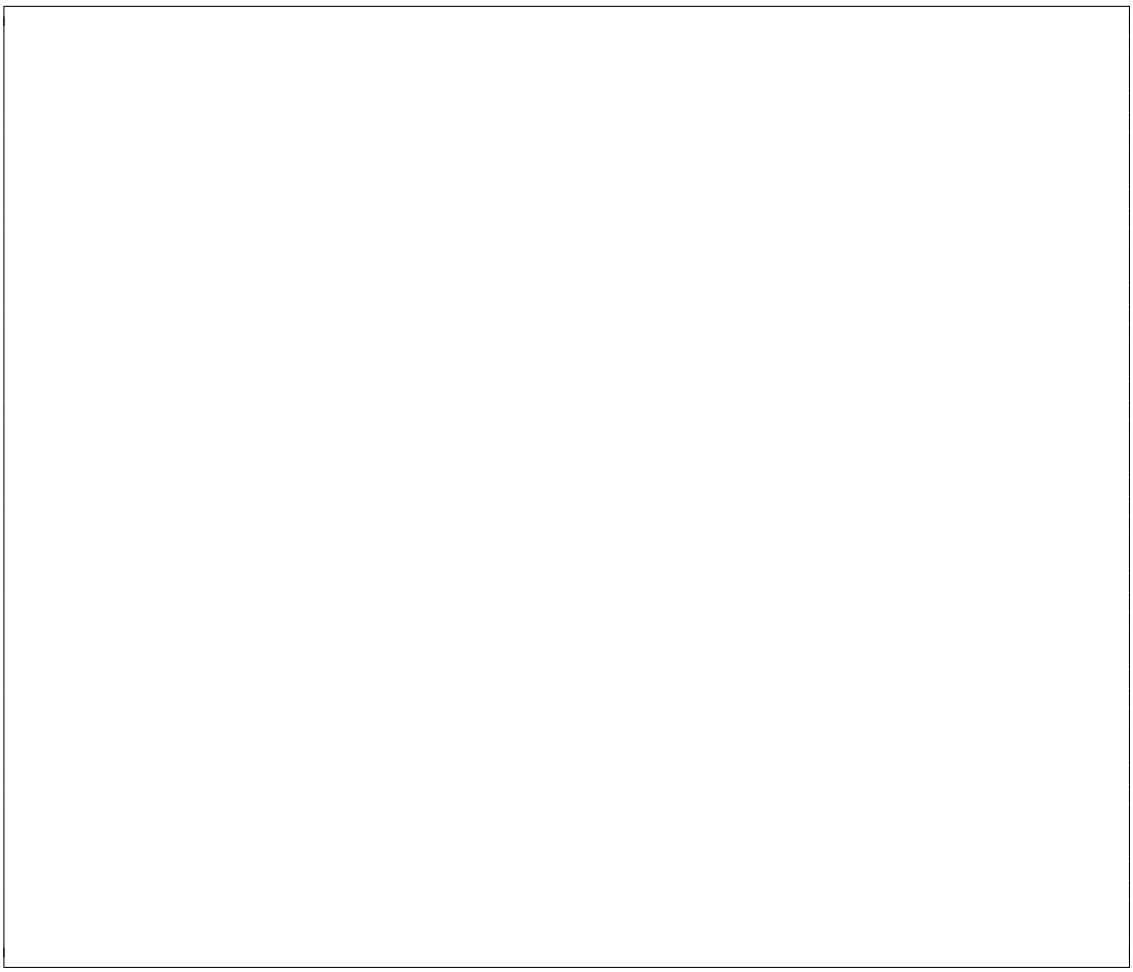
2. (25 points) [`50 minutes`]

(2.1) (5 points) A hypothetical pipeline uses a 256-entry Gshare branch predictor with a 92% accuracy, and a 512-entry BTB with an 82% target prediction accuracy, and incurs a 10-cycle branch/BTB mispredict latency. Also, assume that there is not a single instance when BTB and branch predictor make wrong predictions. To spell it out precisely, either BTB or branch direction predictor performs mispredictions but not both for a given instruction. What is the CPI of this pipeline design? Please write CPI with exactly two decimal places only. For example, if your CPI is 2.5, do mention 2.50. Similarly, if your CPI is 3.9723, do mention 3.97. You are not supposed to assume anything about the number of stages, ISA, program, and of course, the rest of the world.



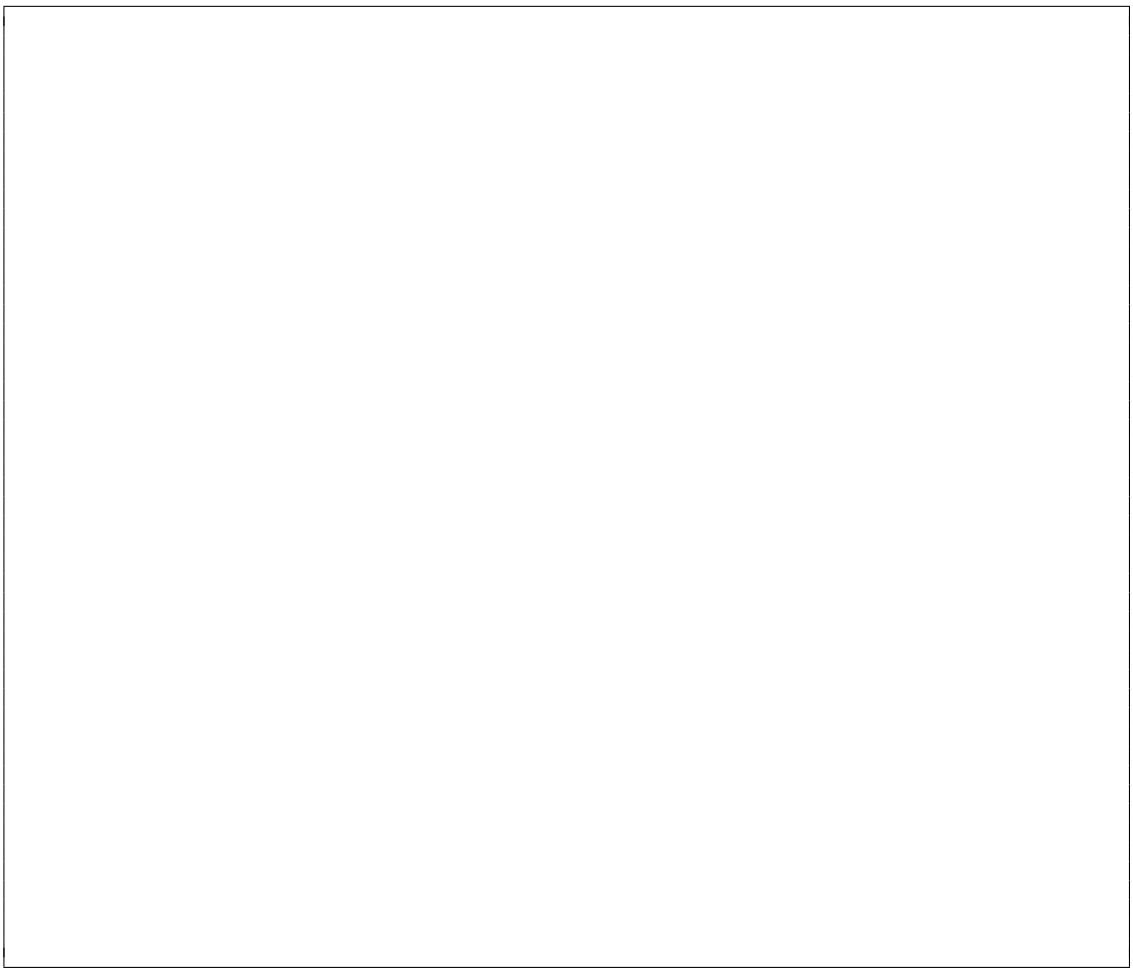
Answer: 3.60
1 + (0.08*10) + (0.18*10) = 3.60
This is with the assumption that all instructions are branch instructions. We are open for other answers with valid assumptions.

(2.2) (5 points) Consider the following instruction runs on a five stage pipelined processor:
add $2, $3, $4
lw $1, 4($2)
sub $4, $1, $5
add $6, $1, $5
and $8, $1, $7
Find the # of cycles needed to execute these instructions a)without operand forwarding [2.5 points], b)with operand forwarding [2.5 points] Show it with pipeline usage diagrams.



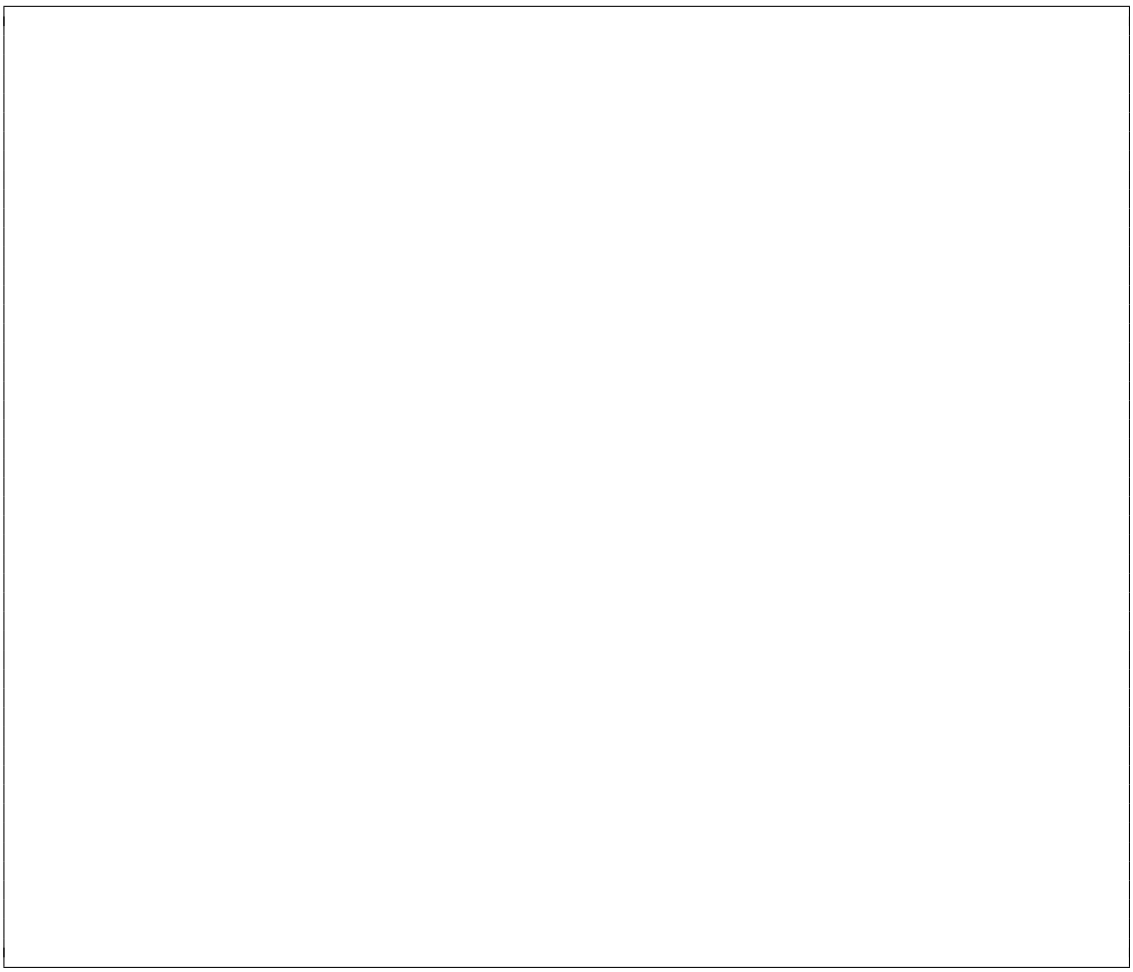
Answer: 13 and 10

(2.3) (5 points) Suppose a system has 32-bit instructions and 32 general-purpose registers. Answer the following questions: (a) What is the number of bits required for the registers? [2 points] (b) Is it possible to have various operations consisting of 20 three-address instructions, 22 two address instructions and ten one-address instructions? [3 points]



(a) 5, (b) Yes, plz check Problem set 3

(2.4) (5 points) Consider a 5 stage pipeline with 2ns clock that supports Branch instructions. Processor stops fetching the following instructions after branch instruction is executed. Target address is available in the pipeline when branch instruction execution is completed. Program contains 30% branch instructions. Among them 40% are conditional in which 60% of instructions don't satisfy the condition. When the condition is false, the following instructions are overlapped. (a) What is the average instruction execution time? [3 points] (b) What is the speedup? [2 points]



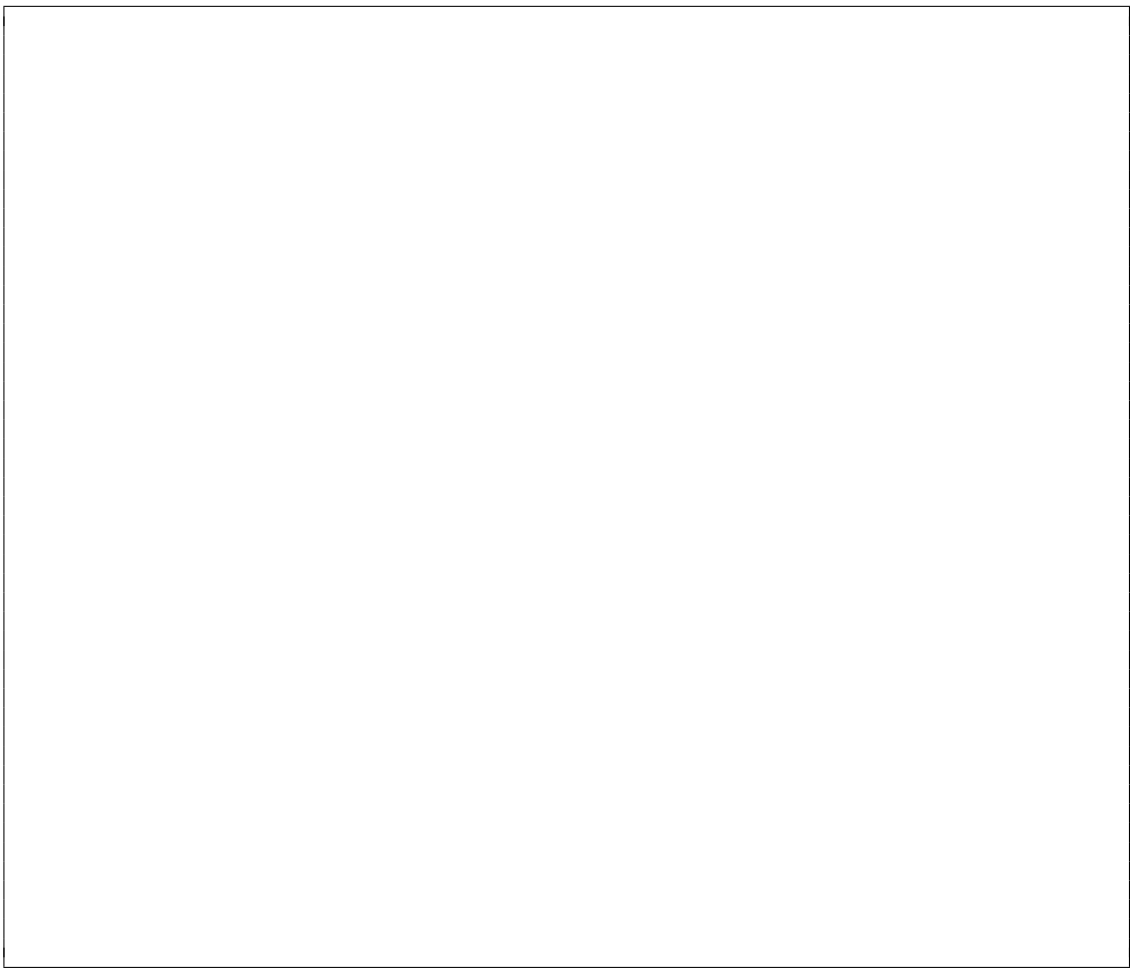
Problem set 4, We will give marks for both 2-cycle and 4-cycle penalty assuming the ambiguity in the word "instruction-execution"

(2.5) (5 points) Lisan and Atharva were designing a typical MIPS datapath implementation that have the following latencies (ps represents picoseconds): Instruction Fetch: 200ps Instruction Decode: 120ps Execute (ALU): 190ps Memory Access: 400 ps Register Write Back 100ps Lisan designed a pipelined implementation whereas Atharva opted for a non-pipelined version.

(a) What is the clock cycle time in a pipelined and non-pipelined implementation version of this MIPS processor? [2 points] **Pipelined: cycle time determined by slowest stage: 400ps. Non-pipelined: cycle time determined by the sum of all stages: 1010ps.**

(b) What is the total latency of the LOAD instruction in a pipelined and non-pipelined processor? [2 points] **LW instruction uses all 5 stages. Pipelined processor takes 5 cycles at 400ps per cycle for a total latency of 2000ps. Non-pipelined processor takes 200+120+190+400+100 = 1010ps.**

(c) Atharva suggested that Lisan should split one stage of the pipelined datapath into two new stages. Which stage would you split, and what is the new clock cycle time of the processor? [1 point]

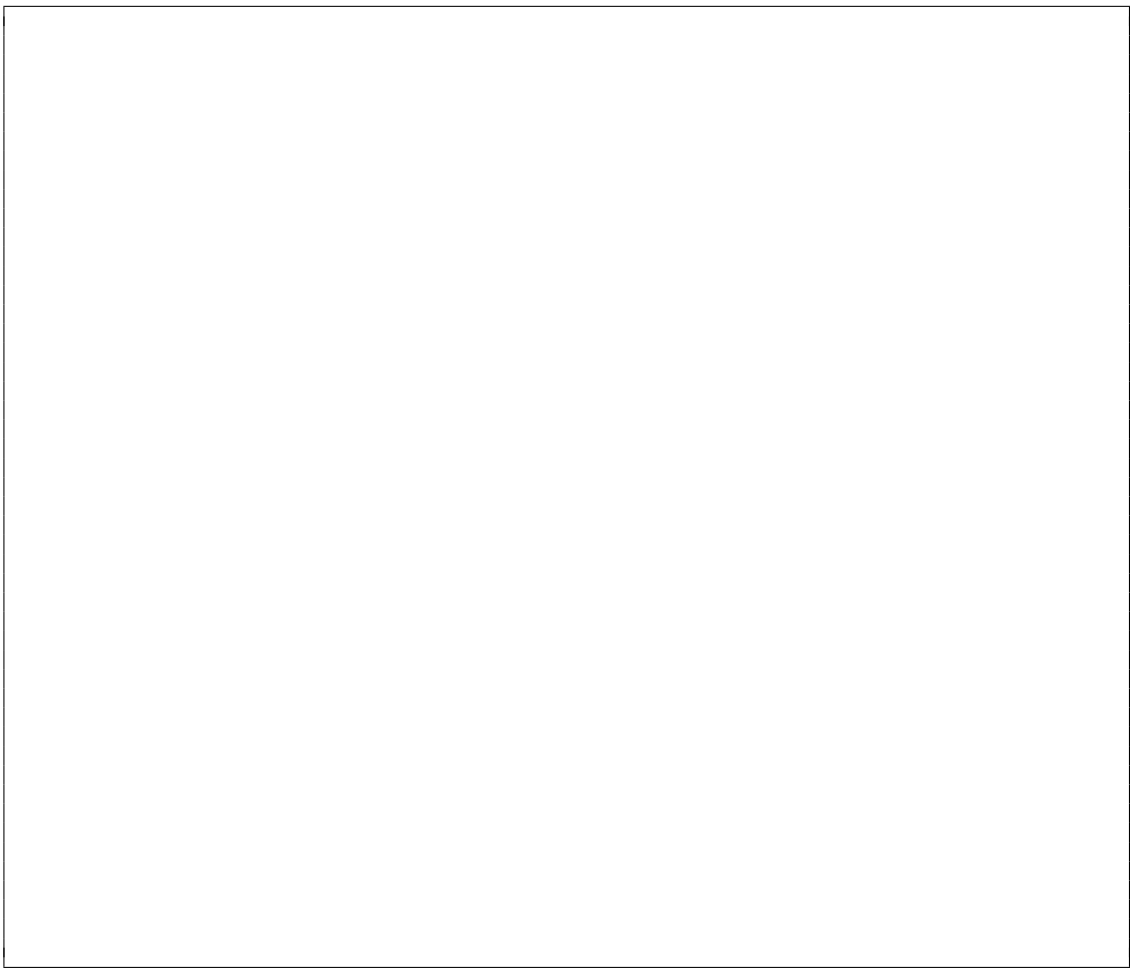


Split the Memory Access stage into two stages of 200ps. The new clock cycle time is 200ps

3. (1 point) [`5 minutes of philosophy`]

   (3.1) (1 point) "A young Apollo, golden-haired, Stands dreaming on the verge of strife, Magnificently unprepared For the long littleness of life"

   What does this four lines mean?



Kuch bhi :)

Yeah CS230 ka quiz hai; aur yeh humara answers hai; aur yeh humara pawri (party) ho rahi hai :) bas pawri ho rahi hai hai :)

Spend 10 minutes on your answers so that there will be zero cribs and you will be able to save 2000 minutes of your TAs.

Hopefully no cribs