CS230: Digital Logic Design and Computer Architecture
Tutorial 07, [Mon 07 Oct, Tue 08 Oct, Thu 10 Oct]

Concepts tested: Pipeline Control, Exceptions in the Pipeline

1. Write the data forwarding control logic to the EX stage, including forwarding from lw.
2. Write the stalling control logic for a dependent reg-reg following a lw. Can this code be combined with the earlier data forwarding control logic code?
3. Considering a 2-stage beq, give the modified datapath to enable the necessary data forwarding (ignore any other data hazards).
4. As per the above datapath modification, write the data forwarding control logic for a dependent 2-stage beq, dependent on any earlier reg-reg instruction.
5. Write the stalling logic resulting from a control hazard due to a 2-stage beq.
6. Suppose that the data memory address misaligned exception is detected early in the MEM stage of LW. Give an example sequence of instructions in which the first instruction of the exception handler is fetched but is flushed due to another exception.