CS230: Digital Logic Design and Computer Architecture
Tutorial 08, [Mon 14 Oct, Tue 15 Oct, Thu 17 Oct]
Concepts tested: Memory Hierarchy, Cache Design

1. What is the difference between registers acting as a cache for L1-cache, versus L1-cache acting as a cache for main memory?
2. What are the three reasons why a cache is faster than main memory?
3. Consider a main memory of 256 words, and a direct mapped cache with 8 blocks of 2 words each. The cache is initially empty. The following sequence of word addresses are accessed by the processor.
   2, 3, 11, 16, 21, 13, 64, 48
   19, 11, 3, 22, 4, 27, 6, 11
   Mark each reference as a hit or a miss, and show the final cache contents. Identify instances of temporal locality and spatial locality.
4. Re-work the above problem assuming that the main memory size is 1024 words.
5. Consider a system with main memory size 32MB, cache size 512KB, 16-word blocks. For the following cases, (i) show the memory address fields as interpreted by the cache controller, (ii) mention the number of comparators required, (iii) indicate the number of bits that must be compared in each comparator, (iv) compute the number of meta-data bits required to implement the cache.
   (a) Direct mapped
   (b) 2-way set associative
   (c) 4-way set associative
   (d) 8-way set associative
   (e) Fully associative