PROBLEM SET - 2 CS230

August 2023

1

Given an S-R latch circuit implemented using NAND gates, where the propagation delay of each NAND gate is 5 ns, and the initial state of the latch is Q = 0 and $\bar{Q}$ (Q bar) = 1. The S and R inputs are connected to a control circuit. At time t = 0, the control circuit activates both S and R simultaneously by setting S = 1 and R = 1. Determine the state of the latch at t = 20 ns. Assume that the S and R inputs remain constant after being activated.

2

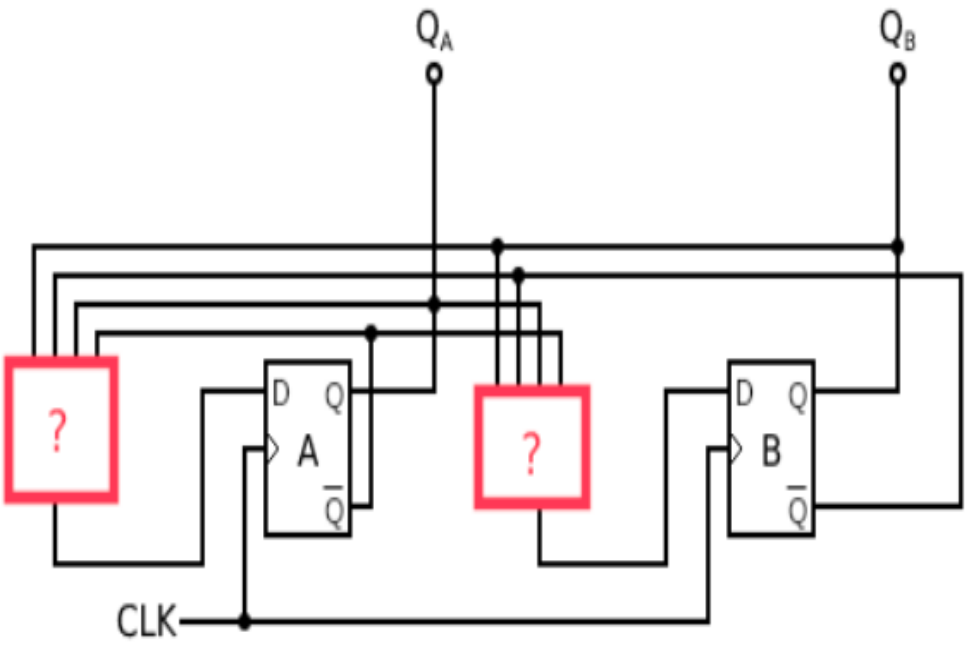
Design a Mealy state machine that simulates a simple doorbell system. The machine has two states, 'Idle' and 'Ring'. When in the 'Idle' state and the input button is pressed (input 1), it transitions to the 'Ring' state and outputs 'Ding'. When in the 'Ring' state and the input button is released (input 0), it transitions back to the 'Idle' state and outputs 'Silent'. Give the state transition table for the Mealy machine.

3

What is the minimum number of D flip-flops to design a counter for the sequence 0, 0, 1,1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6, 7, 7, 0, 0, 1, 1...?

4

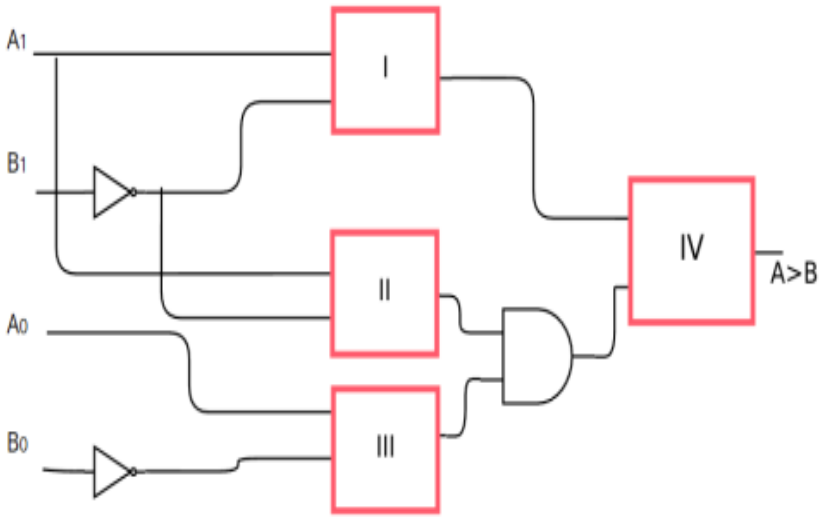
You have to design a 2-bit mod 3 binary counter using D flip-flops. The counter should follow the following sequence: 0, 1, 2, 0, 1, 2, 0..... You are given the following circuit.



Write the Boolean expression for D_A and D_B, in terms of Q_A ,$\bar{Q}_A$,Q_B, $\bar{Q}_B$to complete the circuit.

5

You have to design a two-bit greater than comparator logic circuit (A > B). The following incomplete circuit is provided to you. Name the appropriate logic gate for each red box to complete the circuit.


A1
B1
A0
B0
I
II
III
IV
A>B