PROBLEM SET - 2 Soln CS230

August 2023

1

Design a Mealy state machine that simulates a simple doorbell system. The machine has two states, 'Idle' and 'Ring'. When in the 'Idle' state and the input button is pressed (input 1), it transitions to the 'Ring' state and outputs 'Ding'. When in the 'Ring' state and the input button is released (input 0), it transitions back to the 'Idle' state and outputs 'Silent'. Give the state transition table for the Mealy machine.

Current	Input	Next	Output
Idle	0	Idle	Silent
Idle	1	Ring	Ding
Ring	0	Idle	Silent
Ring	1	Ring	Ding

2

What is the minimum number of D flip-flops to design a counter for the sequence 0, 0, 1,1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6, 7, 7, 0, 0, 1, 1...?

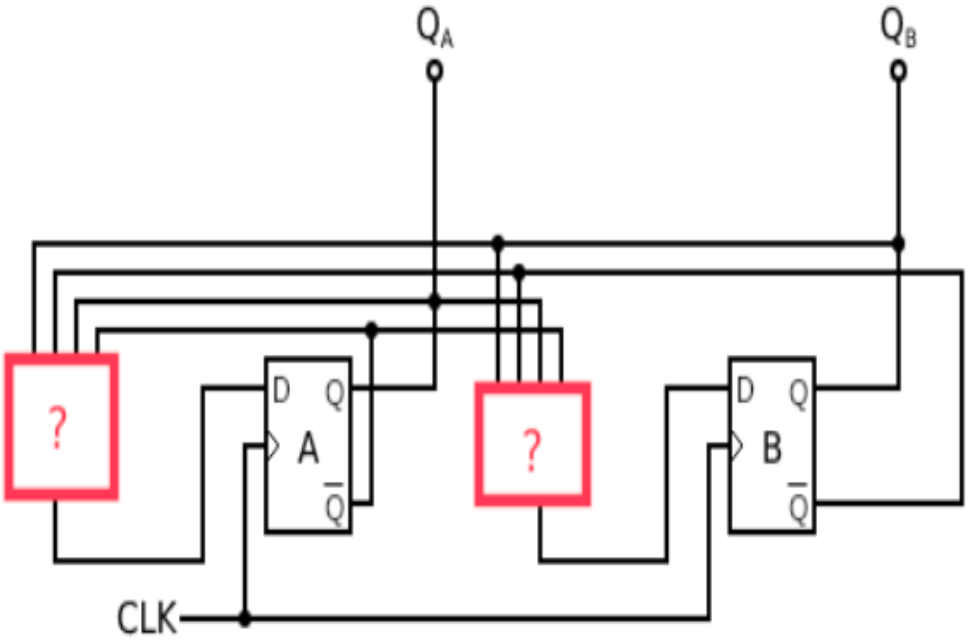
Since each number is repeated two times, we can assign two different states to each number. The sequence then can be written as: 01, 02, 11, 12, 21, 22, 31, 32, 41, 42, 51, 52, 61, 62, 71, 72, 01, 02....
We have 16 distinct states.
To represent m distinct states, we need a minimum of $\lceil \log_2 m \rceil$ flip-flops because each flip-flop can toggle between two states.
So, for 16 states, you need 4 flip-flops.

3

You have to design a 2-bit mod 3 binary counter using D flip-flops. The counter should follow the following sequence: 0, 1, 2, 0, 1, 2, 0..... You are given the following circuit.

Write the Boolean expression for D_A and D_B, in terms of Q_A ,$\bar{Q}_A$,Q_B, $\bar{Q}_B$to complete the circuit.

sol:


Q_A
Q_B
?
D
Q
A
$\overline{Q}$
?
D
Q
B
$\overline{Q}$
CLK

The state table will be:

Q_A	Q_B	Q_{A+1}	Q_{B+1}	D_A	D_B
0	0	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0
1	1	X	X	X	X

K-map for D_A

Q_a \ Q_b	0	1
0	0 (0)	1 (1)
1	0 (2)	- (3)

$$D_A = Q_B$$

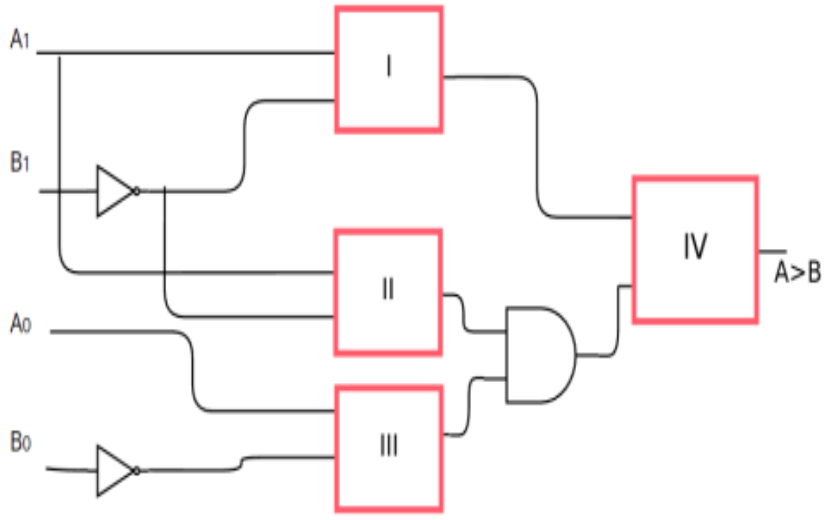
K-map for D_B

Q_a \ Q_b	0	1
0	1 (0)	0 (1)
1	0 (2)	- (3)

$$D_B = \overline{Q_A}\,\overline{Q_B}$$

1

You have to design a two-bit greater than comparator logic circuit ($A > B$). The following incomplete circuit is provided to you. Name the appropriate logic gate for each red box to complete the circuit.

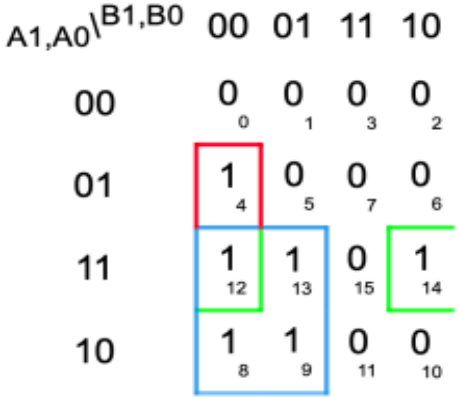


Sol:

The truth table for the comparator:

A_1	A_0	B_1	B_0	C
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

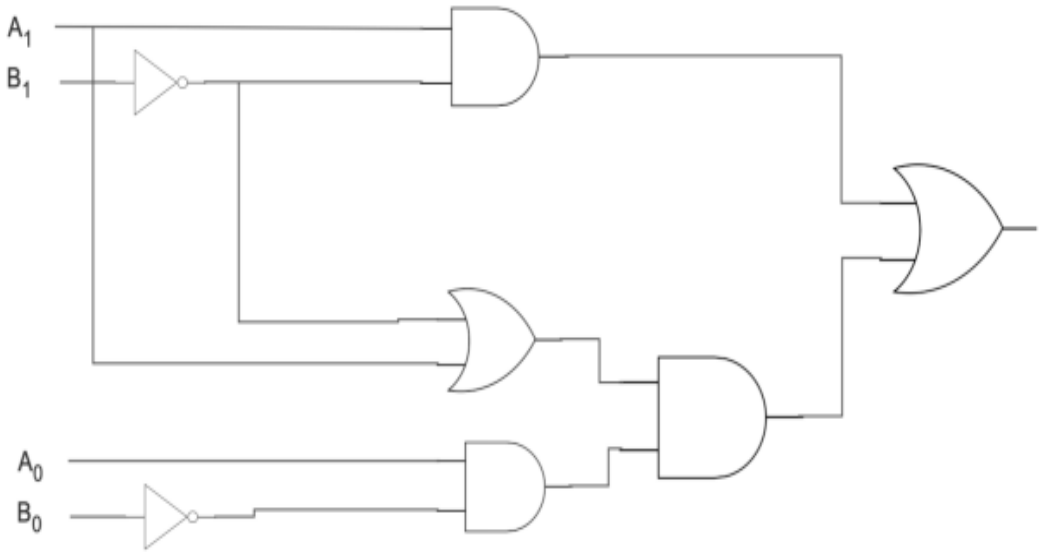
Solving using K-map



$$C = A_0\overline{B_1}\,\overline{B_0} + A_1A_0\overline{B_0} + A_1\overline{B_1}$$
$$= (A_1 + \overline{B_1})A_0\overline{B_0} + A_1\overline{B_1}$$

Mapping the expression with circuit:

I) AND Gate
II) OR Gate
III) AND Gate
IV) OR Gate


A1
B1
A0
B0