Electrical Characterization of RF-sputtered HfO_2 MOS capacitors

by,

Sreemoyee Saha & Abhijeet Singh

Department of Electronic Science, University of Calcutta

MSc. Project stage- II

SEM- IV (February 2024- June 2024)

Supervised by,

Prof. Anupam Karmakar

Department of Electronic Science, University of Calcutta

And

Prof. Sanatan Chattopadhyay

Department of Electronic Science, University of Calcutta

OUTLINE

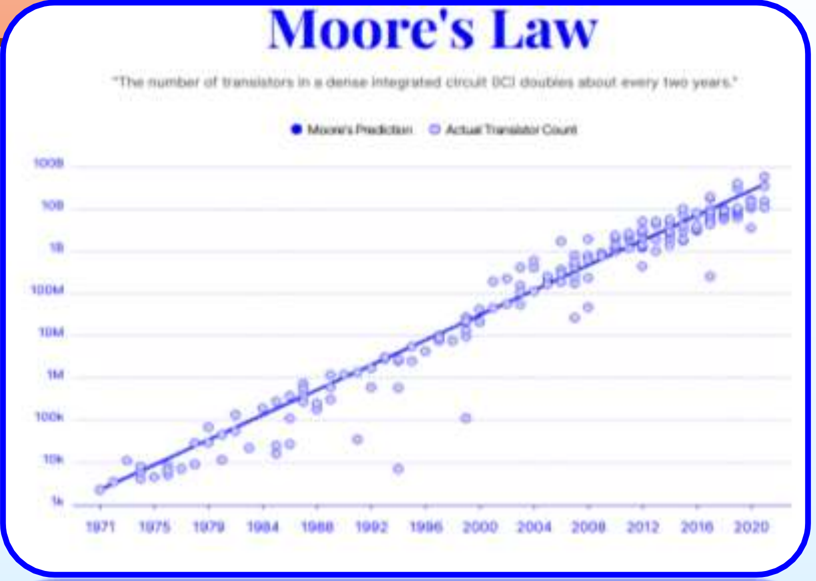
- ❑INTRODUCTION
- ❑NECESSITY OF USING HIGH-K MATERIAL
- ❑CHALLENGES OF HIGH-K
- ❑FABRICATION STEPS
- ❑EXPRIMENTAL ANALYSIS
- ❑ELLIPSOMETRIC SPECTROSCOPY DATA
- ❑C-V MEASUREMENTS DATA
- ❑I-V MEASUREMENTS DATA
- ❑CONCLUSION

INTRODUCTION

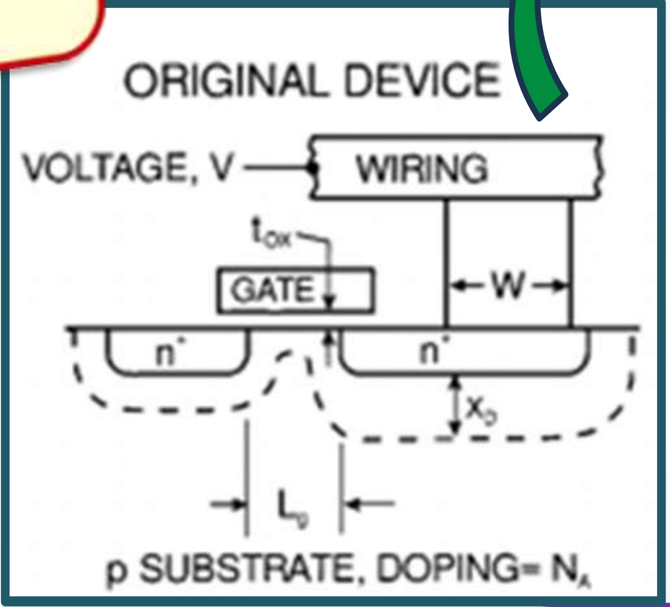
With the advancement of modern technology the need of accommodating higher no. of transistor in a single chip is increasing by the moment.

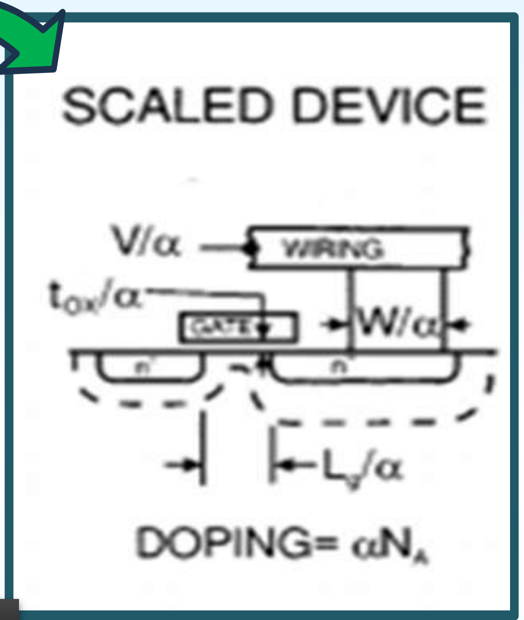
For this purpose the idea of scaling of MOS capacitor was introduced in 1974 by Robert H. Dennard of IBM

In 1965 Gordon Moore stated a observation regarding no. of transistors in a single chip.



DOWNSCALING





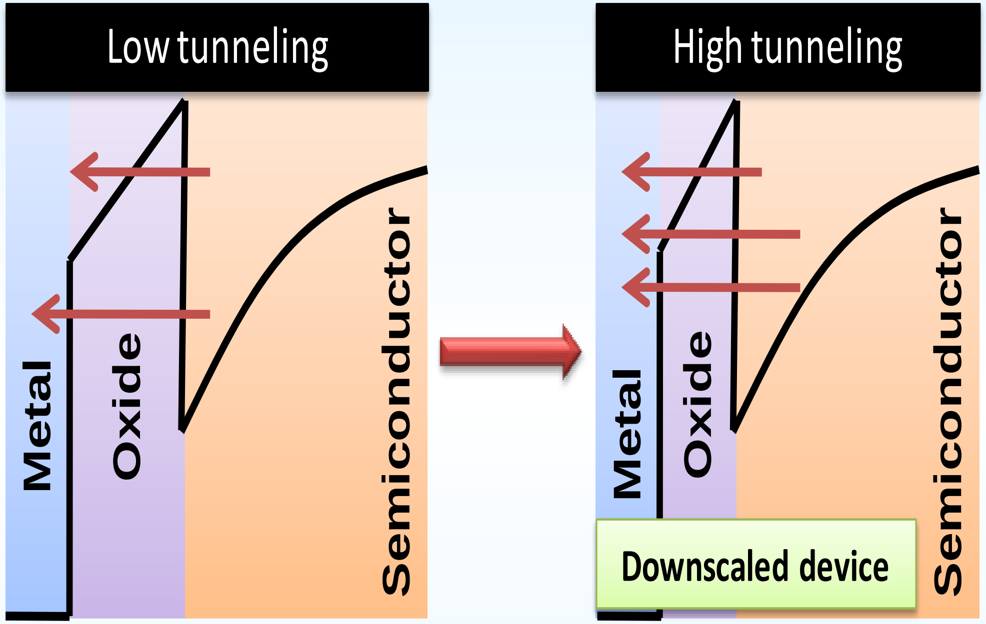
ADVANTAGES:

- Higher packing density
- Improved performance
- Reduced power consumption

INTRODUCTION

SIDE- EFFECTS OF DOWNSCALING

- **Short channel effects**
- **Tunneling effects i.e., *increasing leakage current***
- **Decreased device reliability**
- **Higher gate capacitance leads to slower switching speed**

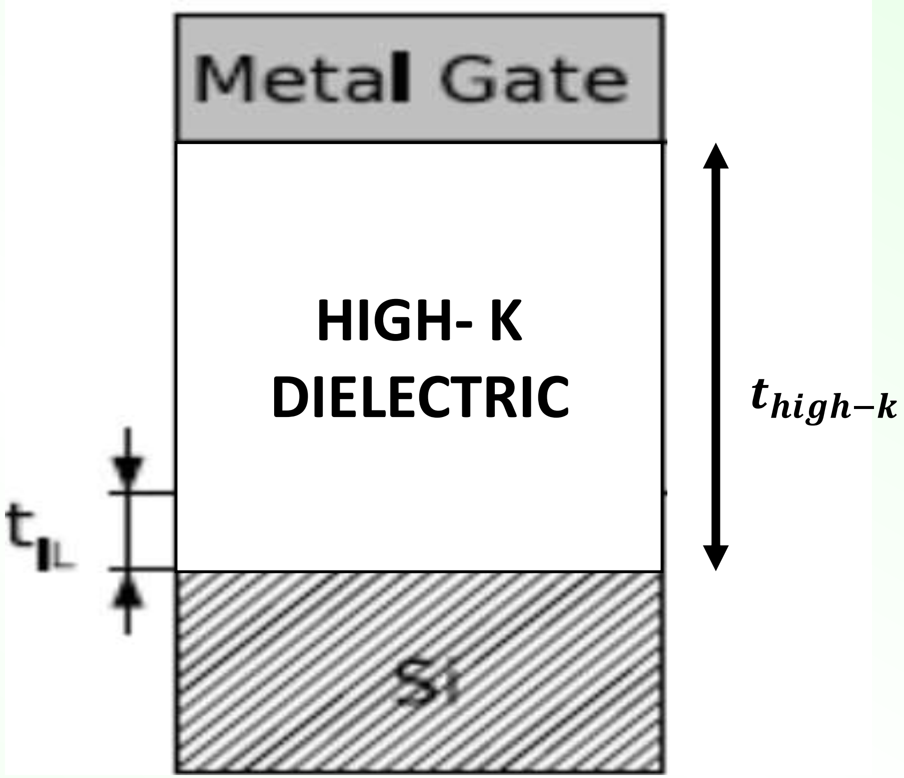


REDUCTION OF OXIDE THICKNESS CAUSES TUNNELING => GATE LEAKAGE

High- k dielectrics **were introduced for better capacitance control but consists a lot of defects.**

WHY HIGH-K?

- Improved Scaling.
- Reduced Equivalent Oxide Thickness (EOT)
- Increased Capacitance
- Reduction in Leakage Current
- High mobility
- Better Threshold Voltage Control
- Enhanced Device Performance
- Reduced Power Consumption



CHALLENGES OF HIGH-K

- **Interface quality: The interface between the high-k dielectric and the silicon substrate contains defects and traps.**
- **Threshold voltage variability: can introduce fixed charges and trap states, leading to threshold voltage instability.**
- **Thermal stability: have lower thermal stability, which can be problematic during high-temperature processing steps.**
- **Finding the right high-k material that balances dielectric constant, band alignment, and process compatibility is a complex task.**

FABRICATION STEPS

RCA1/ RCA2

- **Cleaning of p-Si<100> wafer:**
  - Trichloroethylene, acetone, isopropyl alcohol for 5 mins (each) ultrasonicate
  - 5:3:1 [Di water: H_2O_2:H_2SO_4] 40 °C for 10 min
  - 6:1:1 [Di water:H_2O_2:HCL] 60 °C for 10 min
  - Dip in 1% HF solution for 5 min.

RF-sputtering

- **HfO2 deposition:**
  - Base pressure: 10^{-6}mbar
  - Argon pressure: 2.8×10^{-2} mbar
  - Power wattage: 50 W
  - Deposition time varied for 5 min,10 min and 20 min

Annealing

- **RTA annealing:**
  - In Oxygen ambient
  - Temperature increasing rate 50 °C/sec
  - Annealed for 30 sec
  - At 500 °C and 600 °C

EXPERIMENTAL ANALYSIS

ELLIPSOMETRIC SPECTROSCOPY

For measuring the thickness of HfO_2 thin film

CV measurements

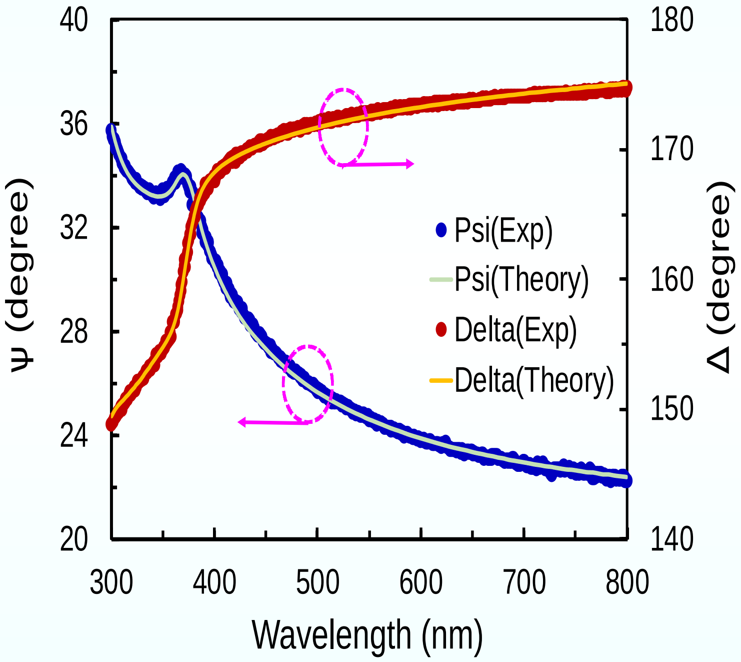
For measuring Q_{eff}, D_{it}, V_{FB}, C_{ox}.

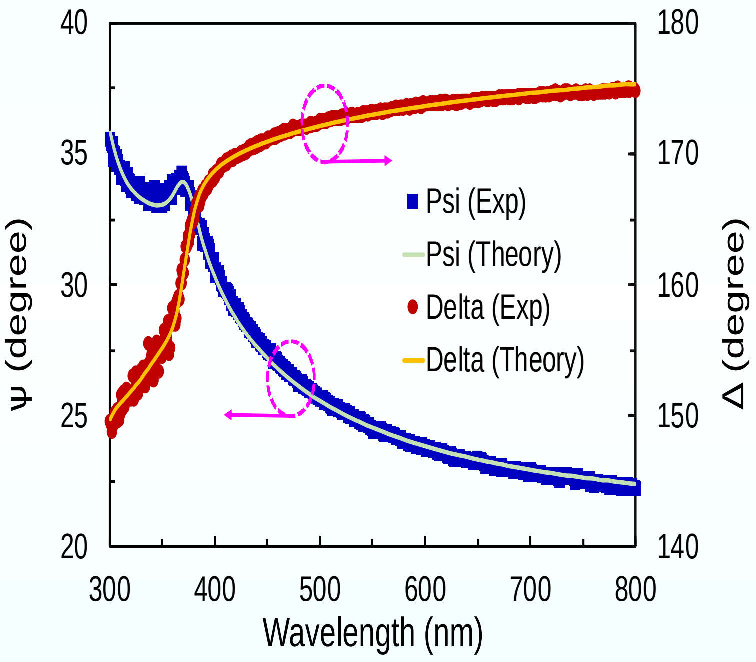
IV measurements

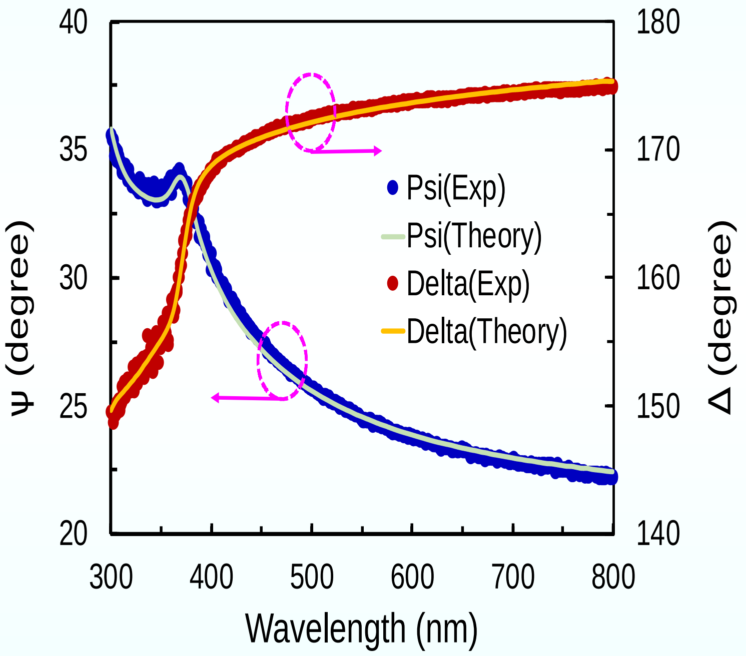
For J-V plot, obtaining plots for tunnelling mechanisms and calculating ϕ_B and ϕ_t

ELLIPSOMETRIC SPECTROSCOPY PLOT

Sample sputtered for 5 min:







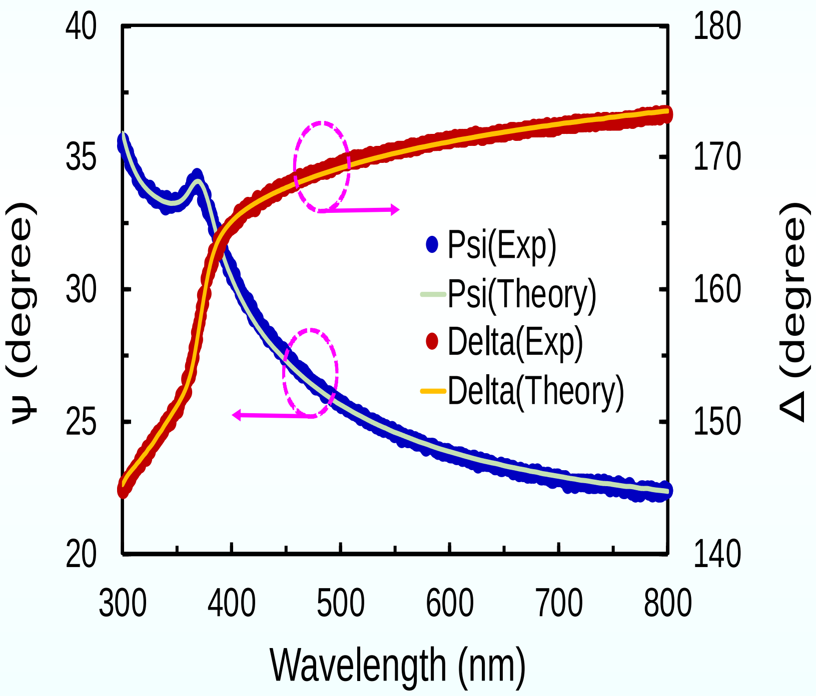
As- dep

500 °C RTA

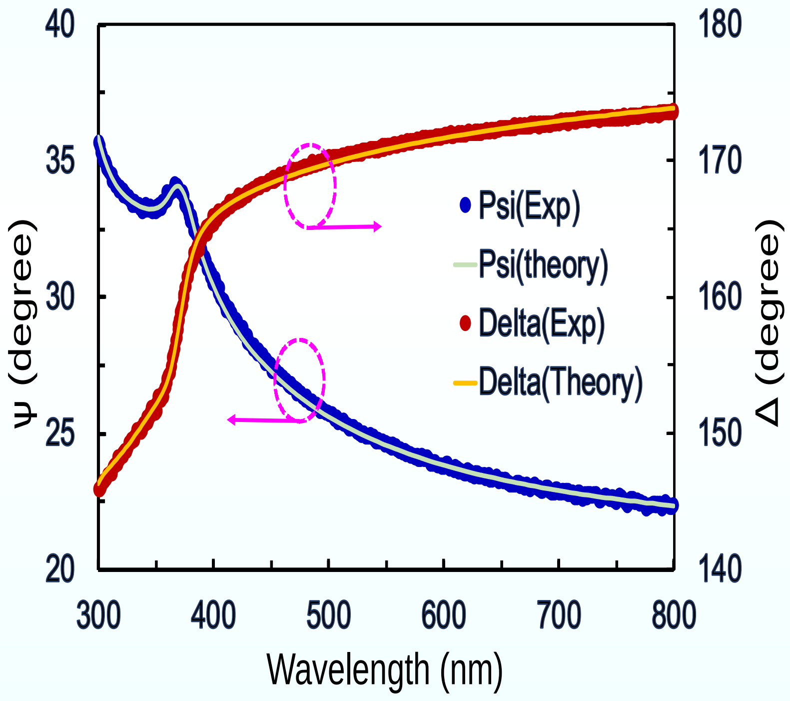
600 °C RTA

ELLIPSOMETRIC SPECTROSCOPY PLOT

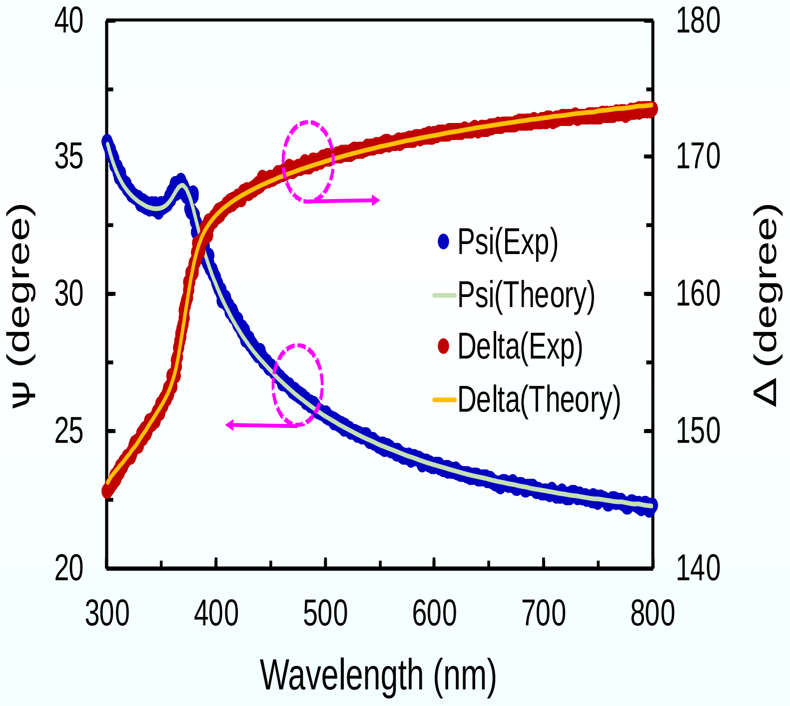
Sample sputtered for 10 min:



As- dep



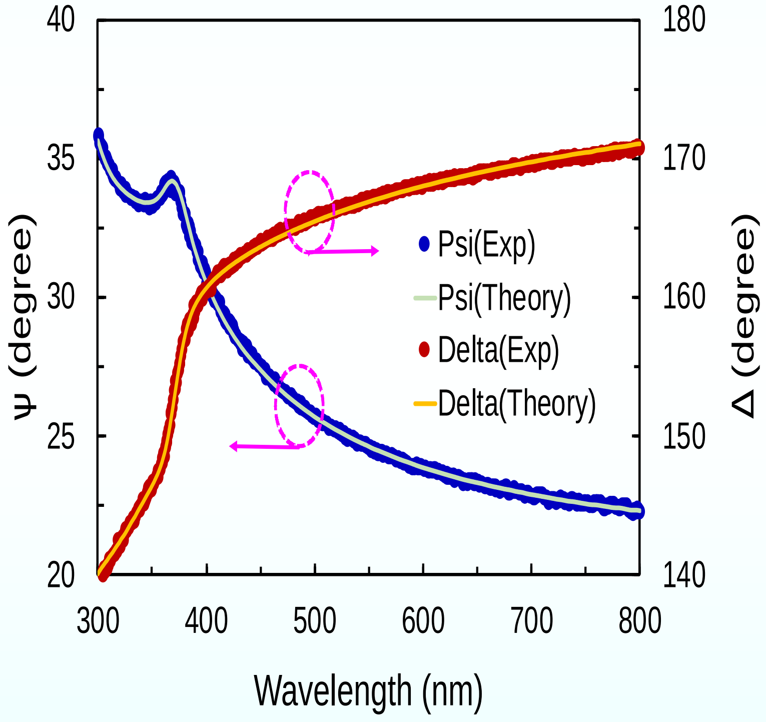
500 °C RTA



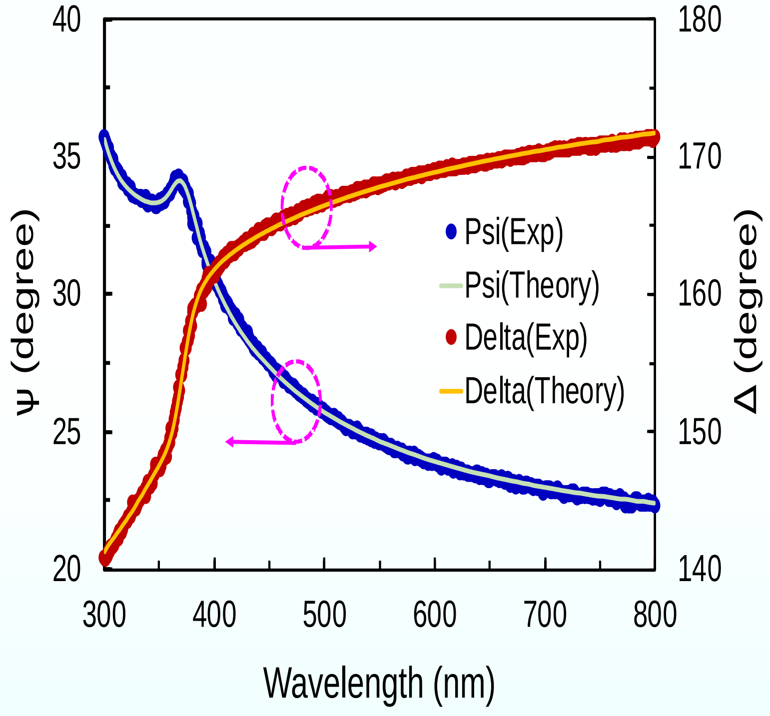
600 °C RTA

ELLIPSOMETRIC SPECTROSCOPY PLOT

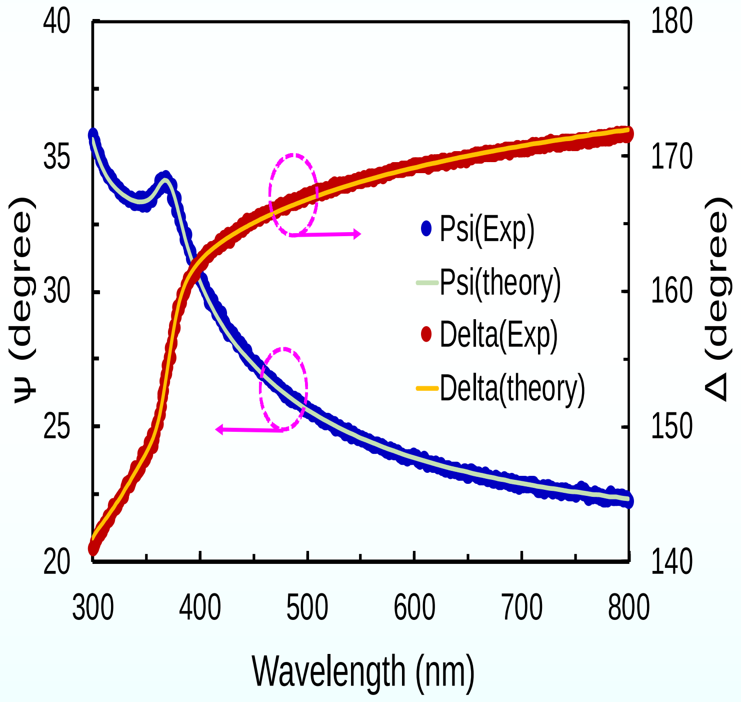
Sample sputtered for 20 min:



As- dep



500 °C RTA



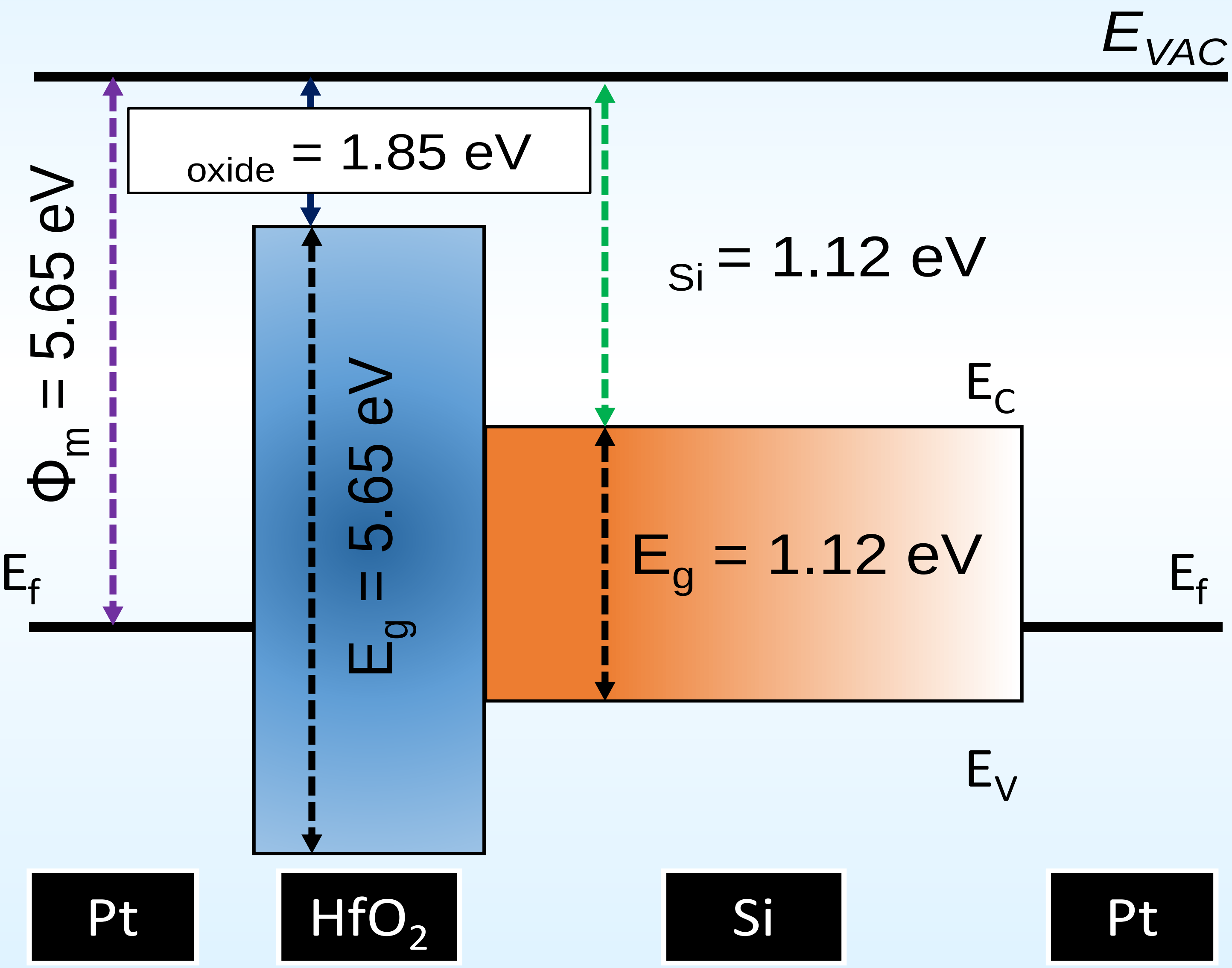
600 °C RTA

THICKNESS OF HfO_2 THIN FILM

Annealing temperature	Sample Thickness (in nm) (sputtered for 5 mins)	Sample Thickness (in nm) (sputtered for 10 mins)	Sample Thickness (in nm) (sputtered for 20 mins)
As- deposited	5.35	7.01	9.66
500ºC	4.60	6.57	8.82
600ºC	4.65	6.51	8.72

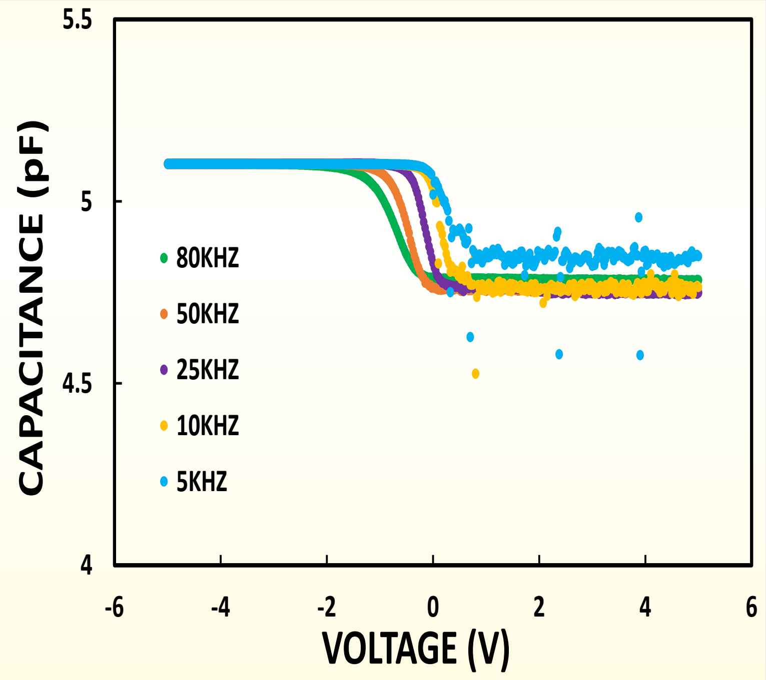
- With the increase of annealing temperature the thickness of the HfO_2 thin film decreased.
- Greater the sputtering time larger the thickness of the HfO_2 thin film.

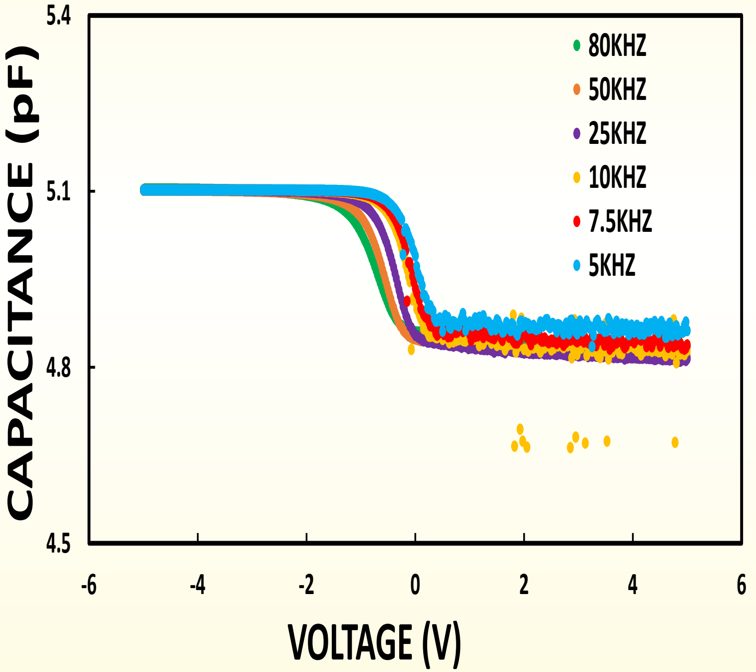
IDEAL BAND DIAGRAM OF HfO_2 MOS CAPACITOR

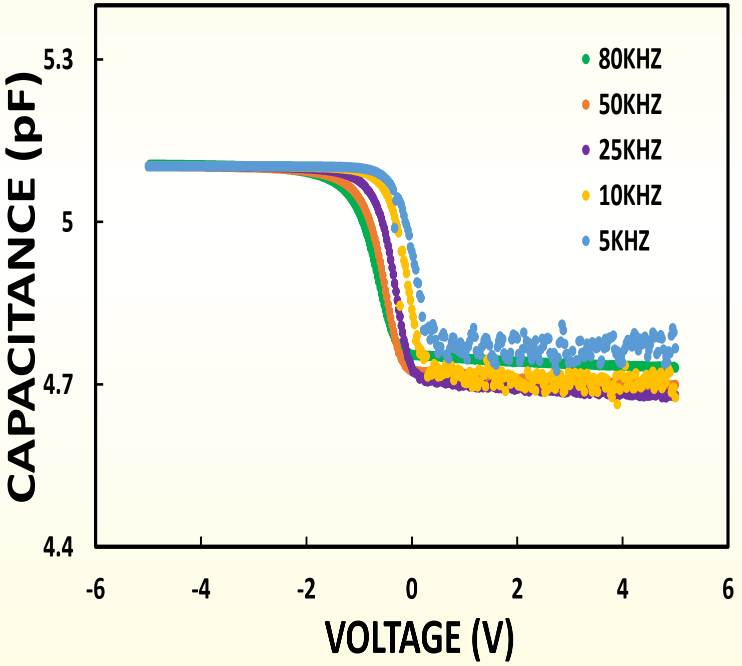


CV MEASUREMENTS PLOTS

Sample sputtered for 5 min:







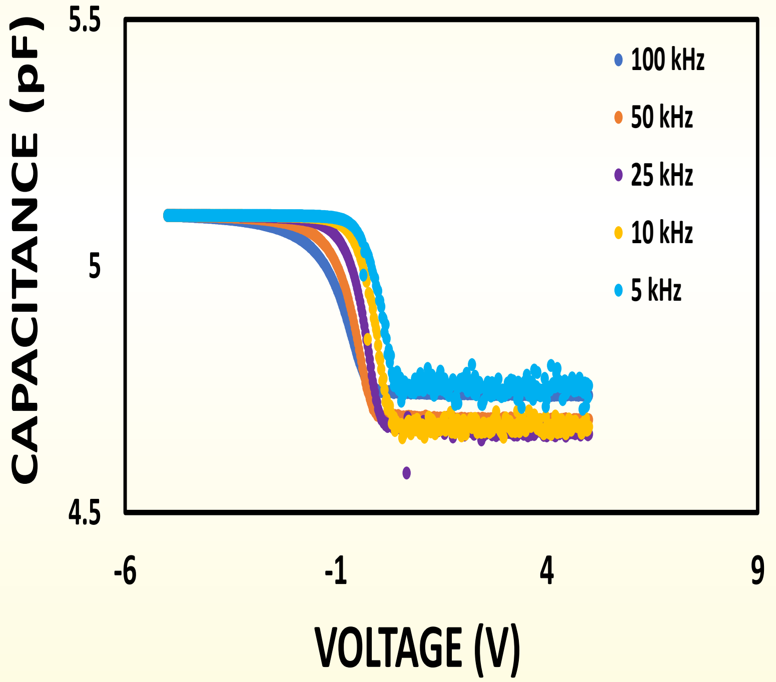
As- dep

500 °C RTA

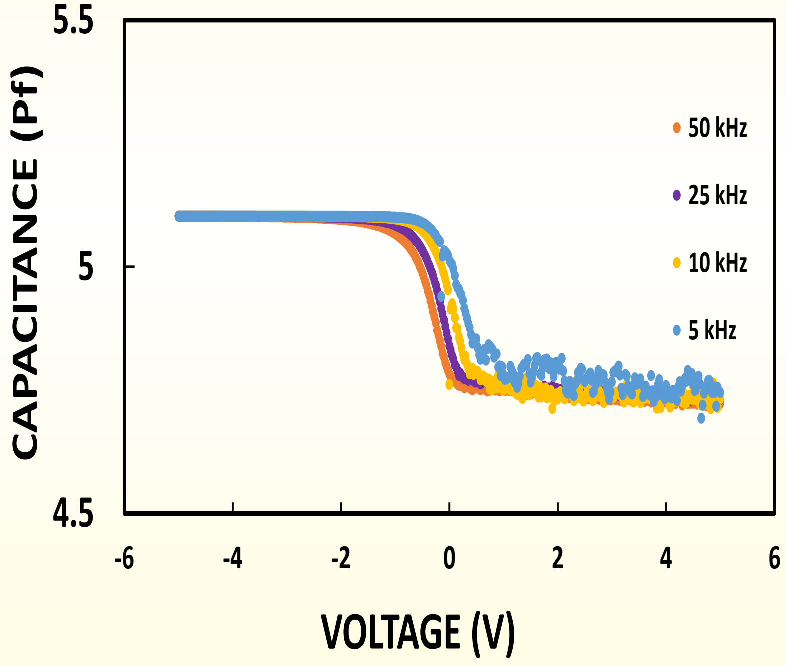
600 °C RTA

CV MEASUREMENTS PLOTS

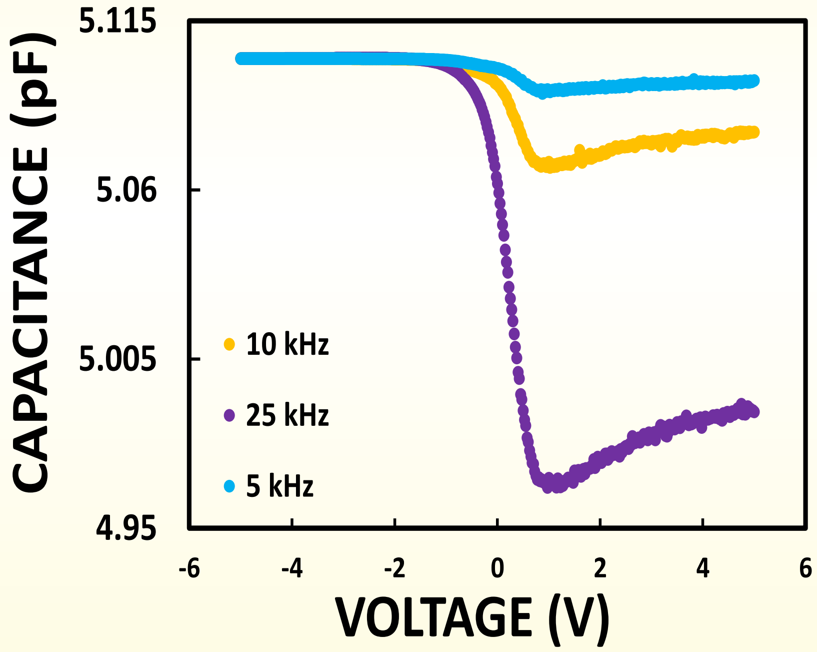
Sample sputtered for 10 min:



As- dep



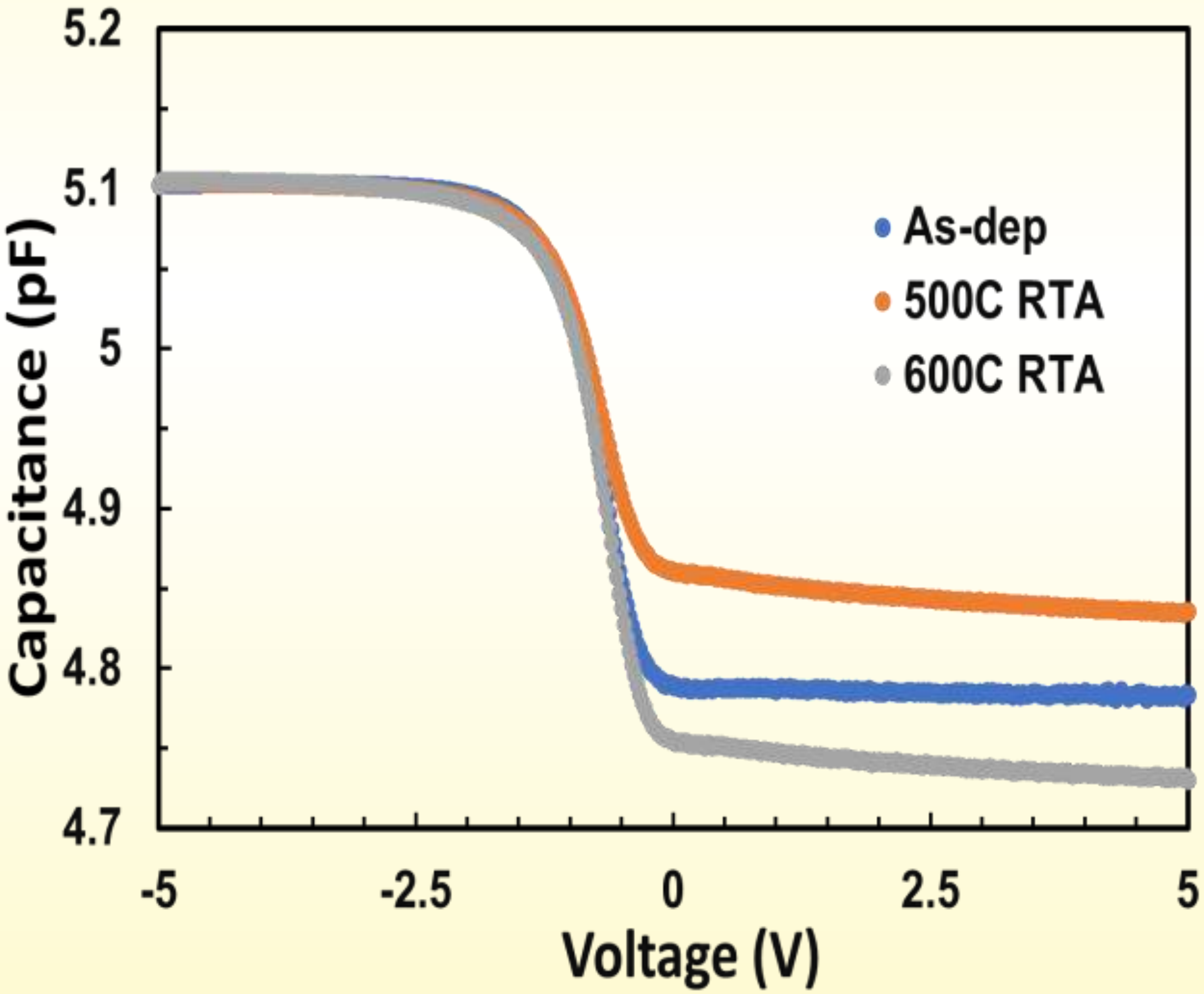
500 °C RTA



600 °C RTA

Q_{eff} and D_{it} COMPARISON (For high frequency)

Sample sputtered for 5 min



Annealing temperature	V_{FB} (V)	Q_{eff} (cm^{-2})	D_{it} ($eV^{-1}cm^{-2}$)
As-dep	-0.05	1.26*10^13	1*10^14
500°C	0.075	1.9*10^13	5.29*10^13
600°C	0.025	6.3*10^12	6.48*10^12

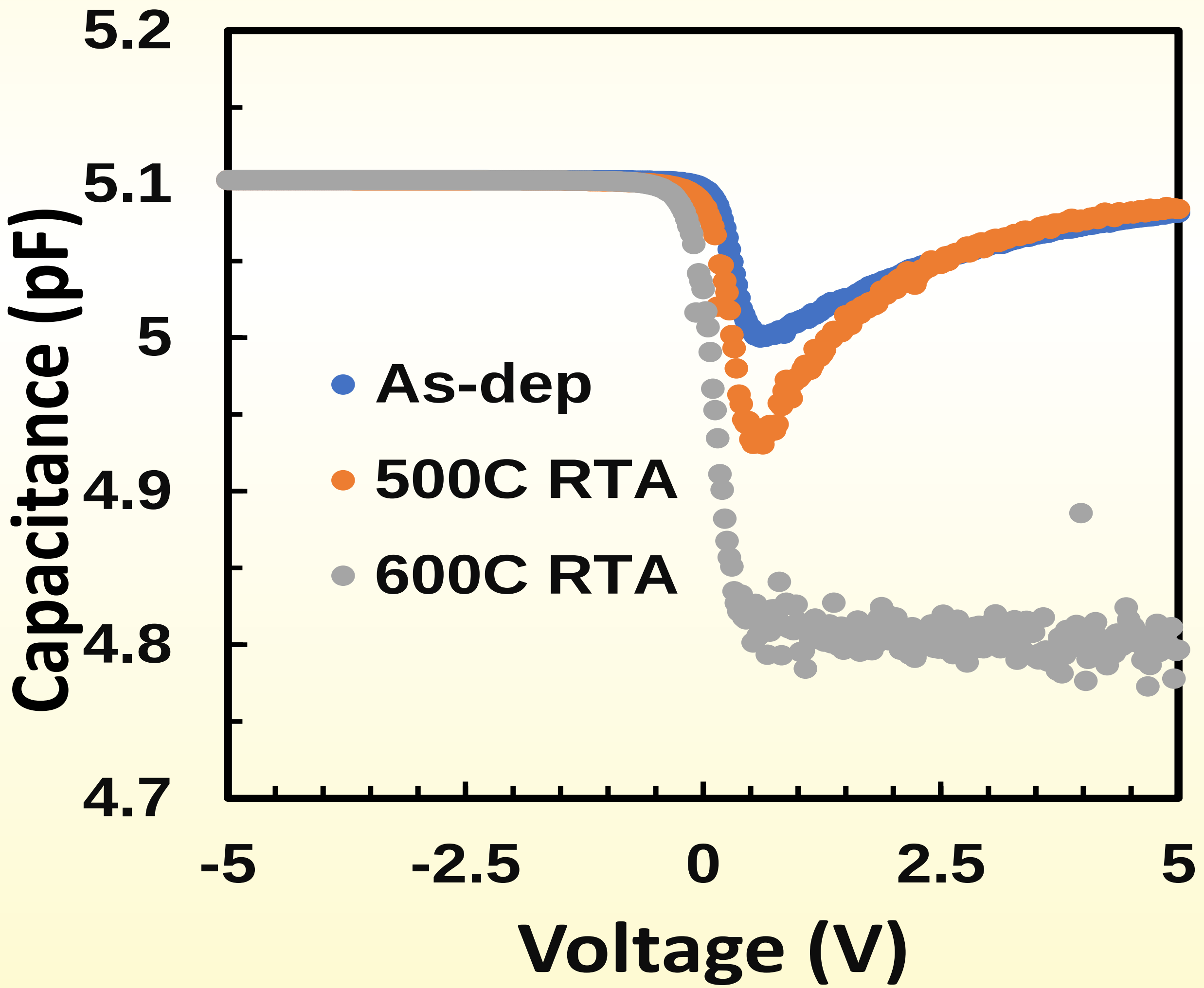
V_{FB} increased for 500°C and decreased for 600°C

Q_{eff} increased for 500°C and decreased for 600°C

D_{it} decreases with increasing annealing temperature

Q_{eff} and D_{it} COMPARISON (For low frequency)

Sample sputtered for 5 min:



Annealing temperature	V_{FB} (V)	Q_{eff} (cm^{-2})	D_{it} ($eV^{-1}cm^{-2}$)
As-dep	0.625	1.58*10^14	1.7*10^14
500ºC	0.95	2.4*10^14	3.47*10^15
600ºC	0.65	1.65*10^14	1.17*10^14

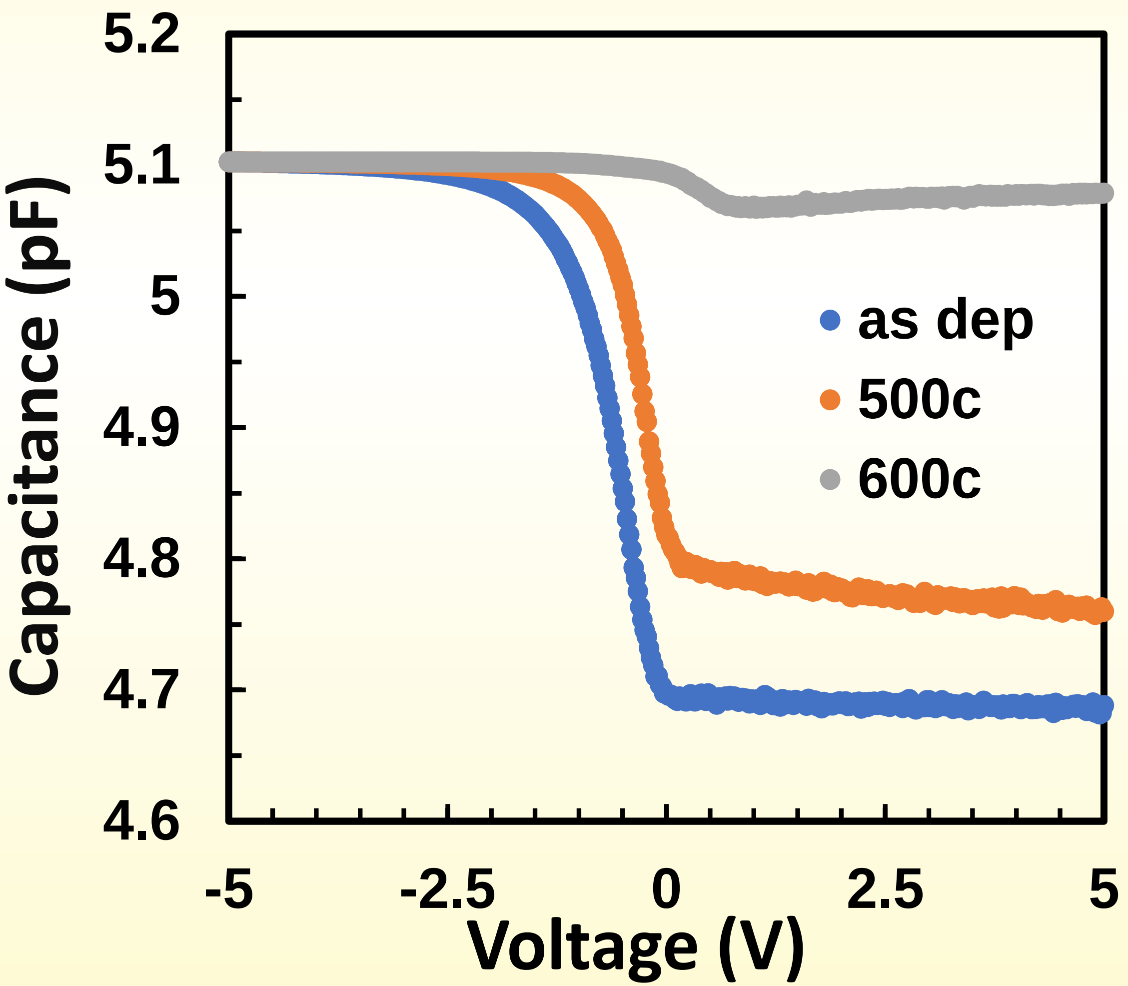
V_{FB} increased for 500°C and decreased for 600°C

Q_{eff} increased for 500C°C and decreased for 600°C

D_{it} also increased for 500°C and decreased for 600°C

Q_{eff} and D_{it} COMPARISON (For high frequency)

Sample sputtered for 10 min:



Annealing temperature	V_{FB} (V)	Q_{eff} (cm^{-2})	D_{it} ($eV^{-1}cm^{-2}$)
As-dep	0.1	2.5*10^13	8.9*10^13
500ºC	0.275	6.9*10^13	9.2*10^13
600ºC	0.9	7.6*10^12	5.5*10^13

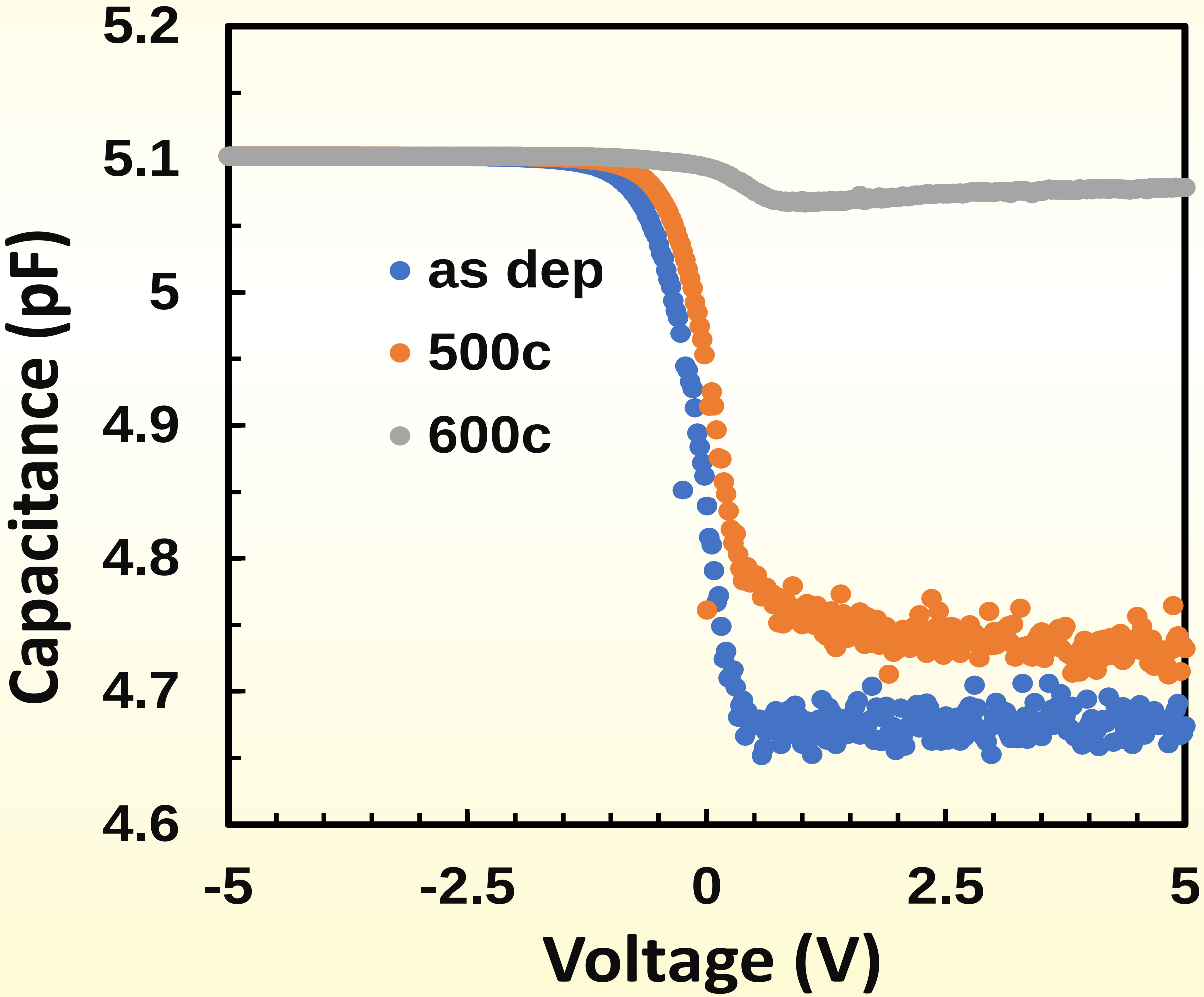
V_{FB} increased with annealing temperature

Q_{eff} increased for 500C°C and decreased for 600°C

D_{it} also increased for 500°C and decreased for 600°C

Q_{eff} and D_{it} COMPARISON (For low frequency)

Sample sputtered for 10 min:



Annealing temperature	V_{FB} (V)	Q_{eff} (cm^{-2})	D_{it} ($eV^{-1}cm^{-2}$)
As-dep	0.65	7.1*10^13	1.1*10^14
500ºC	0.83	2.7*10^13	9.4*10^13
600ºC	1.02	2.41*10^13	3.6*10^13

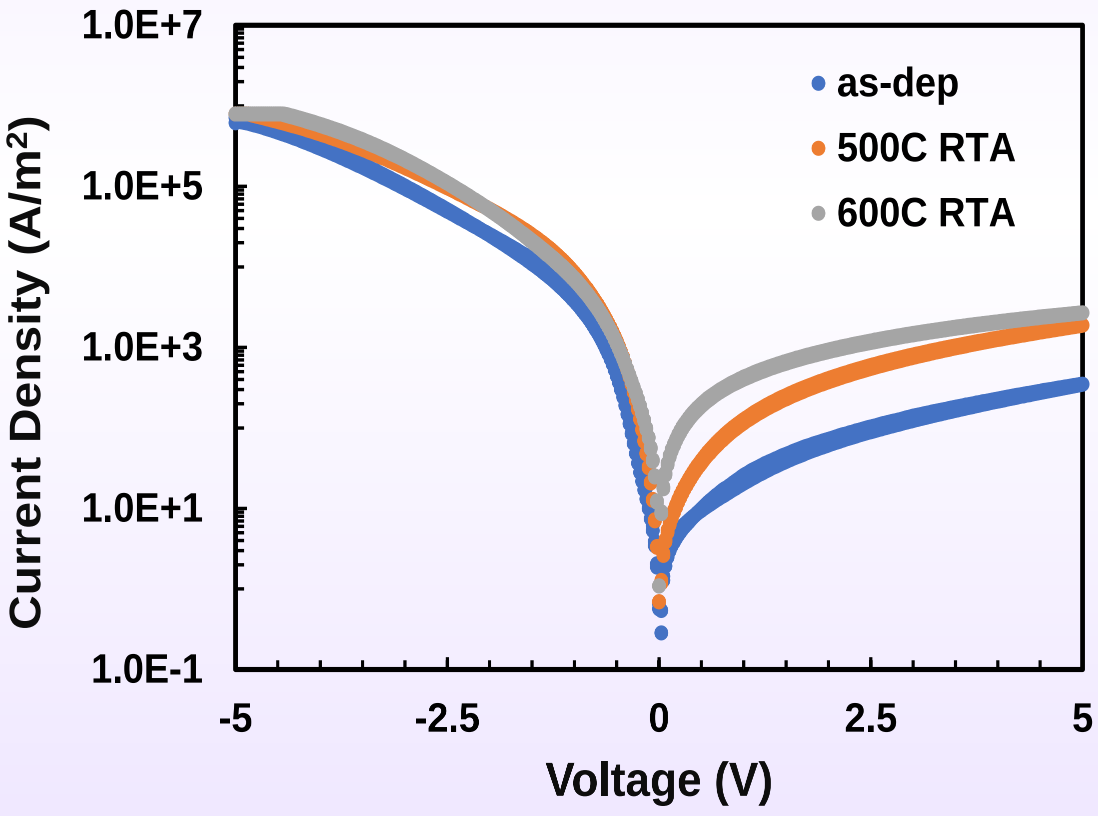
V_{FB} increased with annealing temperature

Q_{eff} decreased with annealing temperature

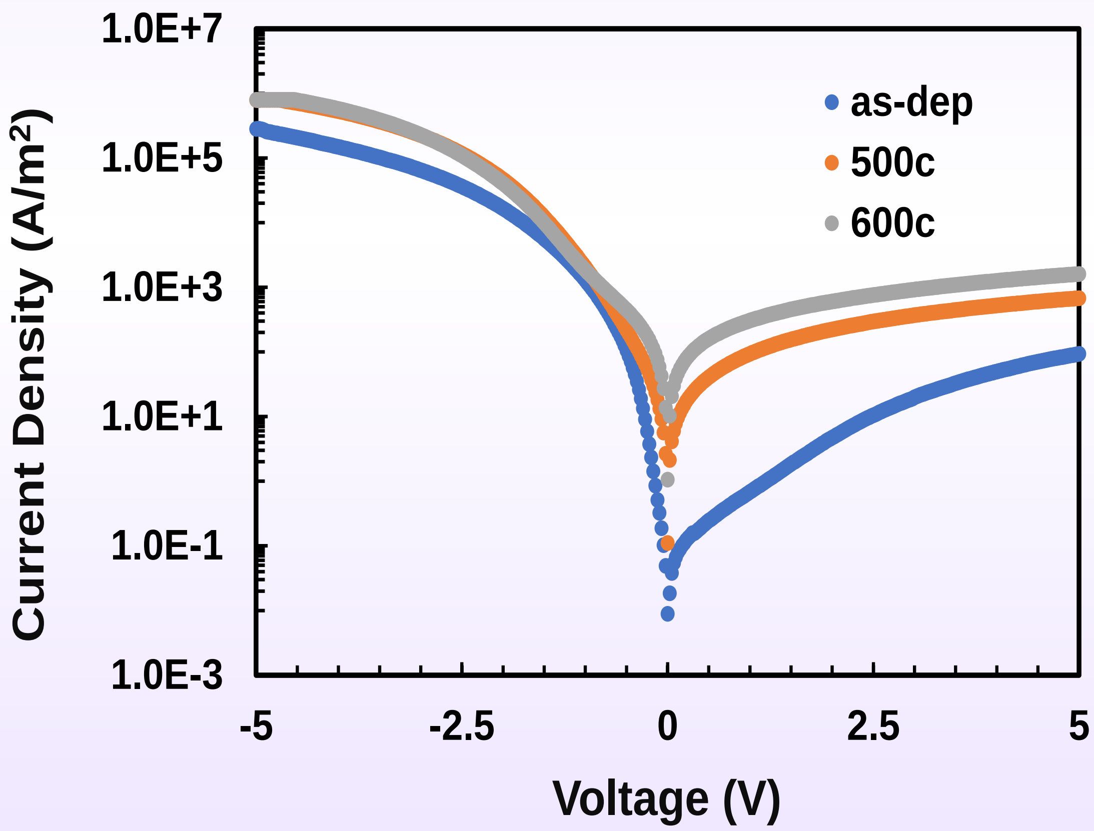
D_{it} also decreased with annealing temperature

I-V MEASUREMENT PLOTS

Sample sputtered for 5 min:

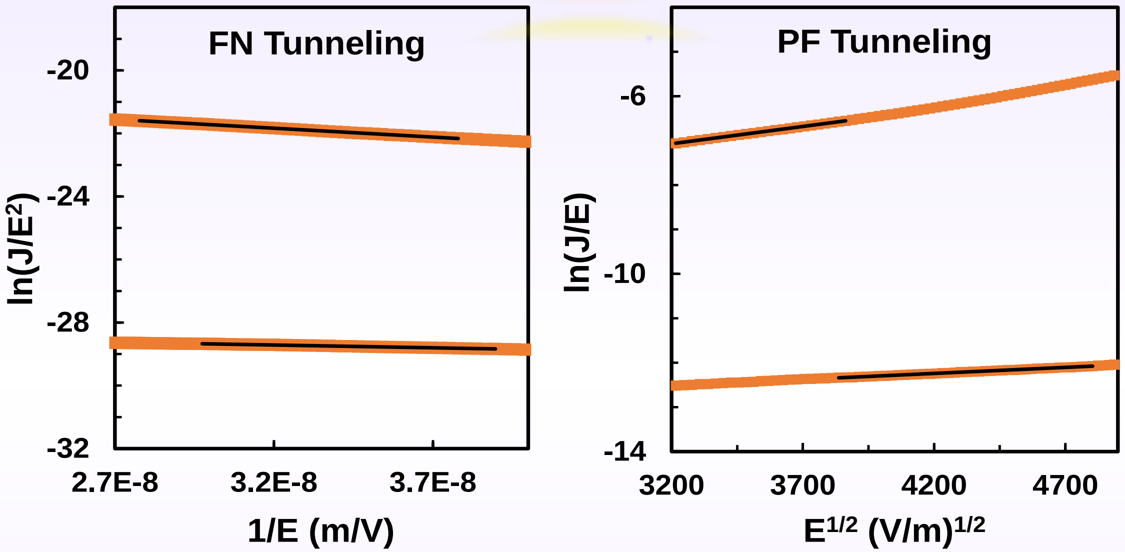


Sample sputtered for 10 min:

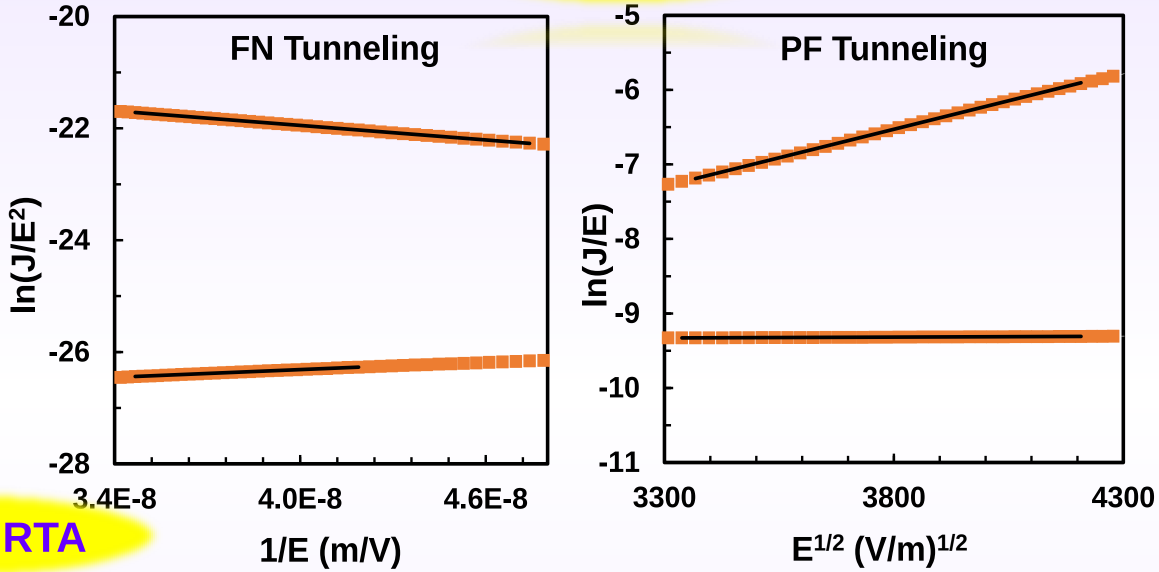


TUNNELING MECHANISMS (sputtered for 5 min)

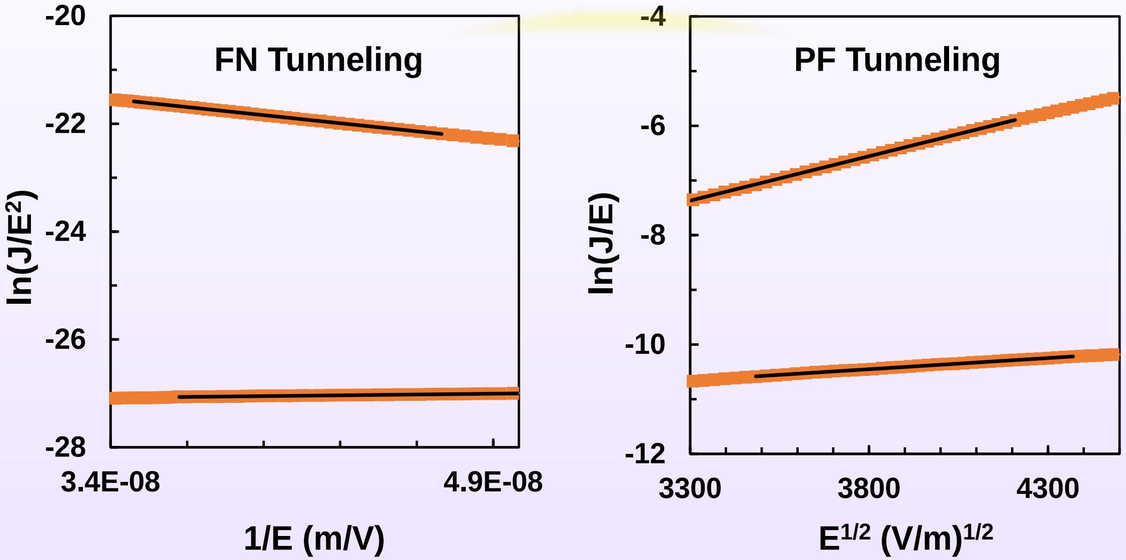
As- dep



500 °C RTA



600 °C RTA



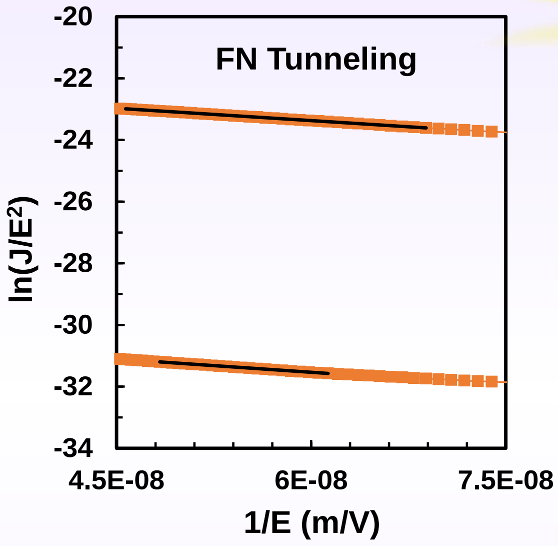
φ_B and φ_t comparison

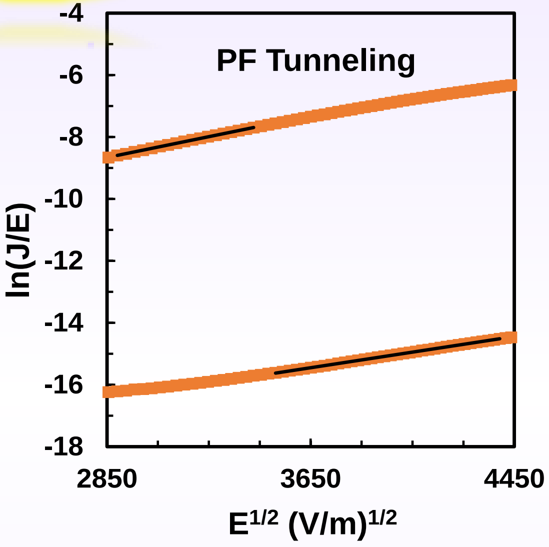
ANNEALING TEMPERATURE	FN		PF	
	φ_{Bn}	φ_{Bp}	φ_{tn}	φ_{tp}
As-dep	1.9	0.9	0.24	0.34
500^{o}C	1.4	0.9	0.32	0.24
600^{o}C	1.6	0.3	0.33	0.31

- The triangular barrier hight φ_B decreases after annealing in both accumulation and inversion
- The trap energy barrier φ_t increases in inversion but decreases in accumulation.

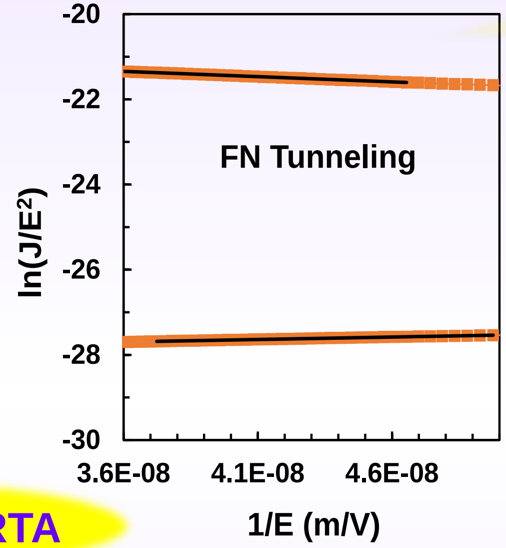
TUNNELING MECHANISMS (sputtered for 10 min)

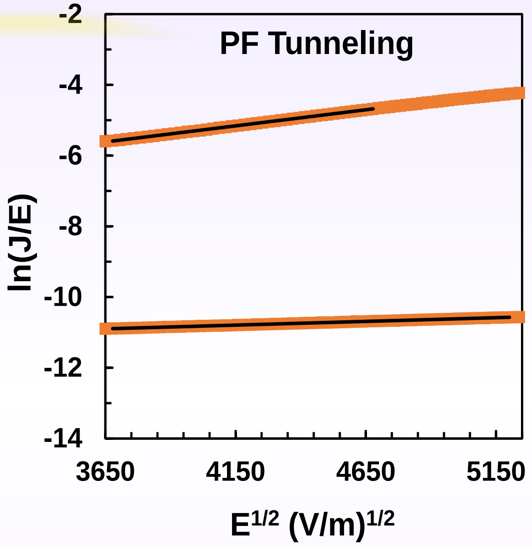
As- dep



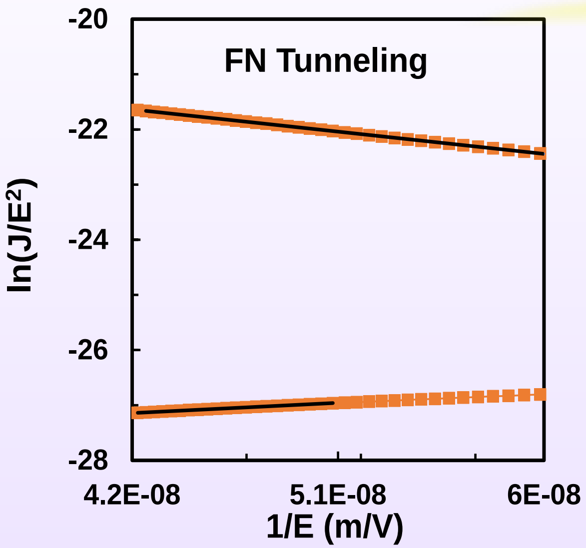


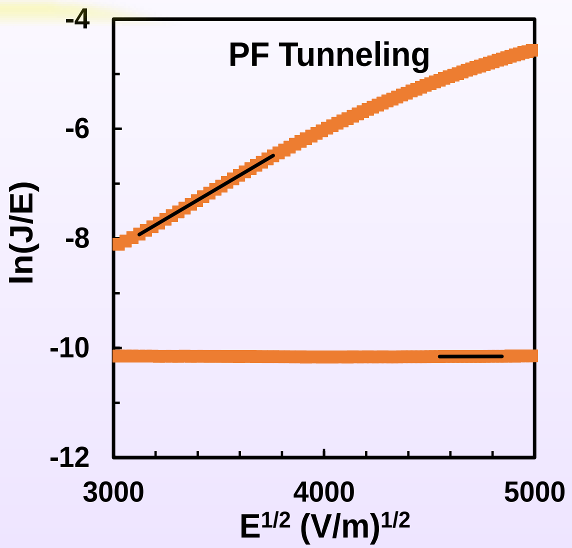
500 °C RTA





600 °C RTA





φ_B and φ_t comparison

ANNEALING TEMPERATURE	FN		PF	
	φ_{Bn}	φ_{Bp}	φ_{tn}	φ_{tp}
As-dep	1.2	1.2	0.39	0.264
500ºC	0.5	0.9	0.23	0.30
600ºC	1.4	0.9	0.39	0.264

- The triangular barrier hight φ_B decreases for 500ºC then increases for 600ºC in inversion but decreases with annealing in accumulation
- The trap energy barrier φ_t decreases in inversion for 500ºC but in accumulation inversion for 500ºC increases.

Comparison of Voltage across oxide

Sample sputtered for 5 min:

ANNEALING TEMPERATURE	V_{ox} (V) [FN]	V_{ox} (V) [PF]
As-dep	0.19 - 0.13	0.107 - 0.0535
500°C	0.128 - 0.096	0.0828 - 0.0506
600°C	0.383 - 0.13	0.051 - 0.088

Sample sputtered for 10 min:

ANNEALING TEMPERATURE	V_{ox} (V) [FN]	V_{ox} (V) [PF]
As-dep	0.101 - 0.201	0.059-0.079
500°C	0.131 - 0.177	0.088-0.1
600°C	0.107 -0.15	0.06-0.1

Comparison of applied field

Sample sputtered for 5 min:

ANNEALING TEMPERATURE	V (V) [FN]	V (V) [PF]
As-dep	-3.325 - -4.525 & 3.325 - 4.225	-1.375 - -1.95 & 1.775 – 2.825
500^{o}C	-3.635 - -2.65 & 3 – 3.575	-2.25 - -1.45 & 1.374 – 2.2
600^{o}C	-3.6 - -2.675 & 2.35 – 3.425	-2.225 - -1.35 & 1.525 – 2.4

Sample sputtered for 10 min:

ANNEALING TEMPERATURE	V(V) [FN]	V(V) [PF]
As-dep	-2.75 - -1.825 & 2.05 – 2.6	-1.475 - -1.05 & 1.55 – 2.425
500^{o}C	-3.5 - -2.7 & 2.525 – 3.375	-2.75 - -1.7 & 1.7 – 3.4
600^{o}C	-2.95 - -2.075 & 2.475 – 2.975	-1.925 - -1.1 & 2.075 – 3.075

- **It is evident that FN tunnelling is dominant in high applied field where as PF is dominant in low applied field.**

CONCLUSION

- Thickness of a Pt/HfO_2/p-Si MOS capacitor decreases negligibly with annealing temperature and increases with increased sputtering time
- With increasing annealing temperature a positive flat band shift occurs
- The effective oxide charge density as well as the interface state density decreases with increasing annealing temperature
- The triangular barrier hight φ_B decreases and trap energy barrier φ_t decreases at 500^{o}C which can be a probable reason for increase of leakage current after annealing.
- FN tunnelling is dominant in high applied field whereas PF is dominant at low applied field.

FUTURE SCOPE

- Explore higher annealing temperature.
- Investigate the effect of substrate heat during deposition.
- Investigate the effect of RF deposition power on film quality.
- Determining the appropriate reason for increase in leakage current after annealing.
- Characterization of traps.

ACKNOWLEDGEMENT

- We express our gratitude to the Department of Electronic science, University of Calcutta for their supports.

- Our deepest thanks also go to our project supervisor, Prof. Anupam Karmakar and Prof. Sanatan Chattapadhay, without whose help and guidance, this project not have been possible.

- We are grateful for the guidance of Mr. Nilayan Paul throughout the project . Our thanks also goes to all scholars in the lab who assisted us.

REFERENCES

1. Ratnesh, Ratneshwar K., A. Goel, G. Kaushik, H. Garg, M. Singh, and B. Prasad. "Advancement and challenges in MOSFET scaling." *Materials Science in Semiconductor Processing* 134 (2021): 106002.
2. Ginez, Olivier, J-M. Portal, and Ch Muller. "Design and test challenges in resistive switching RAM (ReRAM): An electrical model for defect injections." In *2009 14th IEEE European Test Symposium*, pp. 61-66. IEEE, 2009.
3. Sze, Simon M., Yiming Li, and Kwok K. Ng. *Physics of semiconductor devices*. John wiley & sons, 2021.
4. Zhang, J. W., G. He, H. S. Chen, J. Gao, X. F. Chen, P. Jin, D. Q. Xiao, R. Ma, M. Liu, and Z. Q. Sun. "Modulation of charge trapping and current-conduction mechanism of TiO2-doped HfO2 gate dielectrics based MOS capacitors by annealing temperature." *Journal of Alloys and Compounds* 647 (2015): 1054-1060.
5. Manwani, Ajay, Rajesh Junghare, and Abhishek Vaidya. "MODELLING OF TUNNELLING CURRENTS IN METAL-INSULATOR-METAL JUNCTION.
6. S.J. Ding, D.W. Zhang, L.K. Wang, J. Phys. D. Appl. Phys. 40 (2007) 1072e1076.
7. Bentarzi, Hamid.*Transport in metal-oxide-semiconductor structures: mobile ions effects on the oxide properties*. Springer Science & Business Media, 2011.
8. Weinberg, Z. A. "On tunneling in metal-oxide-silicon structures."*Journal of Applied Physics*53, no. 7 (1982): 5052-5056.
9. Depas, Michel, Bert Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, and M. M. Heyns. "Determination of tunnelling parameters in ultra-thin oxide layer poly-Si/SiO2/Si structures." *Solid-state electronics* 38, no. 8 (1995): 1465-1471.

THANK YOU!