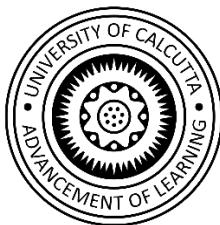


ELECTRICAL CHARACTERIZATION OF RF-SPUTTERED HfO₂ MOS CAPACITOR



Thesis submitted for the degree of

Master of Science (M.sc)

SEM 4

In

Electronics science

By

Sreemoyee Saha

Registration no: 012-1211-0837-19

And

Abhijeet Singh

Registration no: 012-1111-0710-19

Certificate

This is to certify that the project entitled "**ELECTRICAL CHARACTERIZATION OF RF-SPUTTERED HfO₂ MOS CAPACITORS**" by **ABHIJEET SINGH** (Roll no: C91/ELC/221001) Registration No: (012-1111-0710-19) under my guidance for partial fulfilment of the degree of M.Sc. in Electronic Science under **University of Calcutta in 2024.**

This Project is ready for submission.

Supervisor

Dr. Anupam Karmakar

Place: KOLKATA, INDIA

Date: 02/07/2024

Certificate

This is to certify that the project entitled "**ELECTRICAL CHARACTERIZATION OF RF-SPUTTERED HfO₂ MOS CAPACITORS**" by **SREEMOYEE SAHA** (Roll no: C91/ELC/221023) Registration No: (012-1211-0837-19) under my guidance for partial fulfilment of the degree of M.Sc. in Electronic Science under **University of Calcutta in 2024.**

This Project is ready for submission.

Supervisor

Dr. Anupam Karmakar

Place: KOLKATA, INDIA

Date: 02/07/2024

Acknowledgement

I would like to express my gratitude to my project supervisor, Dr ANUPAM KARMAKAR, Professors, Department of Electronic Science, University of Calcutta, for guiding me with his expertise and experience and also for allowing me to work on this topic of my interest.

I would like to extend my gratitude to Mr. Nilayan Paul for contributing immensely to the evolution of my ideas on this project. Her constant support and guidance have helped me to complete my project work on time.

I am also thankful to my class mates and seniors for their constant support throughout this project work.

CONTENTS

1. Introduction
2. Deposition of high-k material
3. Tunneling in Metal-oxide-semiconductor (MOS) structures
4. Tunneling mechanisms in MOS structure
5. Electrical characterization and tunneling mechanisms in MOS
6. Process to fabricate HfO₂ thin film
7. Experimental details
8. Results and discussion
 - 8.1. Ellipsometric analysis
 - 8.2. C-V and G-V measurements:
 - 8.3. Leakage current-conduction mechanism analysis
9. Conclusion
10. Reference

LIST OF FIGURES

	PAGE NO.
Fig. 1 Energy band diagram of ideal MOS capacitor in (a) Accumulation mode, (b) Depletion mode, (c) Inversion mode.	4-5
Fig. 2 Energy-band diagrams showing conduction mechanisms of (a) direct tunneling, (b) Fowler Nordheim tunneling.	6
Fig. 3 Energy-band diagrams showing conduction mechanisms of (c) thermionic emission, and (d) Frenkel-Poole emission.	7
Fig. 4 Energy-band diagram of a metal–silicon dioxide–silicon structure. (a) At zero bias; (b) with large negative bias on the metal electrode; (c) with large positive bias on the metal	8
Fig 5. (i)PF,(ii) Schottky emission (SE) and (iii) FN plots for the MOS capacitor at different annealing temperatures for gate injection.	10
Fig. 6. Conduction mechanism fitting of 600 °C annealed HfO ₂ thin film under gate injection. (a) The curve of Ln (J/V) vs (V) ^{1/2} in moderate electric field (_1.5Vto _3.5 V) P–F fitting. (b)The curve of Ln (J/V ²) vs1/V in high electric field (_3.5 V to _4 V) F–N fitting	11

Fig. 7:	Leakage current density with respect to different annealing temperatures	11
Fig. 8	High frequency CeV characteristics of Al/HfO ₂ /p-Si MOS capacitor annealed at different temperatures (350, 550 and 750 °C).	12
Fig. 9	Low frequency and high frequency C-V characteristics of the HfO ₂ thin film	12
Fig. 10	Block diagram of vacuum system.	13
Fig: 11	Schematic diagram of Spectroscopic ellipsometry	16
Fig 12.	Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b)500°C, (c)600°C.	17
Fig 13.	Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a). as dep, (b)500°C, (c)600°C	18
Fig 14.	Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO ₂ /p-Si MOS., capacitor sputtered for 20 min and annealed at different temperatures (a) as dep, (b)500°C (c)600°C	19

Fig 15.	. Capacitance voltage plot of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies.	21
Fig 16.	: Capacitance voltage plot of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies	22
Fig 17.	. High frequency C-V characteristics of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min as deposited and annealed at different temperatures (500 °C and 600 °C).	23
Fig 18.	. Low frequency C-V characteristics of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min as deposited and annealed at different temperatures (500 °C and 600 °C).	24
Fig 19.	High frequency C-V characteristics of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 10 min as deposited and annealed at different temperatures (500 °C and 600 °C).	25
Fig 20.	Low frequency C-V characteristics of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 10 min as deposited and annealed at different temperatures (500 °C and 600 °C).	26
Fig 21.	Conductance voltage plot of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies	27
Fig 22.	Conductance voltage plot of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies	27
Fig 23.	J-V characteristics of Pt/HfO ₂ /p-Si MOS capacitor sputtered for (a) 5 min and (b) 10 mins annealed at different temperatures (as dep, 500 °C, 600 °C).	28
Fig 24.	Fowler- Nordheim tunneling mechanism of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C.	29
Fig 25.	Pool- Frenkel emission mechanism of Pt/HfO ₂ /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C.	30

- Fig 26.** Fowler- Nordheim tunneling mechanism of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C. 32
- Fig 27.** Pool- Frenkel emission mechanism of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C 33

1. Introduction:

The prime building block of the semiconductor electronics industry is the CMOS based devices. Although the first integrated circuits were designed with a restricted number of CMOS devices, the need for increased speed and functionality in a miniaturized package eventually increased the need for greater number of transistors with smaller footprint. In the year of 1965 Gordon E. Moore, the co-founder of Intel described a law which states that the number of transistors in an IC will be doubled every two years [1]. So, to achieve the large scale and very large-scale integration, downscaling appeared to be the most appropriate solution [2, 3]. Scaling of a MOS transistor is concerned with reducing the dimension of the device, it deals with the change in the device characteristics with the decrease in the dimensions of a MOS transistor [5]. The primary advantages of scaling are improved circuit performance, functional capacity and device density which enables more complex functionality as more numbers of transistors can be integrated in a single chip [4, 5]. This not only makes the circuit less expensive and more compact; it also leads to increased performance and speed. However, making a chip with a large number of the transistors comes with its own difficulties such as short channel effects (SCE), which occur because of reducing the dimensions of the transistor. SCE occurs when the gate terminal of a transistor is not fully shielded from the channel connecting source and drain terminal. Therefore, the main concern here is to diminish the effects of short channel effects and hence to build more efficient downsized FETs [6]. But as the amount of scaling increased, the significantly decreased oxide thickness gives rise to the quantum mechanical tunneling phenomenon due to high electric fields inside the transistor. This degraded the device reliability and increased the leakage current [4]. According to International technology roadmap for semiconductors (ITRS) the flow of current through the gate in a device is directly affected by the reduction of oxide thickness [2]. The oxide thickness is exponentially connected to the gate current where carrier tunneling through the insulator potential barrier leads to leakage current [2]. Quantum mechanically, tunneling is a phenomenon where a particle can penetrate a potential barrier even if the energy of the particle is less than that of the potential barrier [7]. In conventional MOS based semiconductor devices, tunneling is referred to conduction of electrons through oxide layer or above the conduction band of the oxide layer due to phenomena such as charges at the interface region, oxide trap charges, high applied field, high energy of electrons, emission of trapped electrons into conduction band through thermal excitation [7]. To reduce

tunneling of carriers a good quality insulator is needed and high k dielectrics can be a good replacement for ~nm thin SiO₂ in MOS [8]. The compatibility of polysilicon gate electrodes with high dielectric constant (high-k) insulators also raises challenges with CMOS process integration. Most high-k (HK) metal oxides that used as a gate insulator react with polysilicon and degrade the gate dielectric. Furthermore, this interaction makes it difficult to control the MOSFET threshold voltage [9]. HK dielectrics react with the adjacent Si bulk and poly-Si gate electrode, producing abundant defective bonds at the interfaces. It can become polycrystalline at the temperatures used during the fabrication process of the MOSFET, which increases the inhomogeneity of the film and can easily produce defect-rich locations, such as grain boundaries (GBs). The presence of defects in the HK dielectric is problematic because it can increase the source-to-gate and drain-to-gate leakage current, increasing the power consumption and resulting in further defect generation and mobility degradation, which impoverishes the overall reliability of the device [10]. Therefore, to improve device performance, it is crucial to optimize the dielectric material, and thereby, its defect distributions. In this context, the study of leakage current is of great importance for optimizing the dielectrics in terms of defect generation for implementation in MOS and MOS based memory devices. For such purpose, studying the tunneling mechanisms from the current characteristics can lead to the identification of different types of defects, created during fabrication, or inherited in the crystal structure or artificially injected [11]. Different characteristics of the leakage current is observed for different tunneling mechanisms [12]. Therefore, the quality of an insulator can be determined by observing the leakage current of a semiconductor device. Better the quality of the insulator the lesser will be the leakage current.

2. Deposition of high-k materials:

The high k dielectric materials that could potentially replace SiO₂ are SiN, TiO₂, Ta₂O₅, Al₂O₃, HfO₂, ZrO₂. Unfortunately, many of these materials are thermodynamically unstable on silicon and form poor interface with it. It is also well known that high-k film gate oxide structure has considerable bulk and interface charges. These charges are formed during high- k deposition and/or during post deposition processing. Improving the quality of the deposited oxide is essential for MOS device application. Despite such challenges, HfO₂ has emerged as the most promising high k dielectric, as it has high dielectric constant (25), high heat of formation (271 K cal/mol), high band gap (5.8 eV), compatibility with polysilicon gate process and good thermal stability with silicon [13]. As-deposited HfO₂ thin films

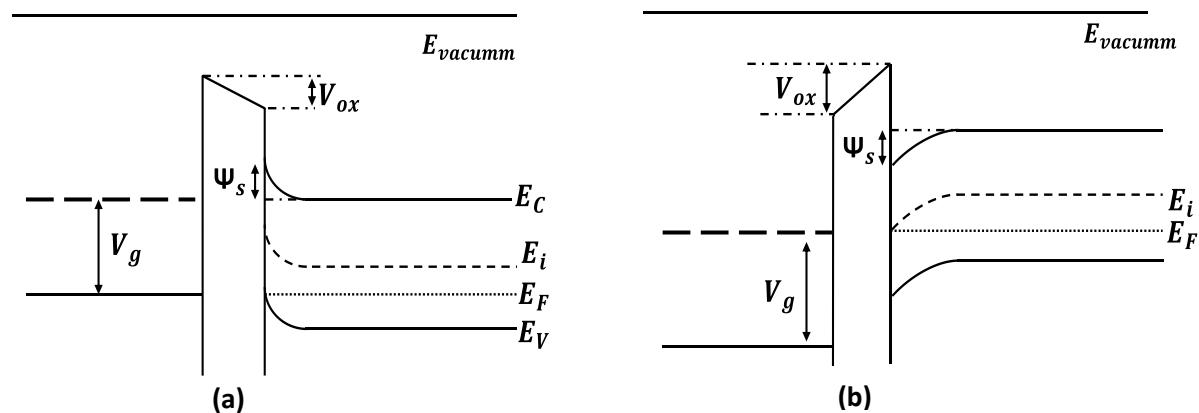
have large number of defects resulting in increased oxide charge and leakage current [14, 15, 16]. Therefore, the deposition process involved is an important factor in determining the quality of such films. RF sputtering is generally preferred due to the possibility of low temperature processing and the processs implicity. However, process optimization in terms of power, sputtering time, substrate temperature and ambient gas pressure is necessary.

To improve the characteristics of the sputtered samples, post deposition annealing is a crucial step. As with the change in annealing temperature the structural phase of the sputtered HfO₂ changes and we can observe monoclinic phase of HfO₂ at higher annealing temperatures [17, 18]. The leakage current also gradually increases eventually with the increase in the annealing temperature but later after a certain temperature it decreases [19] which holds good electric reliability of the device [20]. Hence it can be said that annealing makes a device more electrically reliable. The oxide capacitance (C_{ox}) is found to rise with annealing temperature going from initially, indicating improvement in oxide stoichiometry with annealing. Since higher annealing temperature or longer duration stimulates the local crystallization of HfO₂ and with it the growth of low-k interface layer between silicon and the bulk HfO₂, the effective oxide capacitance falls after a certain temperature of annealing [19]. Frequency dispersion of C-V characteristics also decreases with increasing annealing temperature [20]. The frequency dispersion in the accumulation region occurs mainly due to the presence of an inhomogeneous layer at the oxide semiconductor interface [20]. The difference in accumulation capacitance at low and high frequencies may be attributed to the fact that the trap state scan responds at low frequencies, whereas they do not respond at high frequencies [21]. A positive flat band shift is observed at low annealing temperatures whereas as temperature increases a negative shift can be observed [20]. Accumulation of positive charge at the oxide/semi-conductor interface is responsible for this negative flat-band shift whereas the positive shift of flat band value can be correlated to some kind of rebuild in the bulk layer due to annealing at lower temperatures which ultimately results in decrease of effective oxide charge density (Q_{eff}) value. Also, the interface charge density (D_{it}) decreases with increasing annealing temperature [20].

3. Tunneling in Metal-oxide-semiconductor (MOS) structures:

The metal-oxide-semiconductor (MOS) device is one of the most fundamental and important devices in the study of the physics of semiconductor devices. In an ideal MOS we observe three types of modes,

- **Accumulation-** When a small amount of negative (for p- type) or positive (for n- type) bias is applied the majority carriers accumulate on the SiO_2/Si interface and the energy bands bend upwards or downwards for p- type and n- type MOS, respectively. So due to presence of carriers at metal- oxide and oxide semiconductor interface tunneling of electrons carriers takes place from gate to the semiconductor for a p- type and from semiconductor to the gate for n- type MOS, but the amount of tunneling is respectively low.
- **Depletion-** When small amount of positive (for p- type) or negative (for n- type) bias is applied to the gate terminal the majority carriers then get depleted and the energy bands near the semiconductor surface bends downwards for p- type and upwards for n- type semiconductor.
- **Inversion-** When the applied voltage is increased further the bands bend more and eventually crosses the intrinsic Fermi level and as a result, excess minority carriers get induced at Oxide/Si interface. In such condition, depending on the oxide thickness and applied bias, the minority carriers can also tunnel to the metal contact, which lead to minority carrier-driven tunneling current.



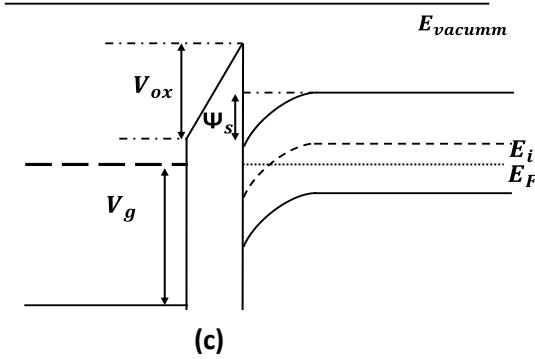


Fig 1: Energy band diagram of ideal MOS capacitor in **(a)** Accumulation mode, **(b)** Depletion mode, **(c)** Inversion mode.

4. Tunneling mechanisms in MOS structure:

Due to scaling of the oxide layer in MOS structure, carriers can escape through it into the metal region. Such process is known as tunneling and it affects the ideal characteristics of MOS. The major tunneling mechanisms in MOS structures are as follows:

i. Direct tunneling:

Direct tunneling is when the tunneling of carriers takes place through the entire width of the insulator. The current due to this tunneling becomes significant for oxides of thickness less than 50Å [22]. To calculate tunneling current we need to know the number of electrons suspected to travel by tunnel effect, the energy distribution of these electrons (given by Fermi–Dirac distribution function), and the transmission or tunneling probability of an electron with energy E that would cross the barrier [23]. Then we can approximately calculate the general equation of tunneling current density, given by [24],

$$J = \frac{4\pi q m_o}{h^3} \int_{E_C}^{E_{max}} T(E) kT \ln \left(1 + \exp \left(-\frac{E - E_F}{kT} \right) \right) dE \quad (1)$$

where $E_{max}=q\phi$ and m_o is the free electron mass. For the direct tunnel conduction, the current density can be evaluated from Eq. (1). Then its approximation can be formulated by [25,26],

$$J = \frac{q^2 m_o \zeta_{ox}^2}{8\pi h (q\phi - E_F) m_{ox}} \left[1 - \left(1 - \frac{q\zeta_{ox} t_{ox}}{q\phi - E_F} \right)^{1/2} \right]^2 \times \exp \left(\frac{-4\sqrt{2m_{ox}}}{3\hbar q \zeta_{ox}} [(q\phi - E_F)^{3/2} - (q\phi - E_F - q\zeta_{ox} t_{ox})^{3/2}] \right) \quad (2)$$

where, m_{ox} is the effective electron mass in the oxide. $q\phi$ is the barrier height at the oxide-silicon interface, ζ_{ox} the electric field strength in the oxide, and h the Plank's constant.

ii. The Fowler- Nordheim Tunneling:

The F-N tunneling takes place at a high applied field. The tunneling of carrier occurs only through partial width of the insulator, hence both average potential barrier height and tunneling distance is less than that of direct tunneling [7]. The current density for F-N tunneling can be derived from Eq. 3, and is given by [27],

$$J = \frac{q^2 m_{si} \zeta_{ox}^2}{8\pi h (q\phi - E_F) m_{ox}} \exp \left(\frac{-4\sqrt{2m_{ox}}}{3\hbar q \zeta_{ox}} [(q\phi - E_F)^{3/2}] \right) \quad (3)$$

It has been estimated that direct tunneling dominates for oxides thinner than 40 Å and FN-tunneling for oxides over 50 Å. This phenomenon, has been used to determine the oxide thickness [28]

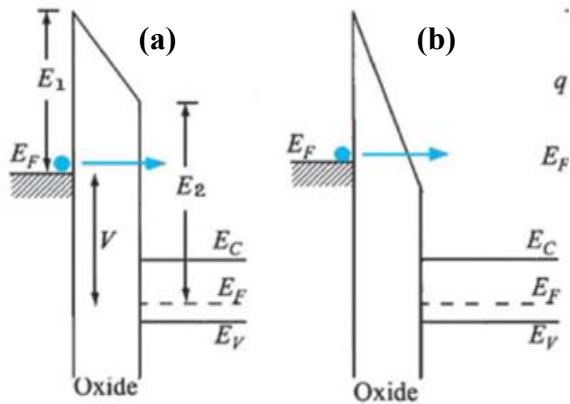


Fig 2: Energy-band diagrams showing conduction mechanisms of (a) direct tunneling; (b) Fowler Nordheim tunneling.

iii. Thermionic emission or Schottky emission:

This emission process takes place when the electron has sufficient energy to overcome the insulator semiconductor barrier [7]. In other words, Schottky current is a result of electrons that moves above the potential barrier i.e., those which has an energy $E > q\phi$ [22]. This current is proportional to the electron density with energies above the barrier height, therefore, for the MOS capacitor the current is proportional to $\exp(q\phi_B/kT)$ [7]. It increases exponentially with decreasing barrier height and increasing temperature [7]. And can be expressed as [23],

$$J = \frac{4\pi n^* q k^2 T^2}{h^3} \exp\left(-\frac{q\phi}{kT}\right) \exp\left(\frac{q}{kT} \sqrt{\frac{q\zeta_{ox}}{4\pi\epsilon_o\epsilon_{ox}}}\right) \quad (4)$$

where m^* is the effective mass of electron.

iv. Frenkel- Poole emission:

Emission of trapped electrons into conduction band through thermal excitation is termed as Frenkel- Poole emission [7]. The expression of Frenkel-Poole current for thin oxides is given by [30],

$$J = qN_c \mu_e \zeta_{ox} \exp\left(-\frac{q\phi}{kT}\right) \exp\left(\sqrt{\frac{q}{\pi\epsilon_o\epsilon_{ox}}} \frac{q\sqrt{\zeta_{ox}}}{kT}\right) \quad (5)$$

where N_c is the density of states in the oxide conduction band and μ_e is the mobility of electrons in the oxide.

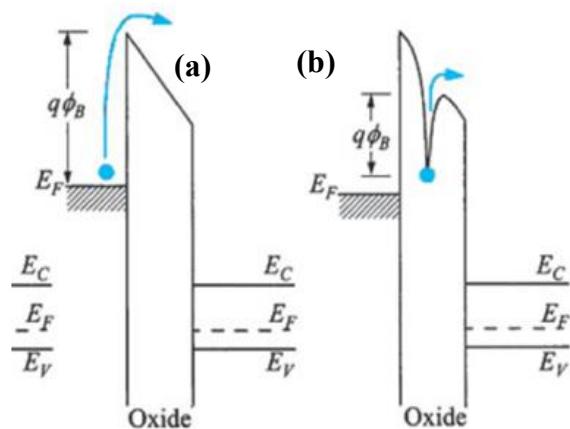


Fig 3: Energy-band diagrams showing conduction mechanisms of (a) thermionic emission, and (b) Frenkel-Poole emission.

5. Electrical characterization and tunneling mechanisms in MOS:

The effects of tunneling on a thin MOS structure can be experimentally determined from the leakage (tunneling) current [31]. For different conduction mechanisms, the dependence of the current with respect to the applied voltage can be checked to understand the conduction mechanisms. For instance, the density of conduction current in conventional SiO_2 (~ 100 nm) films can be excellently described by the classical FN formula [32],

$$J = CE^2 \exp(-\beta/E) \quad (6)$$

where E is the externally applied field while C is the preexponent and β is the slope.

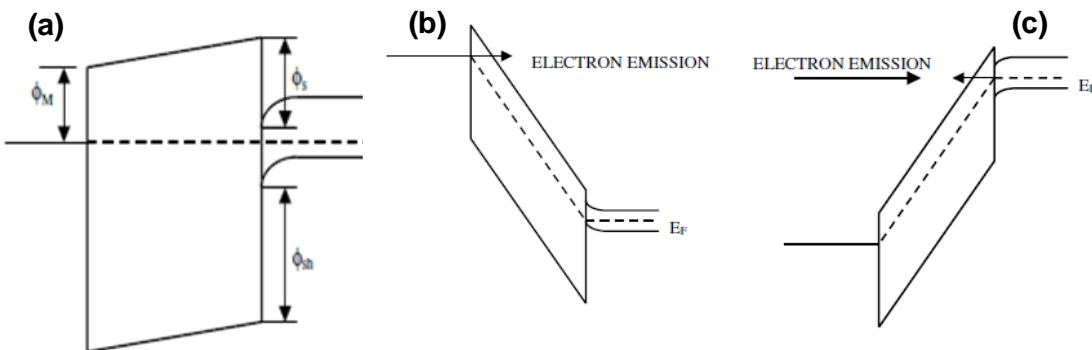


Fig 4: Energy-band diagram of a metal–silicon dioxide–silicon structure. (a) At zero bias; (b) with large negative bias on the metal electrode; (c) with large positive bias on the metal [32].

Fig (4a) illustrates the energy band diagram of MOS structure. ϕ_s is the energy barrier from silicon conduction band to oxide conduction band, while ϕ_{sh} is the barrier for holes from silicon valance band to oxide valance band and lastly energy barrier ϕ_M is the metal work function and it depends on the type of material.

Fig (4b) shows energy band diagram of MOS structure with a negative bias. Schottky emission of electrons over the barrier ϕ_M and FN tunneling of electrons through the triangular barrier, both mechanisms contribute to the current. However, at room temperature, the latter mechanism dominates, leading to F-N tunneling limited current.

Fig. (4c) shows the energy band diagram corresponding to positive bias on the metal. For a large applied bias, the silicon surface is degenerate n-type regardless of the bulk doping. Hence, the silicon can be treated as a metal, and the current is limited by FN tunneling from

the vicinity of the silicon conduction band edge through the triangular barrier into the oxide conduction band. Since the voltage drop in silicon is always less than the silicon bandgap, for large applied voltage, the oxide field is approximately equal to the applied voltage divided by the oxide thickness.

Further, different materials and metals would have different barrier heights for FN injection and the slopes in FN plots are governed by the effective electron or hole mass which also depend on the electrode materials.

However, for further increase in the oxide thickness, the F-N tunnelling mechanism is suppressed [32].

Frenkel-Poole emission is dominant current conduction mechanism at low electric field regions [12] whereas F-N tunnelling mechanism and Schottky emission is dominant in high electric field region for gate injection. Schottky emission is a field-assisted thermionic emission of an electron over a surface barrier. The leakage current density governed by Schottky emission is expressed as [33]

$$J = AT^2 \exp\left[\frac{-q(\Phi_B - \sqrt{qE/4\pi\epsilon_i\epsilon_o})}{KT}\right] \quad (7)$$

where A is effective Richardson constant and $A = 4\pi q(m_{ox})k^2/h^3 = 120(m_{ox}/m_0)$, T, ϕ_B , E, ϵ_o , ϵ_i , k, m_0 , m_{ox} and h are the absolute temperature, the Schottky barrier height, the electric field in oxide, the vacuum permittivity, the dynamic dielectric constant, the Boltzmann constant, the free electron mass, the electron effective mass and the Planck's constant respectively.

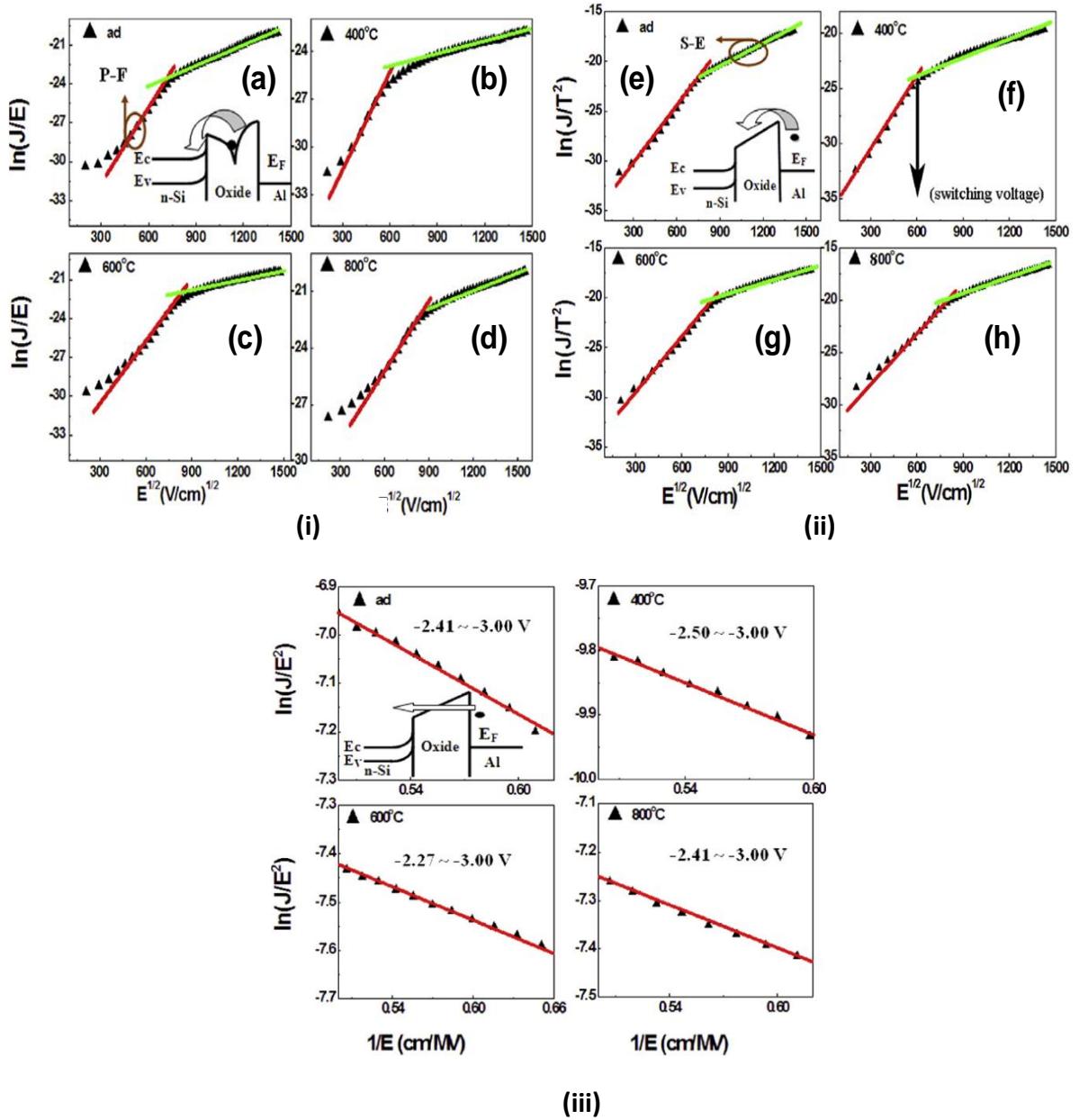


Fig 5: (i) PF, (ii) Schottky emission (SE) and (iii) FN plots for the MOS capacitor at different annealing temperatures for gate injection.

For good quality thin film, the F-N tunneling mechanism becomes secondary, also the 400° annealed sample exhibits the highest threshold voltage in the beginning of this mechanism. Good quality dielectric can be identified if there is an existence of P-F conduction mechanism, it indicates an improved leakage current which in turn refers to better dielectric integrity and reliability [12].

The PF conduction mechanism is bulk limited and depends crucially upon the contribution of traps existing in the bulk of the insulator [20].

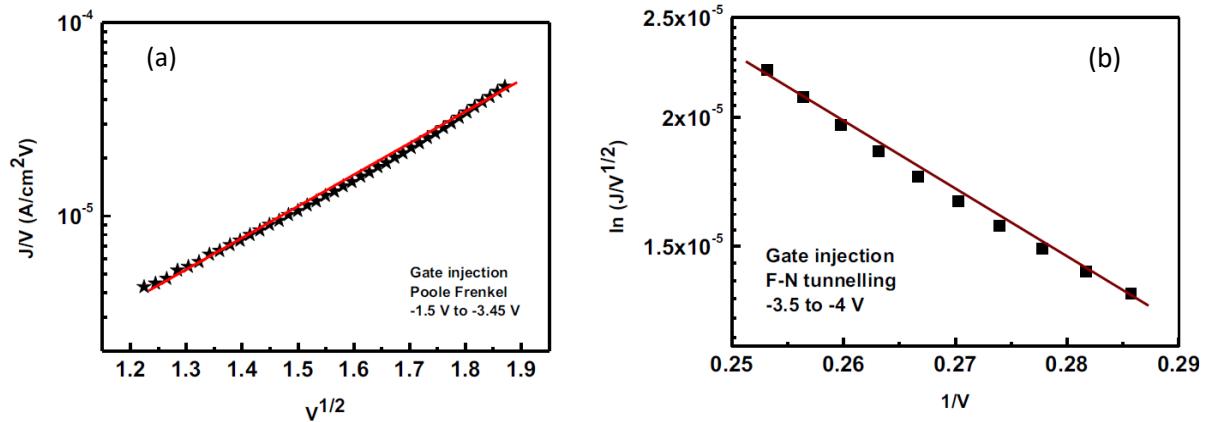


Fig 6: Conduction mechanism fitting of 600 °C annealed HfO₂ thin film under gate injection. (a) The curve of $\ln (J/V)$ vs $(V)^{1/2}$ in moderate electric field (-1.5 V to -3.45 V) P-F fitting. (b) The curve of $\ln (J/V^2)$ vs $1/V$ in high electric field (-3.5 V to -4 V) F-N fitting.

So, in conclusion, P-F emission dominates the variation of leakage current at low oxide field, and Schottky emission dominates the variation of leakage current at high oxide field for gate injection. [20]

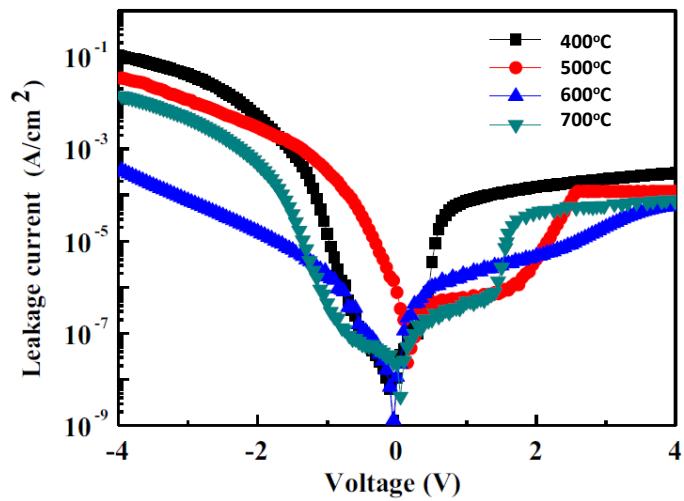


Fig 7: Leakage current density with respect to different annealing temperatures, taken from [35].

It is seen that leakage current decreases with increase of annealing temperature [20, 34]. The accumulation capacitance (C_{ox}) gradually decreases with increasing annealing temperature [19, 35, 36] as shown in Fig 7 [35].

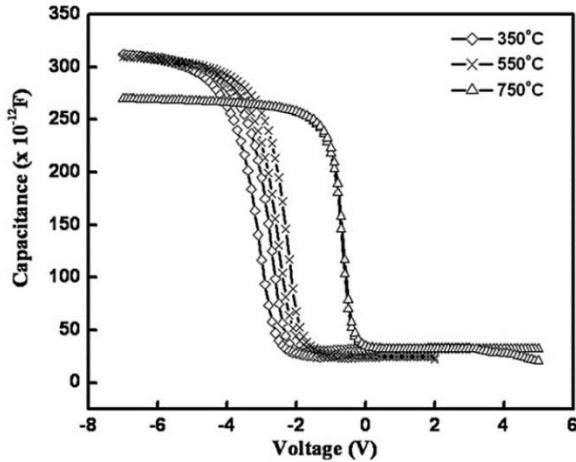


Fig 8: High frequency C-V characteristics of Al/HfO₂/p-Si MOS capacitor annealed at different temperatures (350, 550 and 750°C).

Fig 9 [35] shows Low frequency (<10 kHz) and high frequency (1 MHz) C-V curve of a HfO₂ thin film. From which we can clearly see that as the measurement frequency is lowered, inversion state forms at lower bias and inversion capacitance increases. At lower frequencies minority carriers (electrons) as well as interface traps show capacitive response and inversion capacitance rises [37]. Minority carriers in inversion layer and interface traps begin to respond to a slowly changing ac signal but are unable to follow any high frequency signal. Dispersion observed in the inversion region capacitance is due to large response time of minority carriers. Fig. 9 demonstrates the capacitance voltage (C-V) behaviour measured at 1 MHz frequency of MOS capacitors postdeposition annealed at different temperatures.

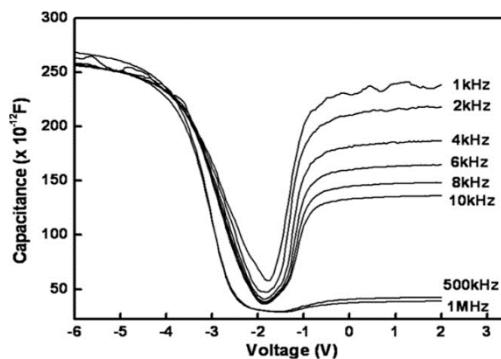


Fig 9: Low frequency and high frequency C-V characteristics of the HfO₂ thin film [35].

6. PROCESSES TO FABRICATE HfO₂ THIN FILM:

The fabrication process of any semiconductor device decides some critical parameters (CV characteristics, thickness, leakage current) of the device and hence its performance. There is a no. of techniques by which oxide/insulators is grown upon the metal surface namely, (i) Thermal oxidation, (ii) Chemical vapour deposition (CVD), (iii) Atomic layer deposition (ALD), (iv) Sputtering (type of Physical vapour deposition (PVD)).

(v) Thermal deposition.

Due to cost effectiveness one of the most common methods is sputtering and which is discussed below

RF sputtering (Radio Frequency sputtering) is a physical vapor deposition (PVD) technique used to deposit thin films of material onto a substrate. It is commonly used for materials that are insulating or have low electrical conductivity. Here's how it works:

1. **Vacuum Chamber:** The process takes place in a vacuum chamber to prevent contamination and to control the environment.

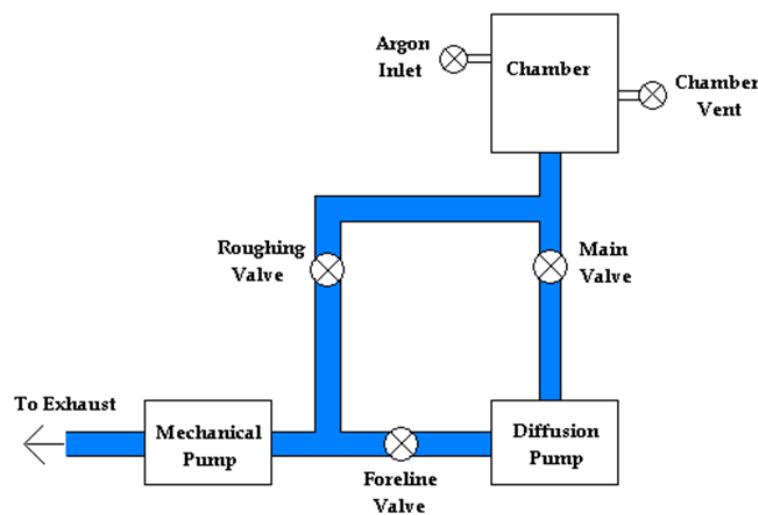


Fig 10: Block diagram of vacuum system.

2. **Target and Substrate:** A target material, which will form the thin film, is placed in the chamber, and the substrate (the material on which the thin film will be deposited) is positioned facing the target.

3. **RF Power Source:** An RF power supply is connected to the target. The radio frequency (typically 13.56 MHz) is used to generate a plasma in the chamber by ionizing a sputtering gas (usually argon).
4. **Plasma Generation:** The RF power creates an alternating electric field that ionizes the gas, forming a plasma. The ions in the plasma are accelerated towards the target material.
5. **Sputtering:** The energetic ions bombard the target, causing atoms or molecules from the target to be ejected (sputtered) into the gas phase.
6. **Film Deposition:** The sputtered atoms then travel through the vacuum and condense on the substrate, forming a thin film.

Advantages of RF Sputtering:

- Suitable for insulating materials: Unlike DC sputtering, RF sputtering can be used for materials that are non-conductive or have low conductivity.
- Uniform films: It can produce uniform and high-quality thin films.
- Complex stoichiometry: RF sputtering can be used to deposit compounds or alloys with complex stoichiometry.

RF sputtering is valued for its versatility and ability to deposit a wide range of materials, including oxides, nitrides, and other insulating compounds.

7. EXPERIMENTAL DETAILS:

The p-type Si<100> substrate was cleaned using standard RCA1 and RCA2 processes. The cleaned Si substrates were then loaded in RF magnetron sputtering system (Advanced process technology) for the deposition of HfO₂ thin films. The thin films were deposited under 10⁻⁶ mbar base pressure. HfO₂ was sputtered in Ar ambient at 2.8 × 10⁻² mbar sputtering pressure. The RF power in the magnetron was maintained at 50 W. HfO₂ thin films of different thicknesses were deposited by varying sputtering time for 5min, 10min and 20min.

After sputtering, the samples were annealed in a rapid thermal process (RTP) furnace in O₂ environment at 500 °C and 600 °C for 30s. The ramp rate was set to ~50 °C/s. Thus, three types of films, i.e., as-deposited, 500 °C anneal and 600 °C anneal were obtained.

The thickness of the as-deposited and annealed films was measured using ellipsometric spectroscopy (Sentech SE500), with HfO₂ supra model. Subsequently, the samples were coated with Pt in a DC table-top sputtering system (Quorum) for 200 s to form the front and back contacts. Shadow mask was used to form the front contacts whereas blanket deposition was carried out to make the back contact.

The electrical properties of the HfO₂ thin films were measured in terms of CV and IV using source meter (Keithley 2612B) and LCR meter (Keysight E4980A) in a probe station

8. RESULTS AND DISCUSSION:

We have characterized our three samples of RF sputtered HfO₂ as deposited, annealed at 500°C and 600°C by (i) ellipsometry, (ii) electrical characterizations (C-V measurements, I-V measurements).

8.1. Ellipsometric analysis:

Spectroscopic ellipsometry (SE) is an optical technique which works on the principle of the change of polarization state of light as it is reflected obliquely from a thin film. It is a non-destructive, non-contact process which uses a model-based approach to determine the thickness and optical properties of thin films of thickness ranging from a few angstroms to several tens of micron.

In spectroscopic ellipsometry, both ψ and Δ is measured which describe the output elliptical polarization state after linearly polarized light is reflected from a thin film sample. The parameters ψ and Δ are related to the complex Fresnel reflection coefficients according to:

$$\rho = \tan(\psi) e^{i\Delta} = R_p / R_s. \quad (8)$$

In order to determine the thickness and optical constant of a thin film, a model representing the thin film structure must be built after collecting ψ and Δ data.

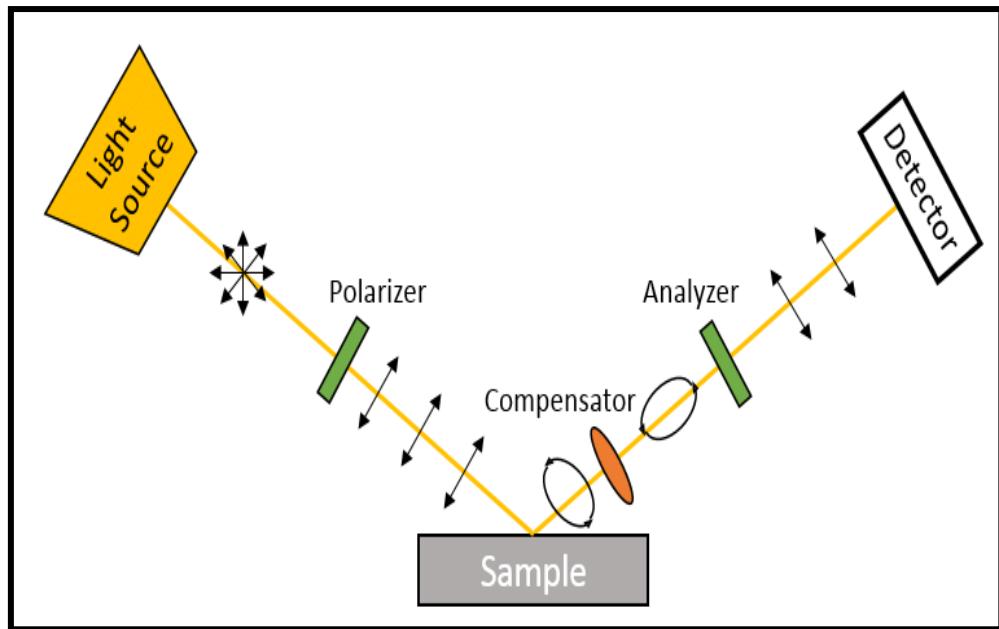


Fig 11: Schematic diagram of Spectroscopic ellipsometry

We have used HfO₂ sopra model [The structure of the model is Air/HfO₂ (sopra)/Silicon<100> (Jellison)] to get the simulated psi delta plots and then fitted them against experimental data. Resulting plots indicate that theoretical model satisfactorily agrees with the experimental data. Which confirms that the material deposited is indeed HfO₂. Upon matching these results the thickness of the layers were calculated from the model parameter.

Fig. 12, 13, 14 show the Psi (Ψ) delta (Δ) plot obtained from the ellipsometric spectroscopy of Pt/HfO₂/Si MOS capacitor for two sample (RF sputtered for 5 mins and RF sputtered for 10 mins to deposit HfO₂) for a wide range of frequencies.

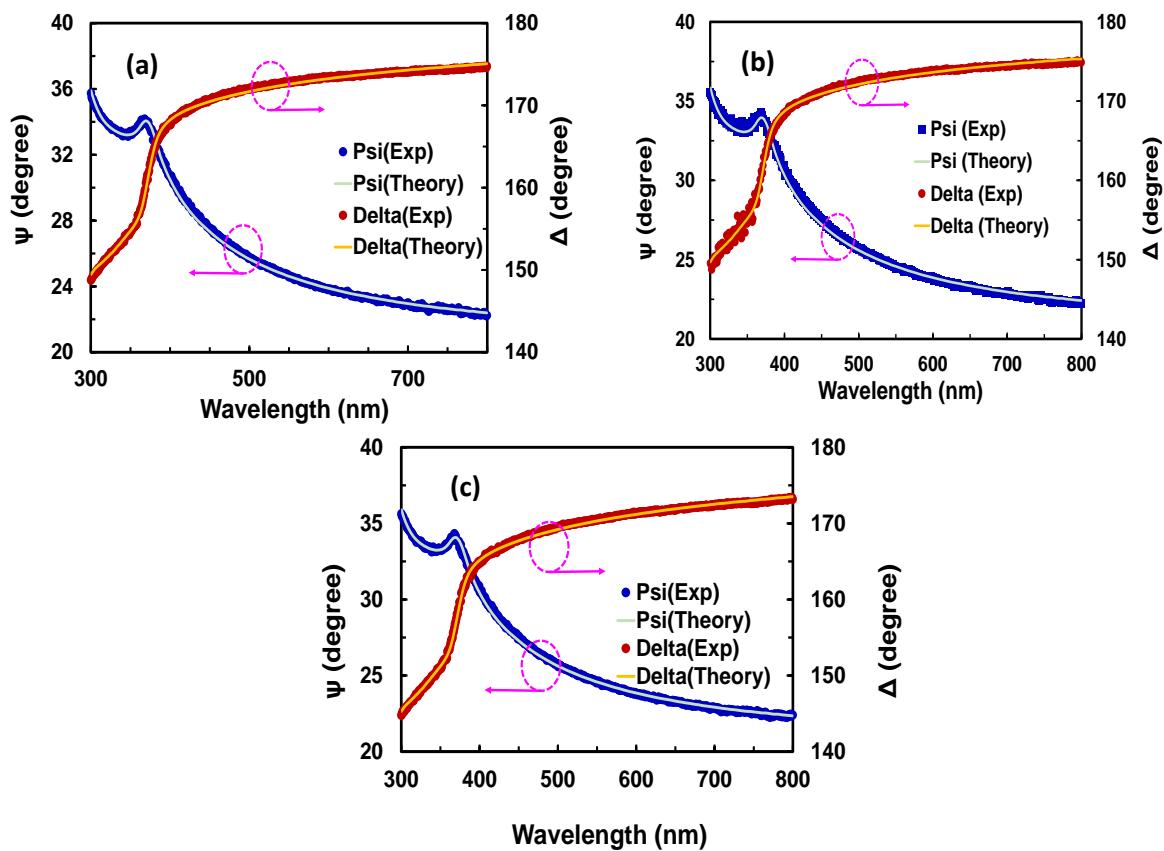


Fig 12: Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500°C, (c) 600°C.

The thickness found for this sample (sputtered for 5 mins) for as dep, annealed at 500°C and 600°C was calculated to be 5.35 nm, 4.60 nm, and 5.65 nm respectively.

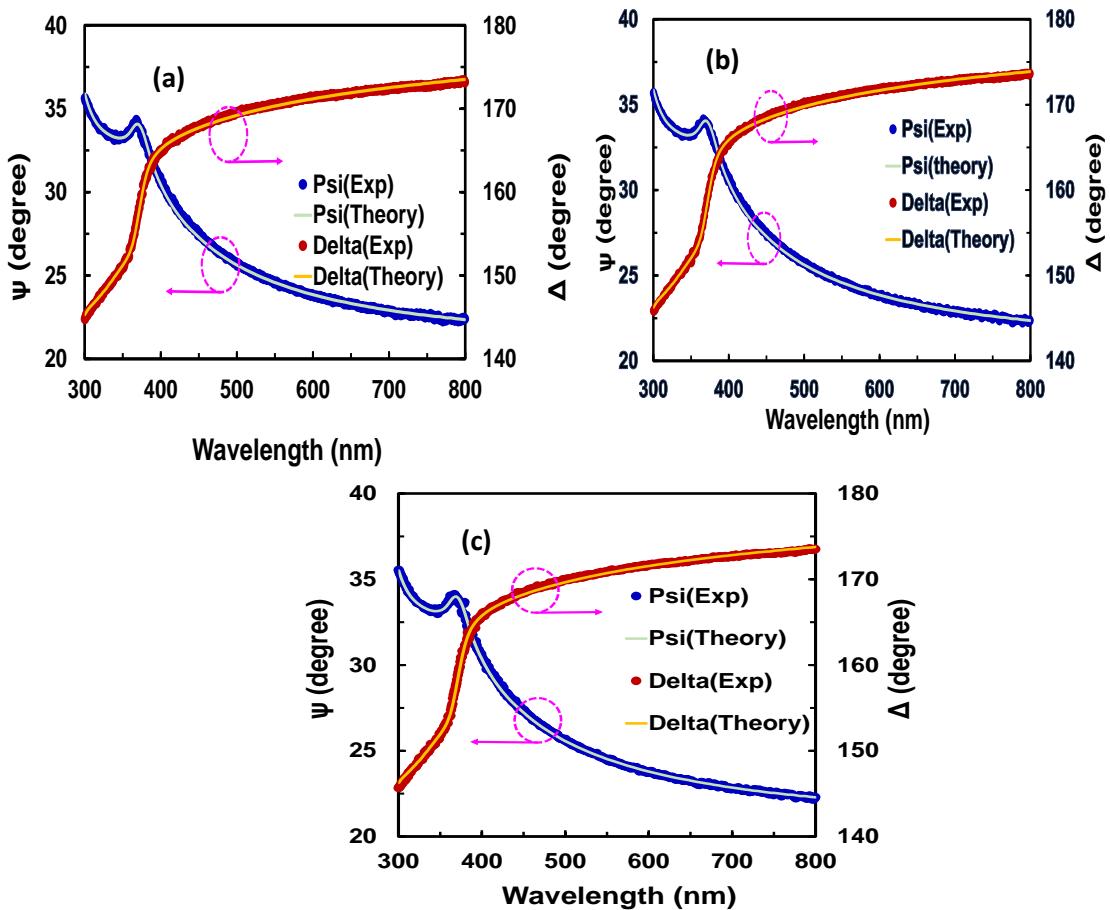


Fig 13: Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a) as dep, (b) 500°C, (c) 600°C.

The thickness found for this sample (sputtered for 10 mins) for as dep, annealed at 500°C and 600°C was calculated to be 7.01 nm, 6.57 nm, and 6.51 nm respectively.

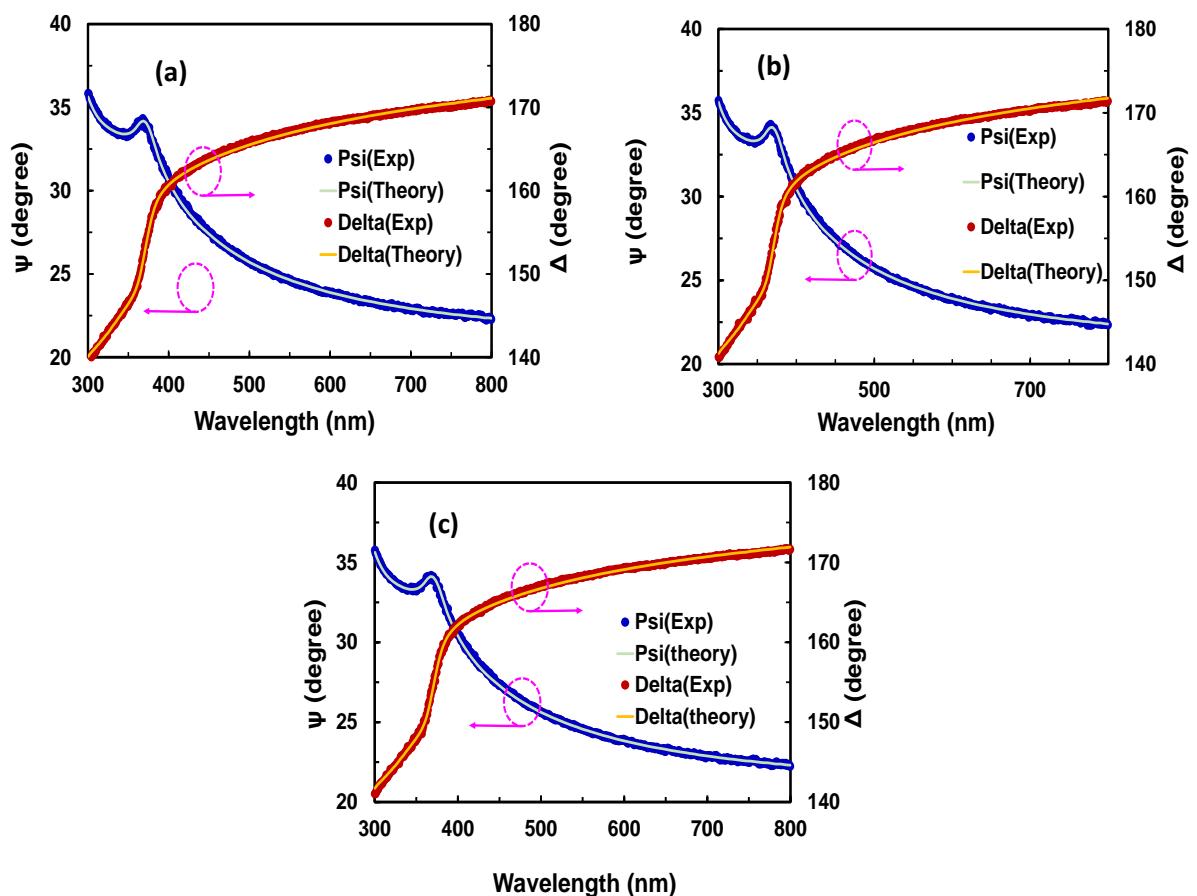


Fig 14: Psi (Ψ) delta (Δ) plot of ellipsometric spectroscopy of Pt/HfO₂/p-Si MOS capacitor sputtered for 20 min and annealed at different temperatures (a) as dep, (b) 500°C, (c) 600°C.

The thickness found for this sample (sputtered for 20 mins) for as dep, annealed at 500°C and 600°C was calculated to be 9.66 nm, 8.82 nm, and 8.72 nm respectively.

From the table no. (1) We can see that the longer a sample has been sputtered thicker is the HfO₂ film. As for the sample sputtered for 20 mins the as deposited film thickness is 9.66 nm. Whereas for the sample sputtered for 5 mins the HfO₂ film thickness is 5.35 nm. And on the other hand, with the increase in annealing temperature the thickness of HfO₂ thin film decreased.

Table: (1): Thickness of the samples from ellipsometric data

Annealing temperature	Sample Thickness (in nm) (sputtered for 5 mins)	Sample Thickness (in nm) (sputtered for 10 mins)	Sample Thickness (in nm) (sputtered for 20 mins)
As- deposited	5.35	7.01	9.66
500°C	4.60	6.57	8.82
600°C	4.65	6.51	8.72

8.2.C-V and G-V measurements:

Capacitance voltage characteristics and conductance voltage characteristics for each sample has been measured for a wide range of frequencies.

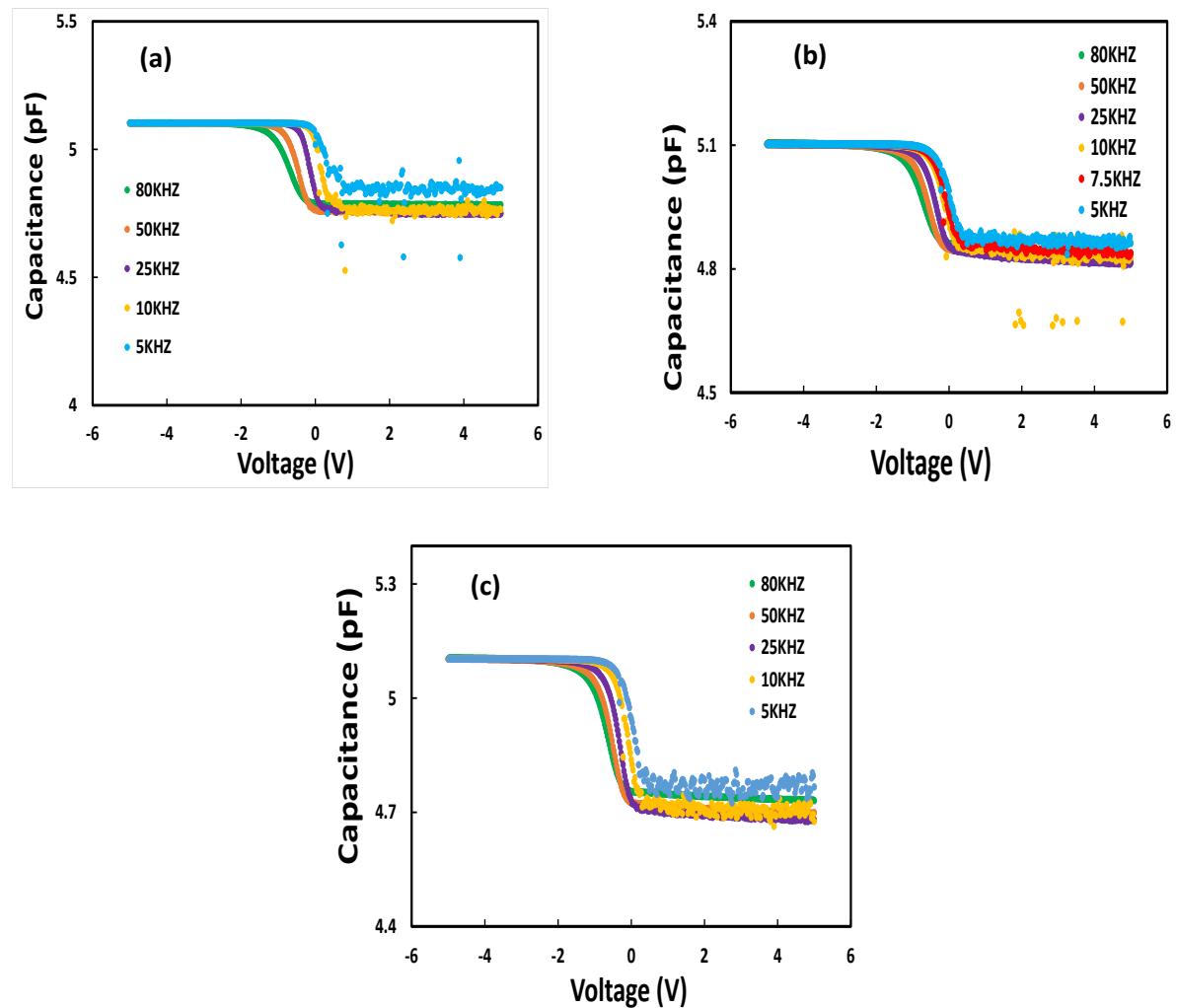


Fig 15: Capacitance voltage plot of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500°C, (c) 600 °C for a range of frequencies.

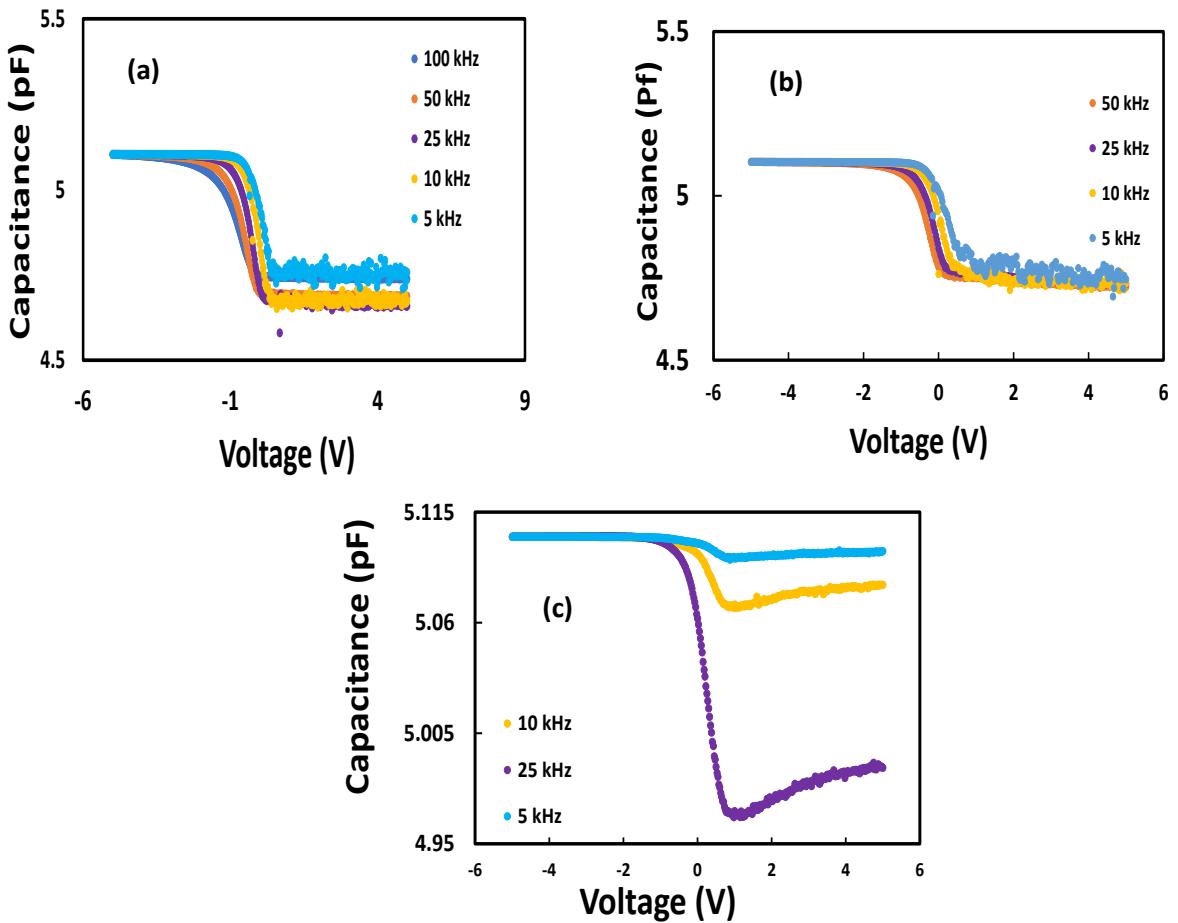


Fig 16: Capacitance voltage plot of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies.

From fig (15) and (16) shows the capacitance voltage characteristics of Pt/HfO₂/Si MOS capacitor for two sample (RF sputtered for 5 mins and RF sputtered for 10 mins to deposit HfO₂) for a wide range of frequencies. It is evident from the figures that there is a frequency dispersion of the capacitance in inversion region. The inversion capacitance for high frequencies is low whereas for low frequencies it becomes high. As at lower frequencies minority carriers (electrons) as well as interface traps show capacitive response and inversion capacitance rises [37]. The dispersion in inversion region may be attributed to large response time of minority carriers [35].

A comparison has been made between high frequency and low frequency capacitance of each sample to observe their change and calculate the effective oxide charge density (Q_{eff}) and interface state density (D_{it}).

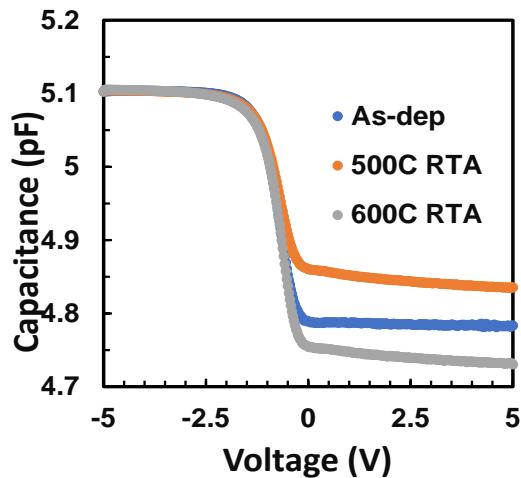


Fig 17: High frequency C-V characteristics of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min as deposited and annealed at different temperatures (500 °C and 600 °C).

Table (2): Q_{eff} and D_{it} comparison at high frequency for sample sputtered for 5 min

Annealing temperature	V_{FB} (V)	Q_{eff} (cm ⁻²)	D_{it} (eV ⁻¹ cm ⁻²)
As-dep	-0.05	1.26×10^{13}	1×10^{14}
500°C	0.075	1.9×10^{13}	5.29×10^{13}
600°C	0.025	6.3×10^{12}	6.48×10^{12}

From table (2) we can observe that the V_{FB} acquires a positive shift after annealing and the Q_{eff} and D_{it} decreases with increasing annealing temperature.

The positive shift of flat band value can be correlated to rebuild in the bulk layer due to annealing at 500 °C and 600 °C which ultimately results in decrease of effective oxide charge density Q_{eff} value [20].

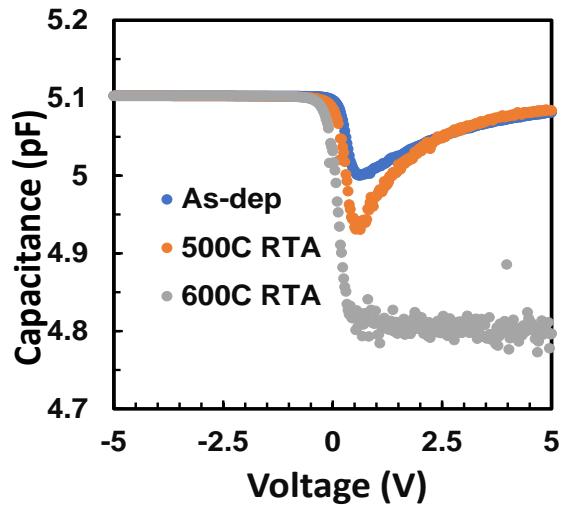


Fig 18: Low frequency C-V characteristics of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min as deposited and annealed at different temperatures (500 °C and 600 °C).

Table (3): Q_{eff} and D_{it} comparison at low frequency for sample sputtered for 5 min

Annealing temperature	V_{FB} (V)	Q_{eff} (cm ⁻²)	D_{it} (eV ⁻¹ cm ⁻²)
As-dep	0.625	1.58×10^{14}	1.7×10^{14}
500C	0.95	2.4×10^{14}	3.47×10^{15}
600C	0.65	1.65×10^{14}	1.17×10^{14}

From table (3) we can observe that the V_{FB} acquires a positive shift after annealing and the Q_{eff} and D_{it} decreases with increasing annealing temperature but the decrease is significantly less than that of high frequencies.

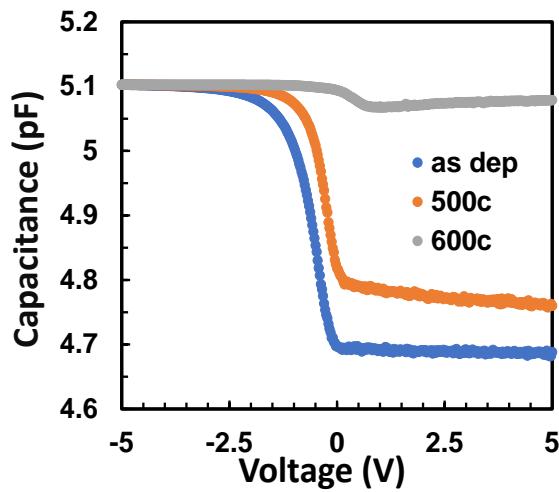


Fig 19: High frequency C-V characteristics of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min as deposited and annealed at different temperatures (500 °C and 600 °C).

Table (4): Q_{eff} and D_{it} comparison at high frequency for sample sputtered for 10 min

Annealing temperature	V_{FB} (V)	Q_{eff} (cm ⁻²)	D_{it} (eV ⁻¹ cm ⁻²)
As-dep	0.1	2.5×10^{13}	8.9×10^{13}
500C	0.275	6.9×10^{13}	9.2×10^{13}
600C	0.9	7.6×10^{12}	5.5×10^{13}

From table (4) we can observe that the V_{FB} acquires a positive shift after annealing and the Q_{eff} and D_{it} decreases with increasing annealing temperature but the improvement is significantly less than that of 5 min sample as the thickness of 10 min sample is more and hence the effective oxide charges and interface states have more area to.

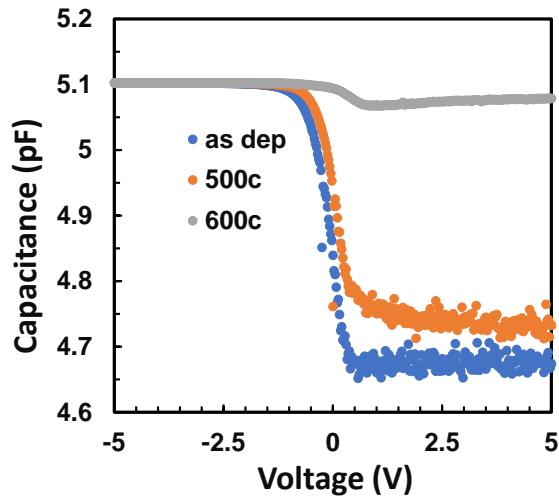


Fig 20: Low frequency C-V characteristics of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min as deposited and annealed at different temperatures (500 °C and 600 °C).

Table (5): Q_{eff} and D_{it} comparison at low frequency for sample sputtered for 10 min

Annealing temperature	V_{FB} (V)	Q_{eff} (cm ⁻²)	D_{it} (eV ⁻¹ cm ⁻²)
As-dep	0.65	7.1×10^{13}	1.1×10^{14}
500C	0.83	2.7×10^{13}	9.4×10^{13}
600C	1.02	2.41×10^{13}	3.6×10^{13}

From table (5) we can observe that the V_{FB} acquires a positive shift after annealing and the Q_{eff} and D_{it} decreases with increasing annealing temperature.

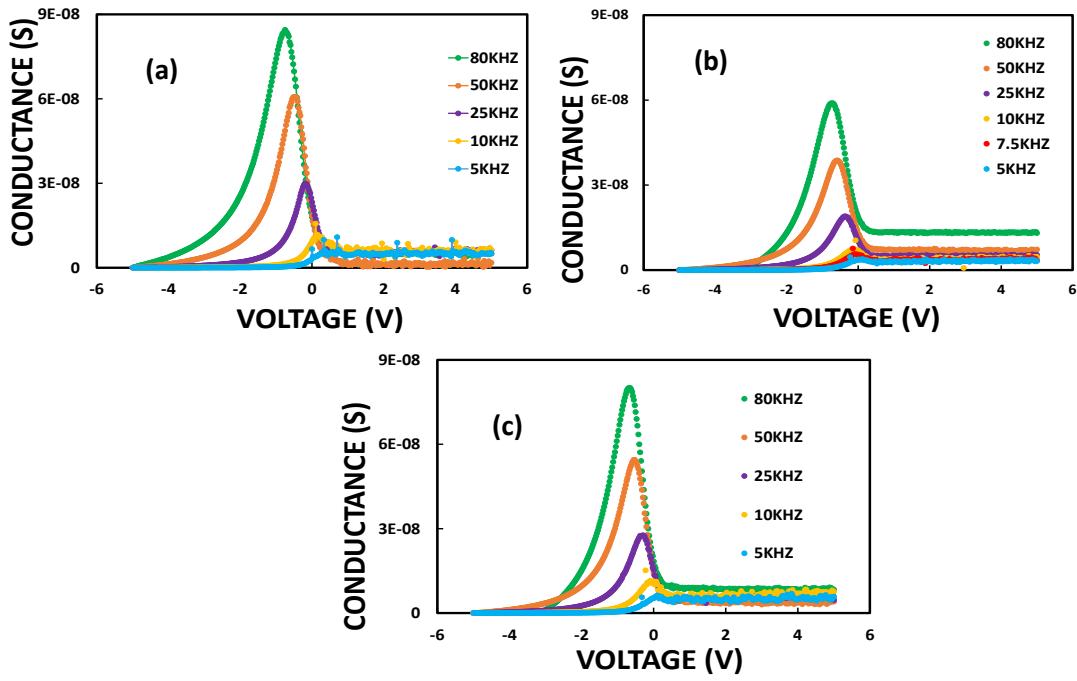


Fig 21: Conductance voltage plot of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies.

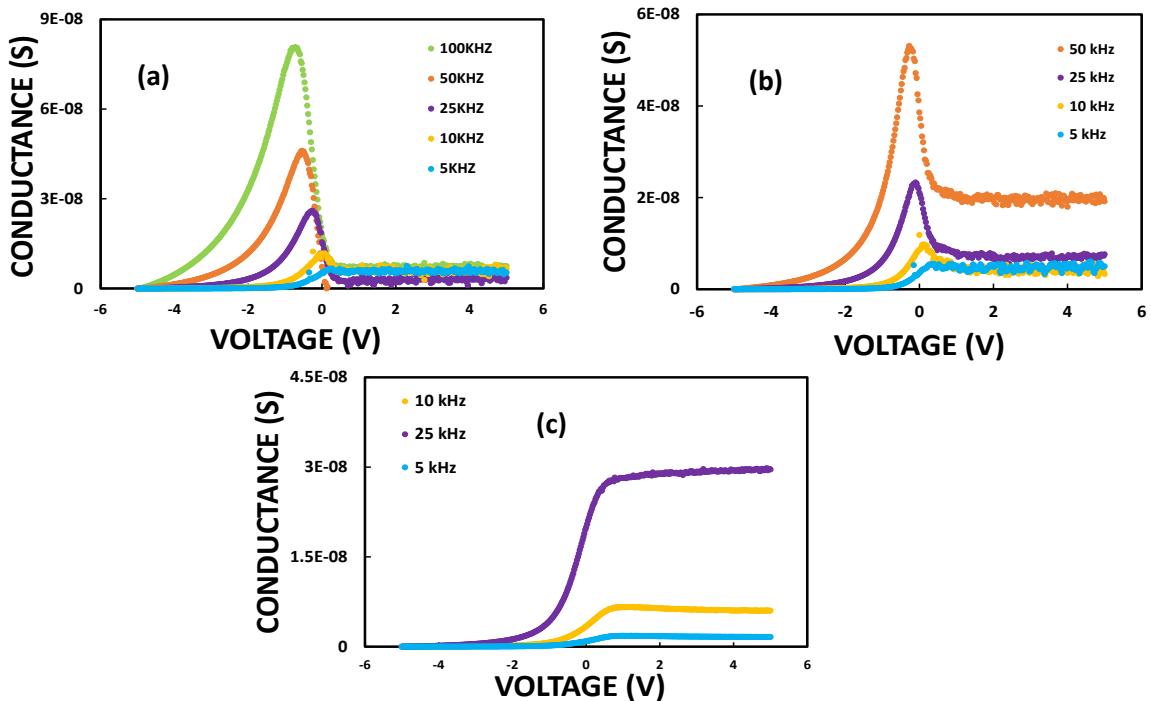


Fig 22: Conductance voltage plot of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a) as dep, (b) 500 °C, (c) 600 °C for a range of frequencies.

From fig (21) and (22) shows the conductance voltage characteristics of Pt/HfO₂/Si MOS capacitor for two sample (RF sputtered for 5 mins and RF sputtered for 10 mins to deposit HfO₂) for a wide range of frequencies.

8.3.Leakage current-conduction mechanism analysis:

In order to analyse the leakage current and conduction mechanism of the HfO₂ thin films, the annealing temperature dependence of the gate leakage current has been investigated systematically. Asymmetric leakage current density via gate voltage (J-V) curves in accumulation and inversion biases can be clearly observed in fig. 23

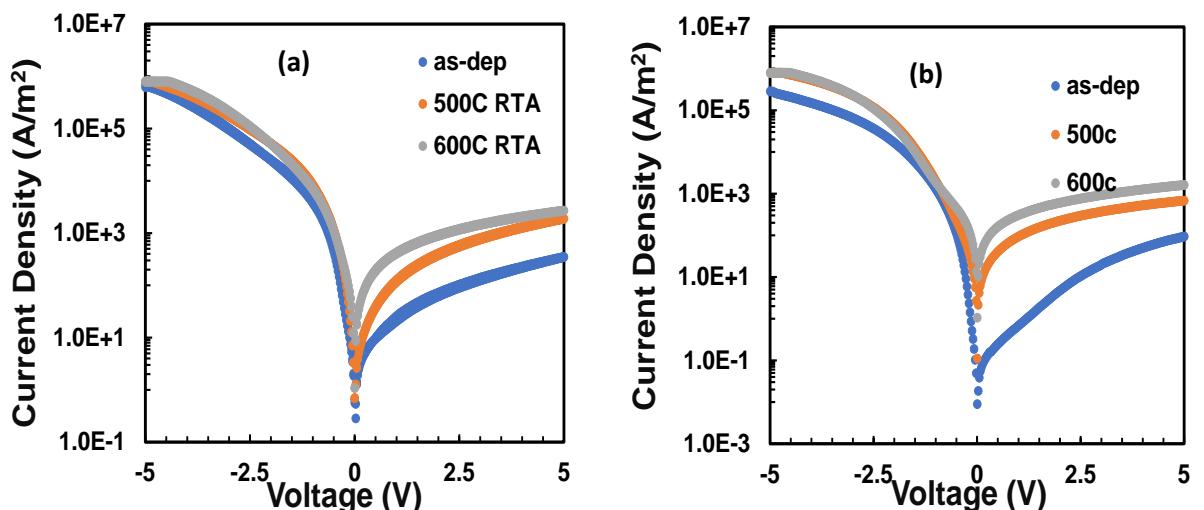


Fig 23: J-V characteristics of Pt/HfO₂/p-Si MOS capacitor sputtered for (a) 5 min and (b) 10 mins annealed at different temperatures (as dep, 500 °C, 600 °C).

In fig.23 the increase of leakage current density with annealing temperature may be caused by electron tunneling form Pt gate electrode to Si through defect and interface states [38].

It is well known that, in MOS structure, the current conduction mechanisms of hopping conduction mainly include direct tunneling (DT), Fowler-Nordheim (F-N) tunneling, Schottky emission (SE), Poole-Frenkel (P-F) emission, and space charge-limited conductions (SCLCs). Here, F-N tunneling and P-F emission through a gate oxide is represented in relation to MOS application with a negatively biased metal gate (gate

injection) as in case of these samples F-N and P-F has been found to be dominant in high and low applied field respectively.

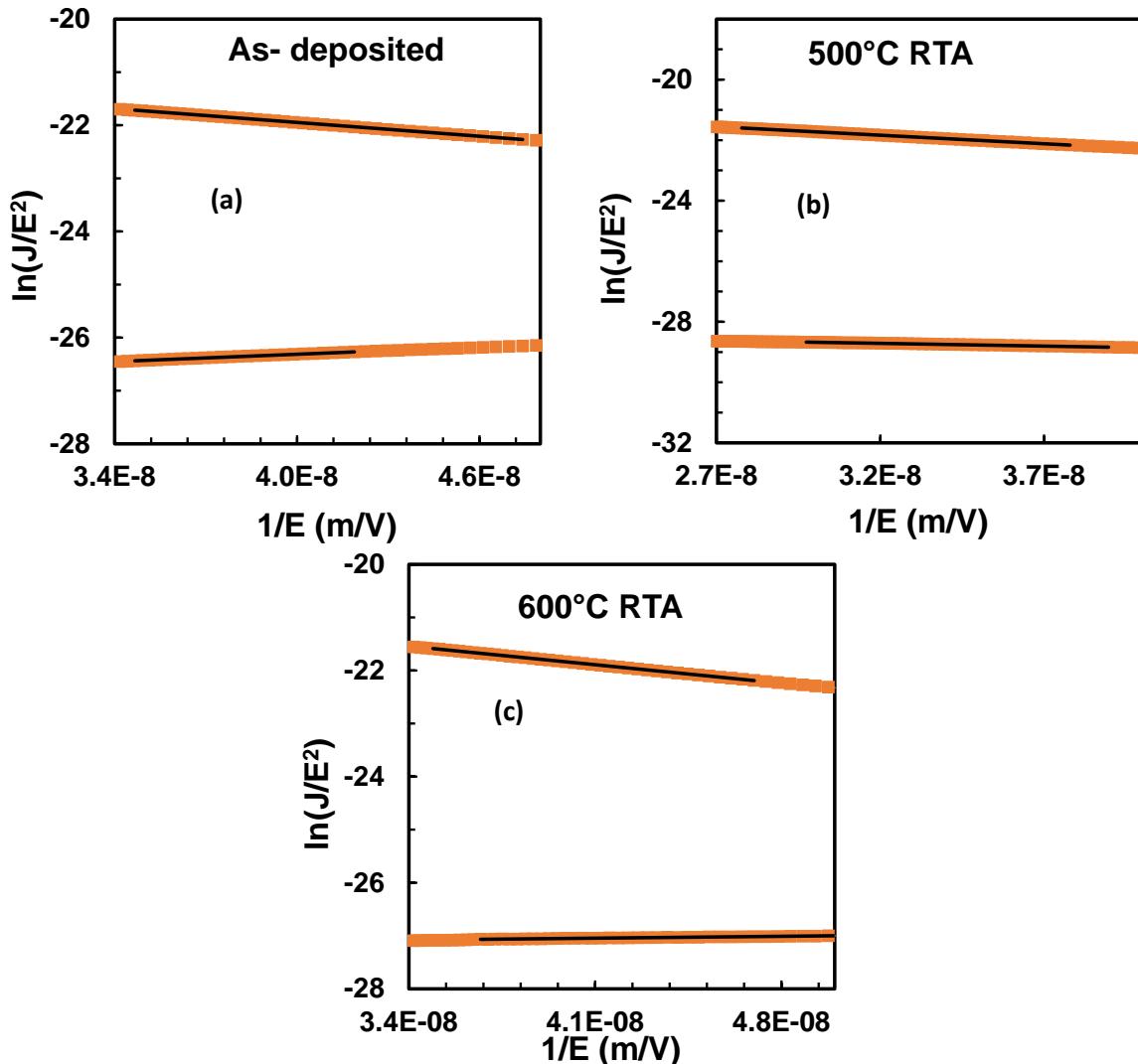


Fig 24: Fowler- Nordheim tunneling mechanism of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C.

In F-N conduction even though electron don't have enough energy to be used to tunnel through surface potential barrier, it can tunnel from the semiconductor conduction band into the oxide conduction band through a triangular barrier, governed by the well-known formula given by following [39]:

$$J = \frac{q^3 E^2 m_0}{8\pi h \phi_B m^*} \exp \left[\frac{-8\pi(2qm^*)^{\frac{1}{2}} \phi_B^{\frac{3}{2}}}{3hqE} \right] \quad (9)$$

Where, m^* is the tunneling electron effective mass ($m^* = m_{ox}$) in HfO_2 thin film, ϕ_B is the triangular barrier height and E , k , m_{ox} and h are the electric field in oxide the Boltzmann constant, the electron effective mass and the Planck's constant respectively. For a standard F-N tunneling, a plot of $\ln(J/E^2)$ versus $1/E$ should be linear, as shown in Fig. 24 & 26.

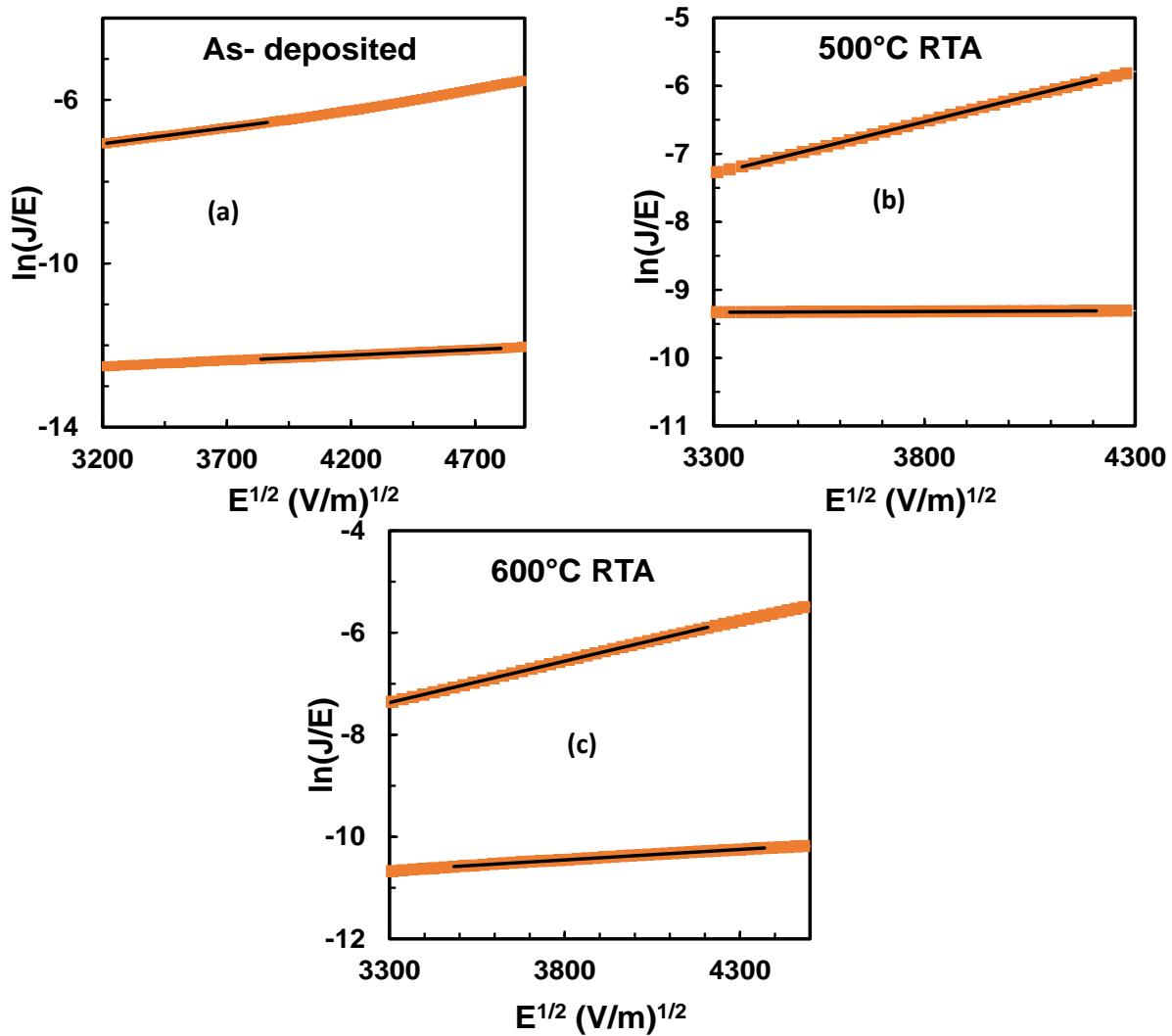


Fig 25: Pool-Frenkel emission mechanism of Pt/ HfO_2 /p-Si MOS capacitor sputtered for 5 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C.

The leakage current in oxide associated with P-F emission can be shown by utilizing the following equation [40]:

$$J \sim E \exp \left[\frac{-q(\phi_t - \sqrt{\frac{qE}{\pi \epsilon_i \epsilon_0}})}{kT} \right] \quad (10)$$

Where, ϕ_t is the trap energy barrier separating traps from conduction band, T, E, ε_0 , ε_i , k, and h are the absolute temperature, the electric field in oxide, the vacuum permittivity, the dynamic dielectric constant, the Boltzmann constant, and the Planck's constant respectively.

The plot of P-F coordinate of $\ln(J/E)$ versus $E^{1/2}$ at different annealing temperatures is sketched in Fig 25 & 27.

Table (6): φ_B and φ_t comparison for sample sputtered for 5 min

ANNEALING TEMPERATURE	FN		PF	
	φ_{Bn}	φ_{Bp}	φ_{tn}	φ_{tp}
As-dep	1.9	0.9	0.24	0.34
500C	1.4	0.9	0.32	0.24
600C	1.6	0.3	0.33	0.31

In table. 6 the values of triangular barrier height and trap energy barriers of Pt/HfO₂/p-Si MOS capacitor sputtered for 5 min are compared for both electrons and holes at different annealing temperature.

The triangular barrier height for electrons (φ_{Bn}) vary from 1.9-1.4 eV, whereas for holes (φ_{Bp}) it varies within 0.9-0.3eV.

On the other hand, the trap energy barrier (φ_{tn}) varies from 0.24-0.33 eV for electrons and for holes (φ_{tp}) it varies from 0.24-0.34 eV.

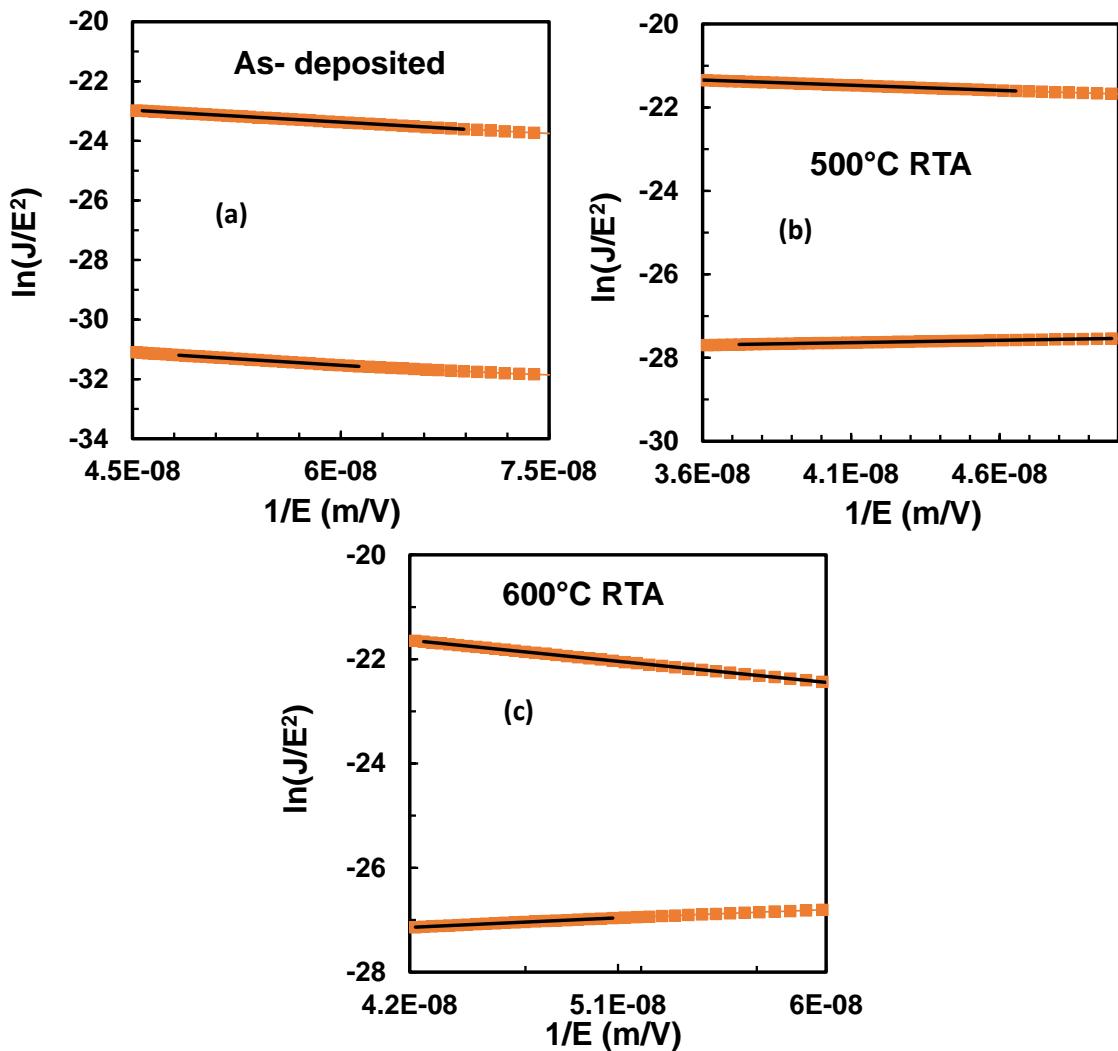


Fig 26: Fowler- Nordheim tunneling mechanism of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C.

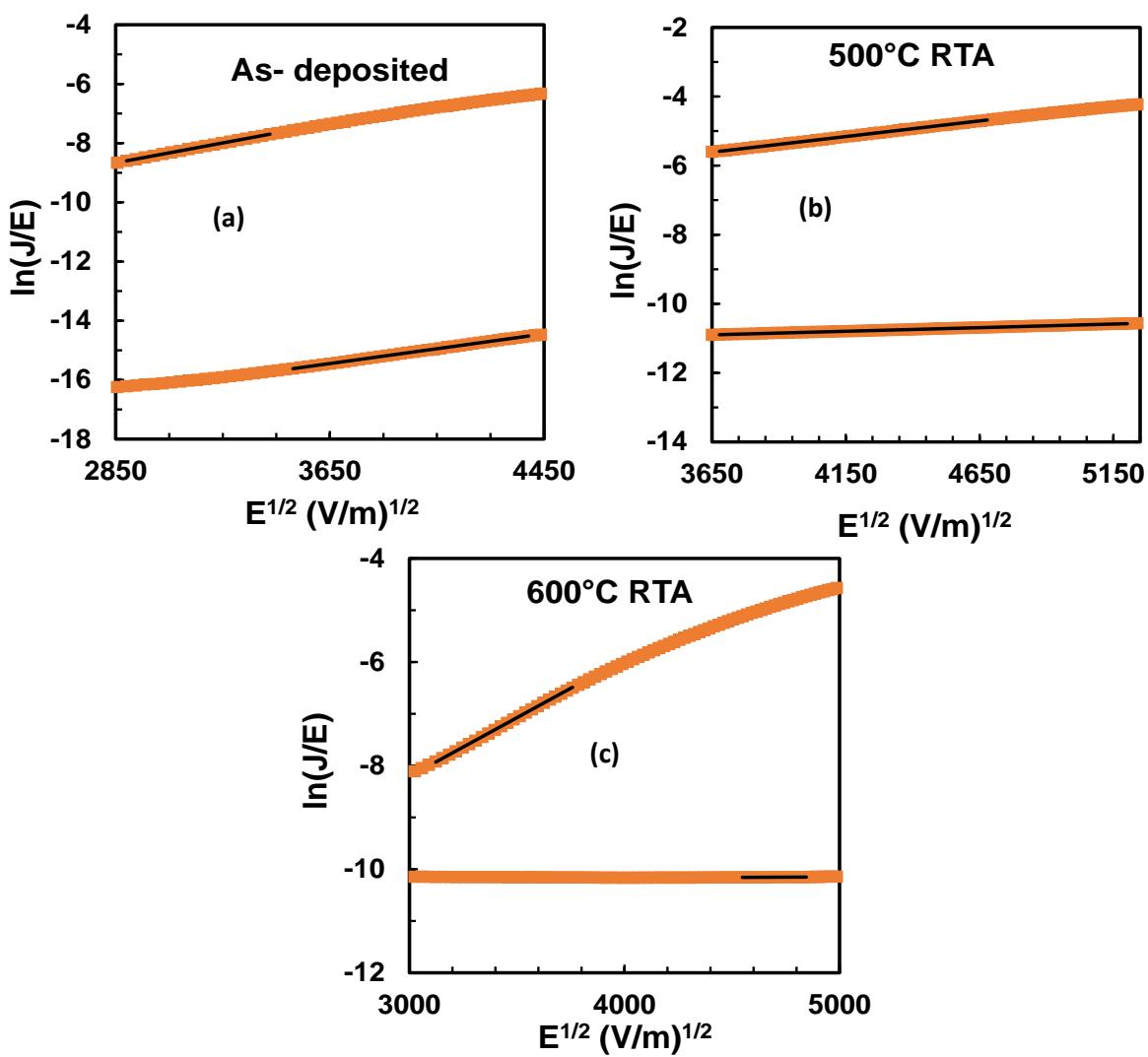


Fig 27: Pool- Frenkel emission mechanism of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min and annealed at different temperatures (a)as dep, (b)500 °C, (c)600 °C

Table (7): φ_B and φ_t comparison for sample sputtered for 10 min

ANNEALING TEMPERATURE	FN		PF	
	φ_{Bn}	φ_{Bp}	φ_{tn}	φ_{tp}
As-dep	1.2	1.2	0.39	0.264
500C	0.5	0.9	0.23	0.30
600C	1.4	0.9	0.39	0.264

In table. 7 the values of triangular barrier hight and trap energy barriers of Pt/HfO₂/p-Si MOS capacitor sputtered for 10 min are compared for both electrons and holes at different annealing temperature.

The triangular barrier hight for electrons (φ_{Bn}) vary from 0.5-1.4 eV, whereas for holes (φ_{Bp}) it varies within 0.9-1.2eV.

On the other hand, the trap energy barrier (φ_{tn}) varies from 0.23-0.39 eV for electrons and for holes (φ_{tp}) it varies from 0.264-0.30 eV.

9. CONCLUSION:

In conclusion, it was observed from ellipsometric analysis that the thickness of a Pt/HfO₂/p-Si MOS capacitor decreases with annealing temperature and increases with increased sputtering time. From the CV analysis it can be concluded that with increasing annealing temperature a positive flat band shift occurs in the CV characteristics. Also, the effective oxide charge density as well as the interface state density decreases. Decreased effective oxide charge density means fewer interface states hence, less probability of trapping charge carriers. High oxide charge density can shift the threshold voltage, leading to unpredictable device behaviour, and can increase the leakage current. So, reducing it leads to more stable operation over time. Interface states can also trap and release charge carriers, leading to instability in the device's electrical characteristics. So, lowering of the interface state density reduces this trapping, resulting in more stable device performance. The leakage current although should decrease with annealing temperature has not shown significant change possibly due to barrier height lowering but a more conclusive study needs to be done to investigate the exact reason. From the plot of tunneling mechanisms, it was observed that for a Pt/HfO₂/p-Si MOS capacitor sputtered for different time F-N tunneling is dominant in high applied field whereas P-F tunneling is dominant for low applied field.

10. REFERENCE

1. https://en.wikipedia.org/wiki/Moore%27s_law
2. Ratnesh, Ratneshwar K., A. Goel, G. Kaushik, H. Garg, M. Singh, and B. Prasad. "Advancement and challenges in MOSFET scaling." *Materials Science in Semiconductor Processing* 134 (2021): 106002.
3. Wong, Stephen, and C. Andre T. Salama. "Impact of scaling on MOS analog performance." *IEEE Journal of Solid-State Circuits* 18, no. 1 (1983): 106-114.,
4. Chopra, Shivani, and Subha Subramaniam. "A review on challenges for MOSFET scaling." *Int. J. Innovative Science* 2, no. 4 (2015).
5. Kumar, Manish. "Effects of Scaling on MOS DevicePerformance." *IOSR J. VLSI Signal Process.(IOSR-JVSP)*, e-ISSN 2319–4200, p-ISSN No. 2319–4197www.iosrjournals.org 5 (2015): 25-28.
6. Advancement and challenges in MOSFET scaling R.K. Ratnesh
7. Sze, Simon M., Yiming Li, and Kwok K. Ng. *Physics of semiconductor devices*. John wiley & sons, 2021.
8. Maity, Niladri Pratap, Reshma Maity, R. K. Thapa, and Srimanta Baishya. "A tunneling current density model for ultra thin HfO₂ high-k dielectric material based MOS devices." *Superlattices and Microstructures* 95 (2016): 24-32.
9. The Progress and Challenges of Applying High-k/Metal-Gated Devices to Advanced CMOS Technologies Hsing-Huang Tseng, Ph.D. *Professor of Electrical Engineering Ingram School of Engineering Texas State University 601 University Drive, San Marcos, TX 78666, USA*
10. A Review on Dielectric Breakdown in Thin Dielectrics: Silicon Dioxide, High-*k*, and Layered Dielectrics *Felix Palumbo, * Chao Wen, Salvatore Lombardo, Sebastian Pazos, Fernando Aguirre, Moshe Eizenberg, Fei Hui, and Mario Lanza**
11. Ginez, Olivier, J-M. Portal, and Ch Muller. "Design and test challenges in resistive switching RAM (ReRAM): An electrical model for defect injections." In *2009 14th IEEE European Test Symposium*, pp. 61-66. IEEE, 2009.
12. Zhang, J. W., G. He, H. S. Chen, J. Gao, X. F. Chen, P. Jin, D. Q. Xiao, R. Ma, M. Liu, and Z. Q. Sun. "Modulation of charge trapping and current-conduction mechanism of TiO₂-doped HfO₂ gate dielectrics based MOS capacitors by annealing temperature." *Journal of Alloys and Compounds* 647 (2015): 1054-1060.

13. M. Housa, High k gate dielectric, IPO, Bristal (2004) Chapter 1
14. L. Pereira, A. Marques, H. Aguas, N Netev, S. Georgiev, E. Fortunato, R. Martins, Mat. Sci. & Engg. B 109, 89 (2004)
15. B. Sen, C.K. Sarkar, H. Wong, M. Chan, C.W. Kok, Solid State Elect. 50, 237 (2006)
16. B.H. Lee, L. Kang, J.C. Lee, Appl. Phys. Lett. 76, 1926 (2000)
17. Effect of postdeposition annealing on the thermal stabilityand structural characteristics of sputtered HfO₂ filmson Si (100)G.He
18. Influence of annealing condition on the properties of sputteredhafnium oxideSeok-Woo Nam a,b, Jung-Ho Yoo a, Suheun Nam
19. Study of the effect of thermal annealing on high k hafnium oxidethin film structure and electrical properties of MOS and MIMdevicesA. Srivastava • R. K. Nahar • C. K. Sarkar
20. Interface and electrical properties of ultra-thin HfO₂ film grown by radio frequency sputtering Madhuchhanda Nath, Asim Roy n
21. Banani Sen, C.K. Sarkar, Hei Wong, M. Chan, C.W. Kok, Electrical characteristics of high- κ dielectric film grown by direct sputtering method, Solid-State Electron. 50(2006)237–240.
22. 2011 SPRINGER BOOK
Pananakakis, G., G. Ghibaudo, R. Kies, and C. Papadas. "Temperature dependence of the Fowler–Nordheim current in metal-oxide-degenerate semiconductor structures." *Journal of Applied Physics* 78, no. 4 (1995): 2635-2641.
24. C Chang, Chi. *TUNNELING IN THIN GATE OXIDE MOS STRUCTURES (SILICON IMPACT IONIZATION, VALENCE-BAND, ELECTRON)*. University of California, Berkeley, 1984.
25. Depas, Michel, Bert Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, and M. M. Heyns. "Determination of tunnelling parameters in ultra-thin oxide layer poly-Si/SiO₂/Si structures." *Solid-state electronics* 38, no. 8 (1995): 1465-1471.
26. Maserjian, J., and N. Zamani. "Behavior of the Si/SiO₂ interface observed by Fowler-N tunneling." *Journal of Applied Physics* 53, no. 1 (1982): 559-567.
27. Weinberg, Z. A. "On tunneling in metal-oxide-silicon structures." *Journal of Applied Physics* 53, no. 7 (1982): 5052-5056.
- Zafar, S., Q. Liu, and E. A. Irene. "Study of tunneling current oscillation dependence

28. on SiO₂ thickness and Si roughness at the Si/SiO₂ interface." *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 13, no. 1 (1995): 47-53.
29. Bentarzi, Hamid. *Transport in metal-oxide-semiconductor structures: mobile ions effects on the oxide properties*. Springer Science & Business Media, 2011.
30. Scarpa, A., A. Paccagnella, G. Ghidini, A. Vianello, and E. Zanoni. "Instability of post-Fowler-Nordheim stress measurements of MOS devices." *Solid-State Electronics* 41, no. 7 (1997): 935-938.
31. Maserjian, J. "Tunneling in thin MOS structures." *Journal of Vacuum Science and Technology* 11, no. 6 (1974): 996-1003.
32. Lenzlinger, M., and E. H. Snow. "Fowler-Nordheim tunneling into thermally grown SiO₂." *Journal of Applied physics* 40, no. 1 (1969): 278-283.
33. S.J. Ding, D.W. Zhang, L.K. Wang, J. Phys. D. Appl. Phys. 40 (2007) 1072e1076.
34. Chemical structure and electrical properties of sputtered HfO₂ films on Si substrates annealed by rapid thermal annealing Tingting Tan*, Zhengtang Liu, Hongcheng Lu, Wenting Liu, Feng Yan
35. Effect of post-deposition annealing temperature on RF-sputtered HfO₂ thin film for advanced CMOS technology A.G. Khairnar, A.M. Mahajan*
36. Electrical Properties of Radio-Frequency Sputtered HfO₂ Thin Films for Advanced CMOS Technology Pranab Kumar Sarkar and Asim Roy*
37. A.C. Rastogi, S.B. Desu, J. Electroceram. 13 (2004) 122e127.
38. T. Yu, C.G. Jin, Y.J. Dong, D. Cao, L.J. Zhuge, X.M. Wu, Mat. Sci. Semicon. Proc. 16 (2013) 1321e1327
39. K.Y. Cheong, J.H. Moon, H.J. Kim, W. Bahng, N.K. Kim, J. Appl. Phys. 103 (2008) 084113-1e084113-8.
40. Hori, Takashi. "Gate dielectrics and MOS ULSIs, volume 34 of Springer series in electronics and photonics, chapter 4." (1997): 149-156.

