15ECE386 VLSI DESIGN LAB

7. Positive Edged Triggered D flip-flop

Date:

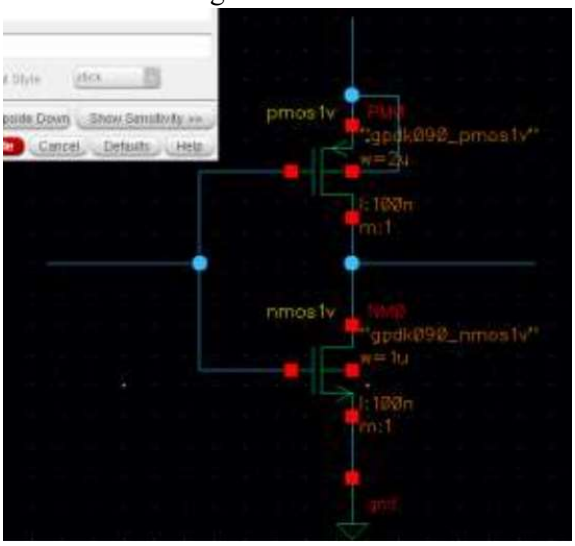
Objectives:

- Creating the Symbols for NOT and NAND Gates
- Implementation of D-Latch
- Creating the symbol
- Implementation of Master Slave D-Flip Flop
- Testing the Boolean Function

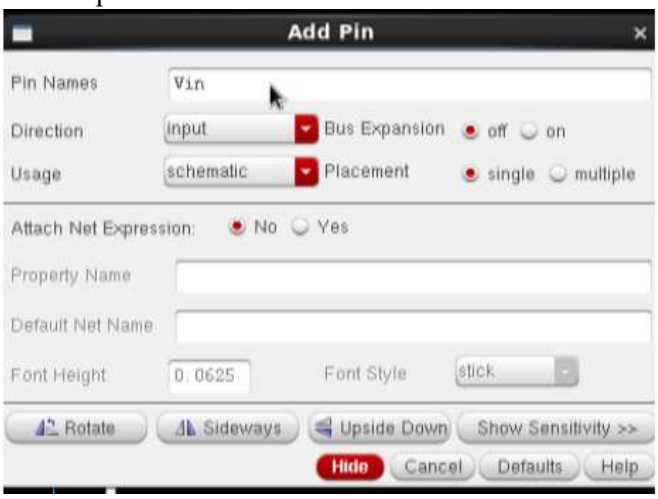
Steps:

- **Creating the Symbol for NOT and NAND logic.**
  Draw the CMOS NOT gate in *virtuoso schematic editor* window. Set the width of NMOS and PMOS devices as 1µm and 2µm respectively to make the pull up and pull down strength same.

  Step 1: Draw the inverter as shown in figure.

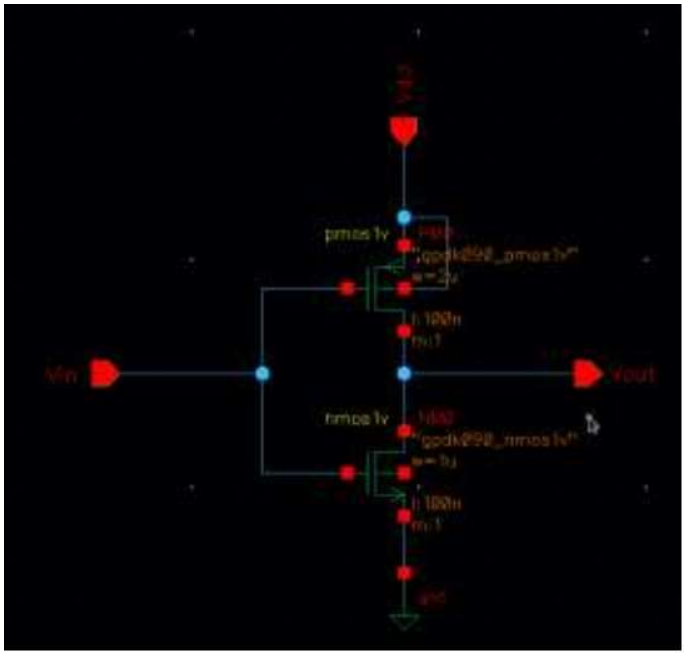


  Step 2: Creating pin
  Select the second last option available in the toolbar. It pops up a window as shown below. To set the input pin give pin name as VIN and direction as INPUT as shown in figure and select hide. After this, place the pin at the input line.



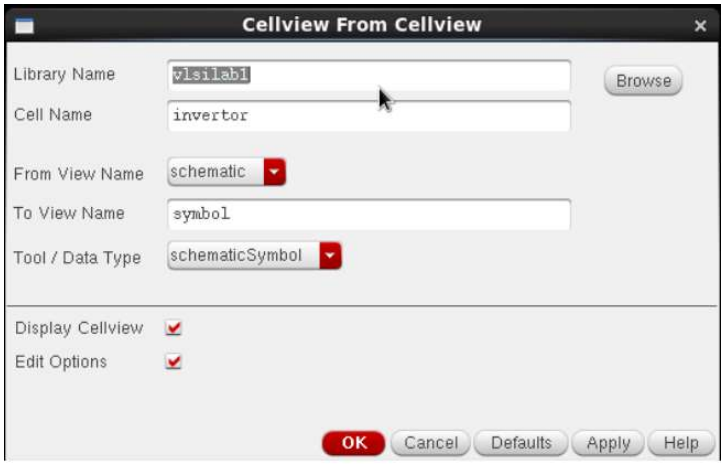
  Similarly add pins for output line and Vdd line.

After adding pins the circuit will look like as shown below

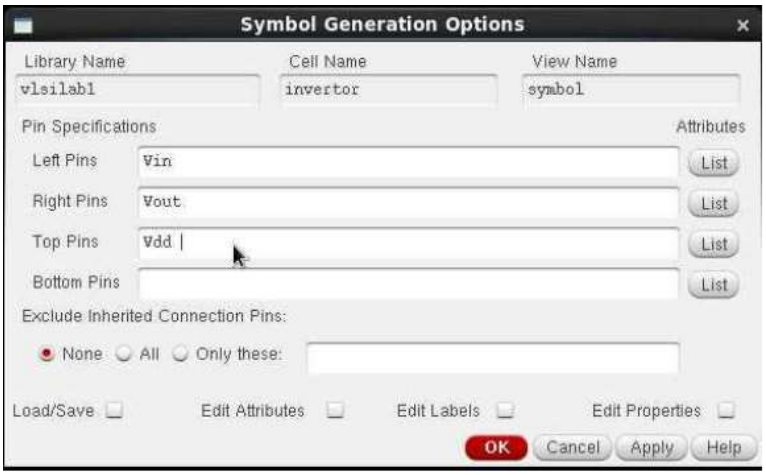


Step 3: Creating the symbol

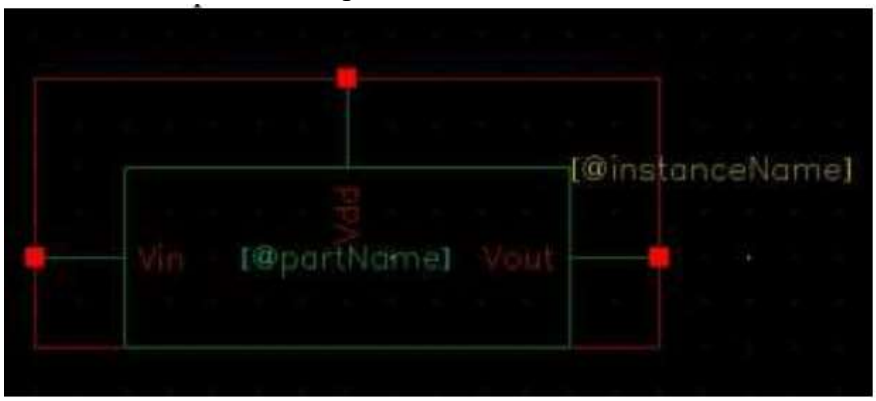
a) Create→Cellview→From cellview. Then the below window pops up. Select your library and provide an appropriate cellview name(Inverter). Then click OK.



b) New window as shown below will appear. Specify the pin positions as shown below. Then click OK.



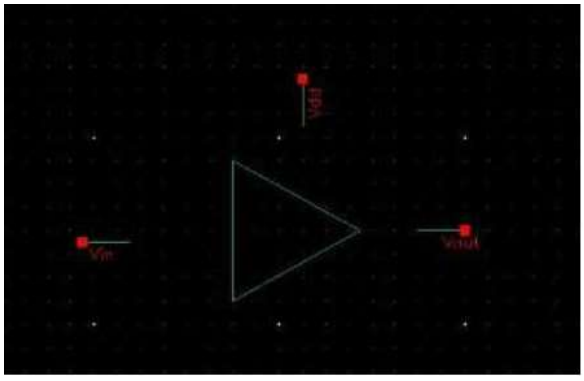
c) The below shown schematic is opened.



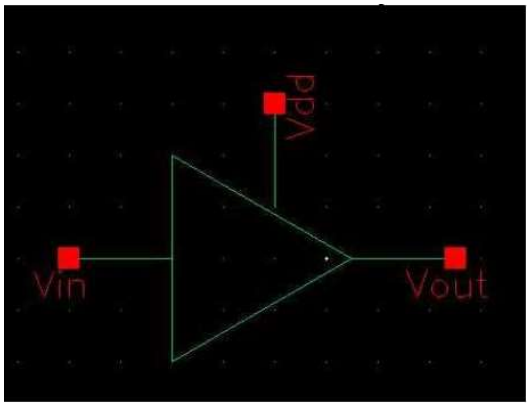
d) Delete the red and green boxes. Also, remove instance name and part name.

e) Draw the inverter symbol following the steps below and arrange the pin positions.

From symbol window toolbar, select create line (3rd from right). Draw a triangle by clicking at three places anywhere in the window as shown below.



Select and move the pins to the desired location and make the symbol as shown below.



Then **Check and Save** the symbol

Similarly follow the above steps to create the symbol for **NAND gate**. While drawing the circuit don't forget to **size the transistors properly**.ie maintaining the **2:1 ratio**.

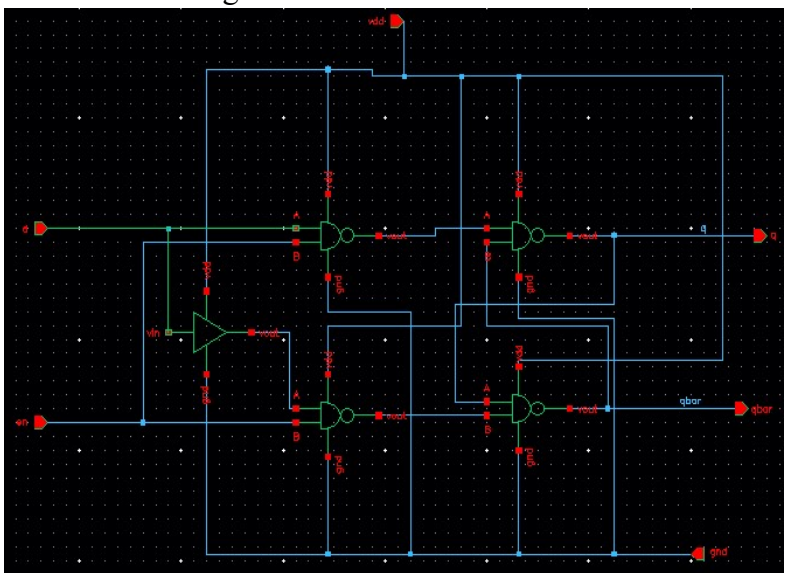
f) **Using the symbol**

- Create a new cellview.
- Go to Create instance→Select the library name which contains inverter symbol(vlsilab1)→

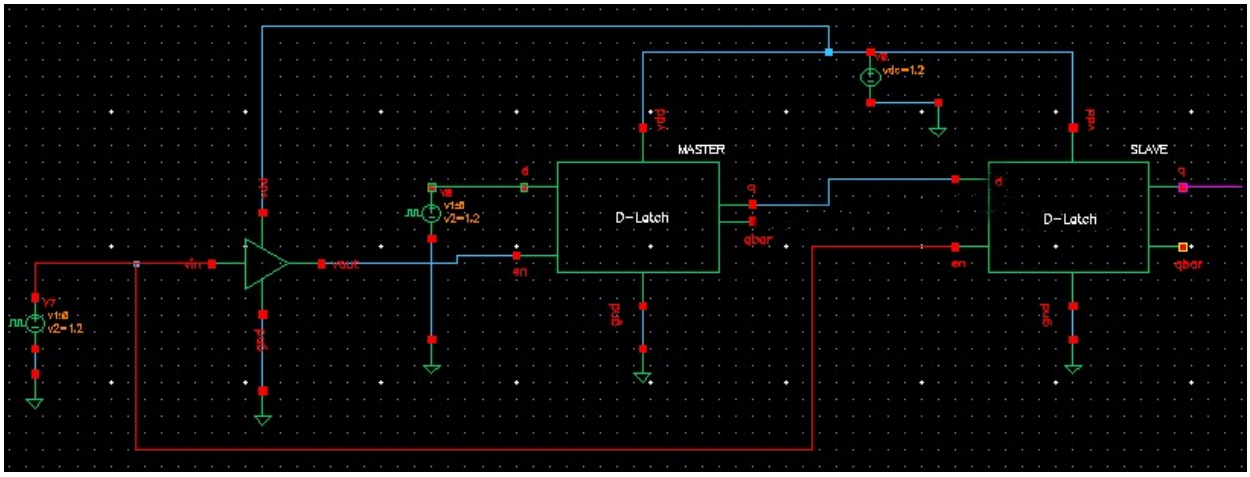
Select the cell inverter→symbol→close→hide and place the symbol on the schematic window.

- To view and edit the schematic, Select the inverter symbol→go to edit→Hierarchy→Descend Edit (Shift+E). The below window will pop up. Then click OK. Now the schematic will be displayed.

- To go back to the symbol, edit→Hierarchy→Return to top(ctrl+E).
- Connect input as vpulse and Vdd as Vdc to the NOT and NAND symbol, Draw the circuit for the D-latch as shown in figure below.



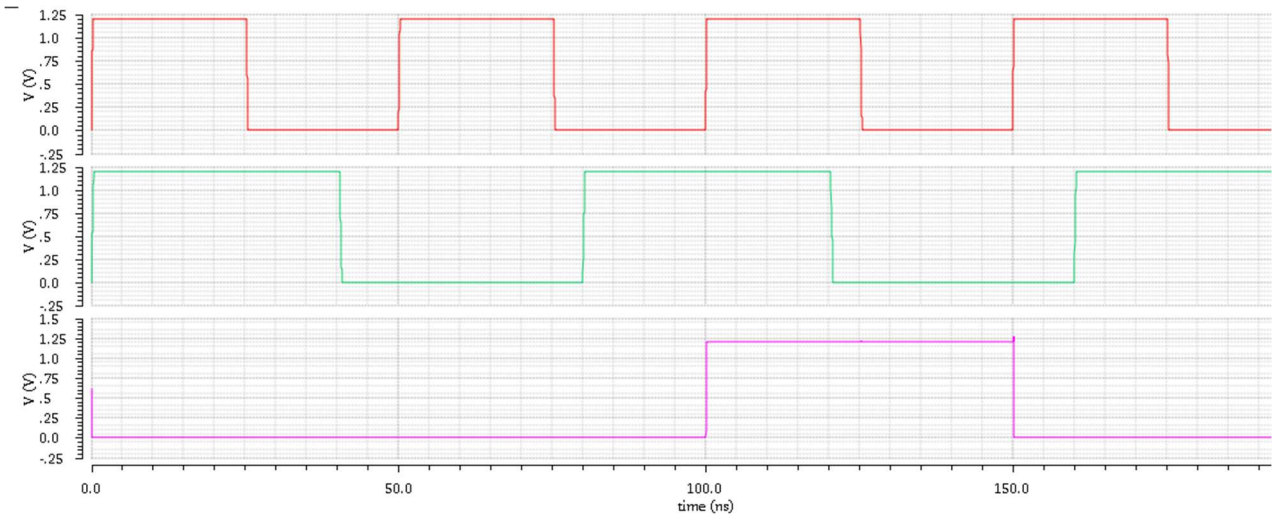
- Now follow the above steps to create a symbol of the D-latch.
- After creating the symbol, take a new Cellview and draw the circuit for the positive edged triggered Master Slave D-flip flop as shown below.



MASTER-SLAVE D-FLIP FLOP

- Take the clock pulse period to be 50ns and pulse width as 25ns with V0 = 1.2v and V1 = 0. Similarly the D in pulse period be 80ns and pulse width as 40ns and same voltages.
- Then **check and Save**
- After that go to files → **ALE** and then from **ALE** window perform **Analysis** and choose **Transient analysis**. Take period to be 200ns, Click OK.
- After that go to **Outputs → to be plotted →** select from Schematic. Select D, clk and Q nets. Click on the play button to RUN the analysis.

We will get a graph something similar to given below.



MASTER-SLAVE D-FLIPFLOP TIMING DIAGRAM

Signature: