

COL 216 ASSIGNMENT 2

PART 4

SATWIK

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2022CS51150

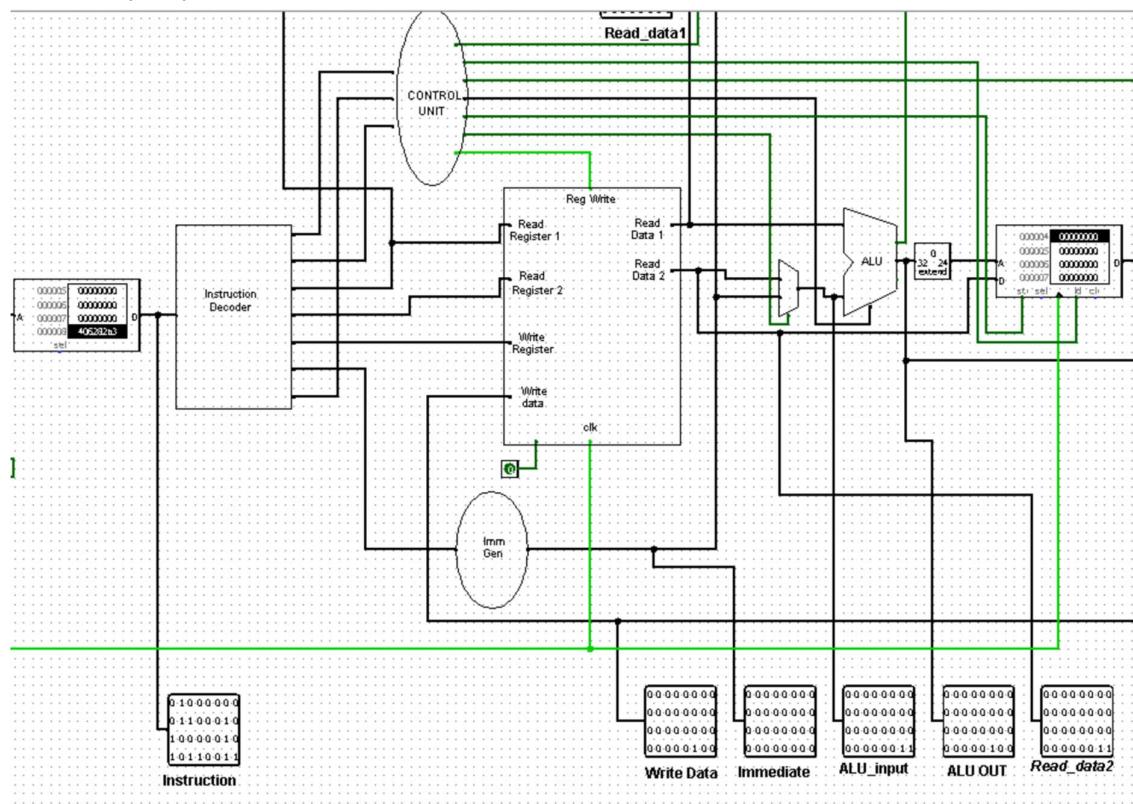
2022CS11104

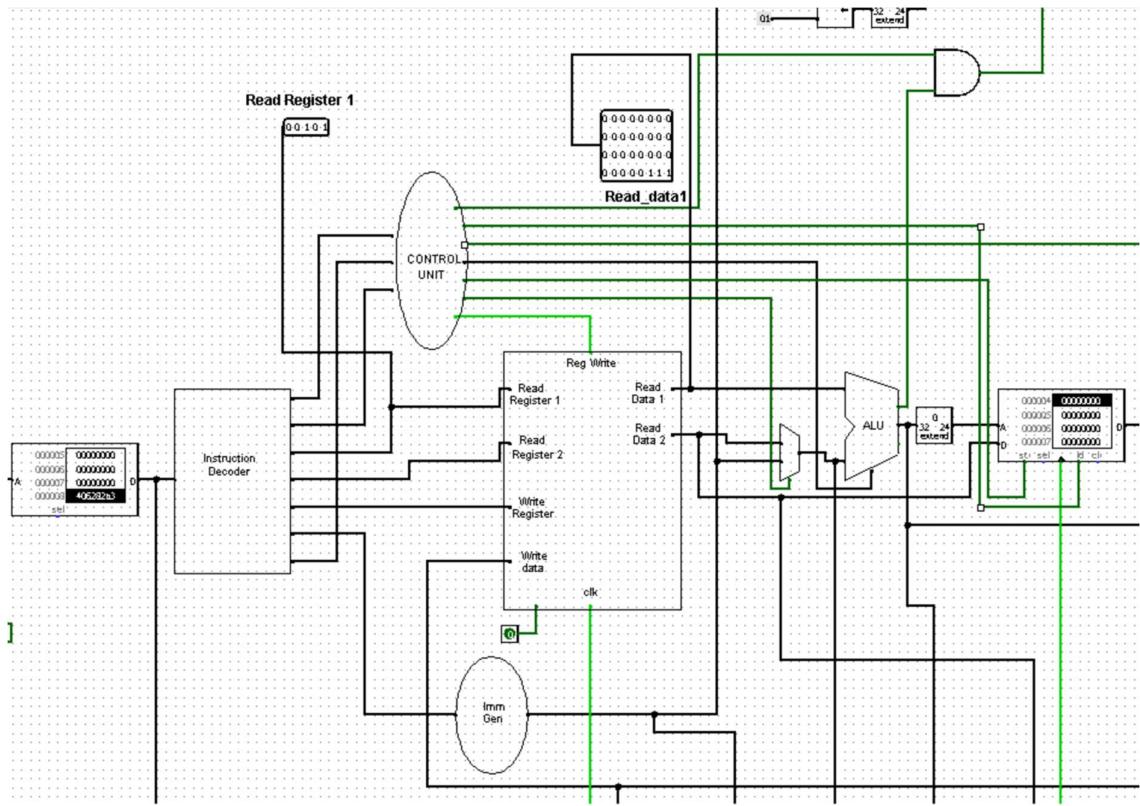
1. SUB

addi x5,x5,7

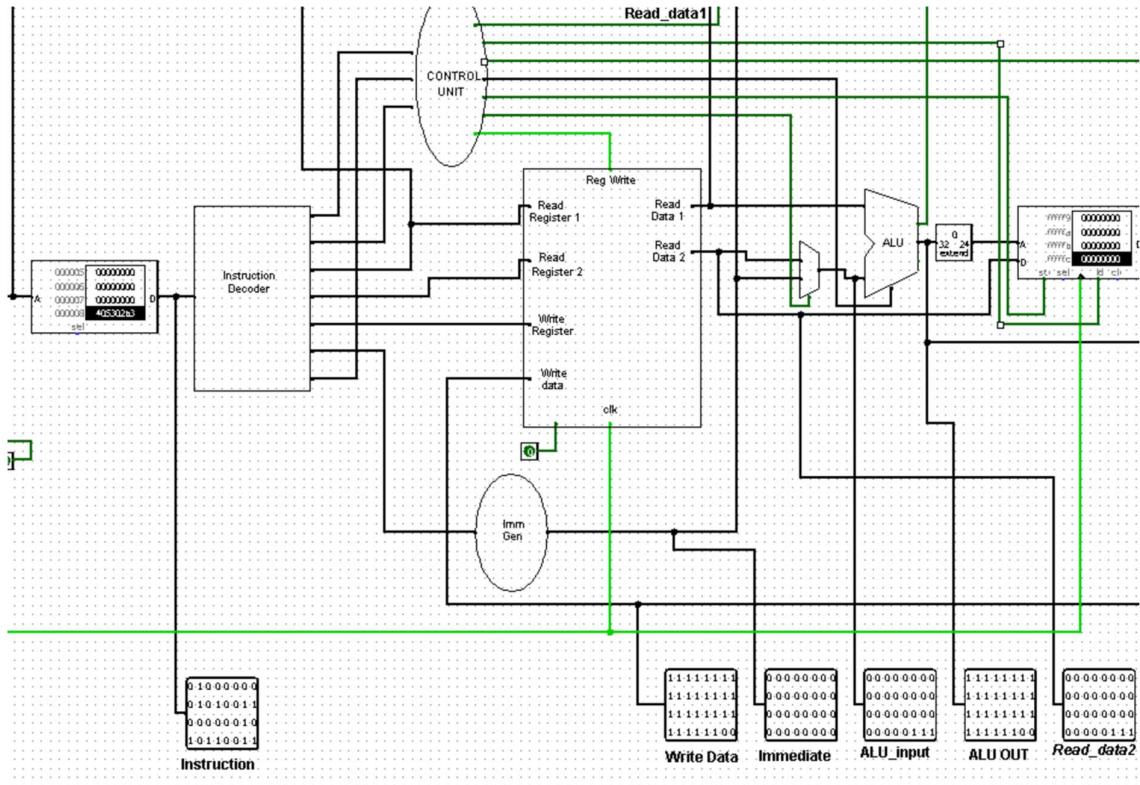
addi x6,x6,4

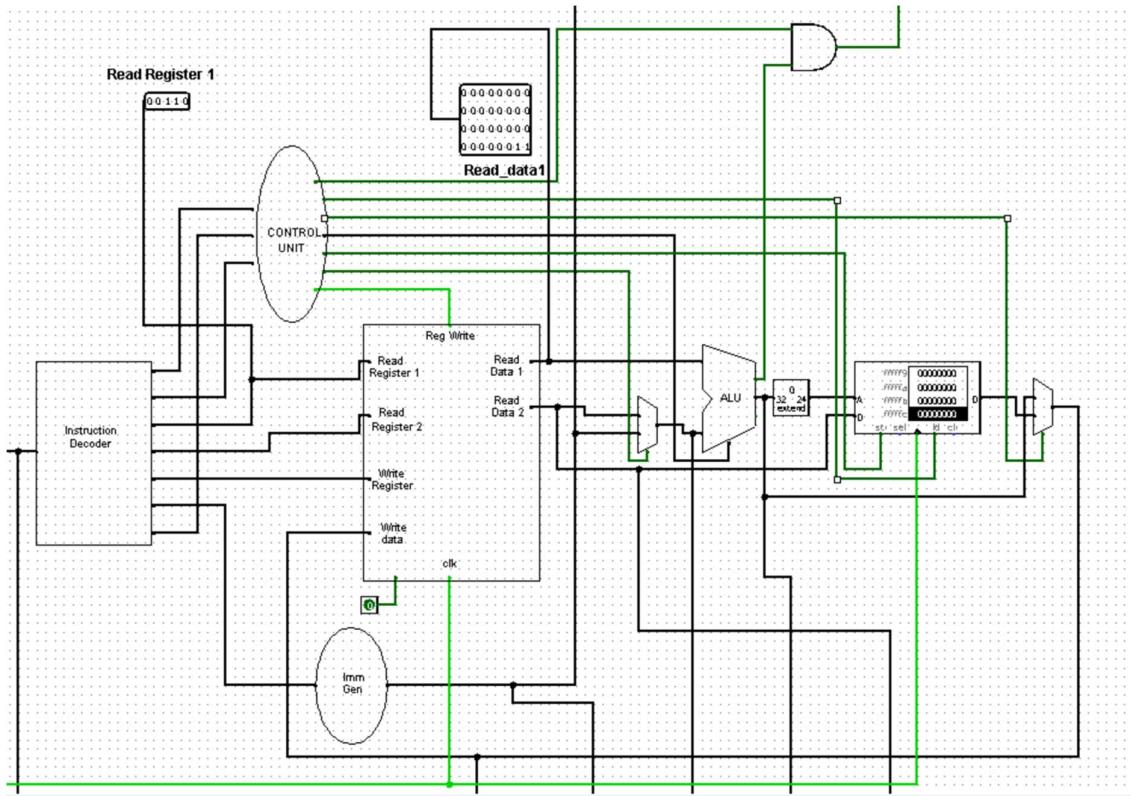
sub x5,x5,x6





In this case the instruction `sub x5,x6,x5` is executed



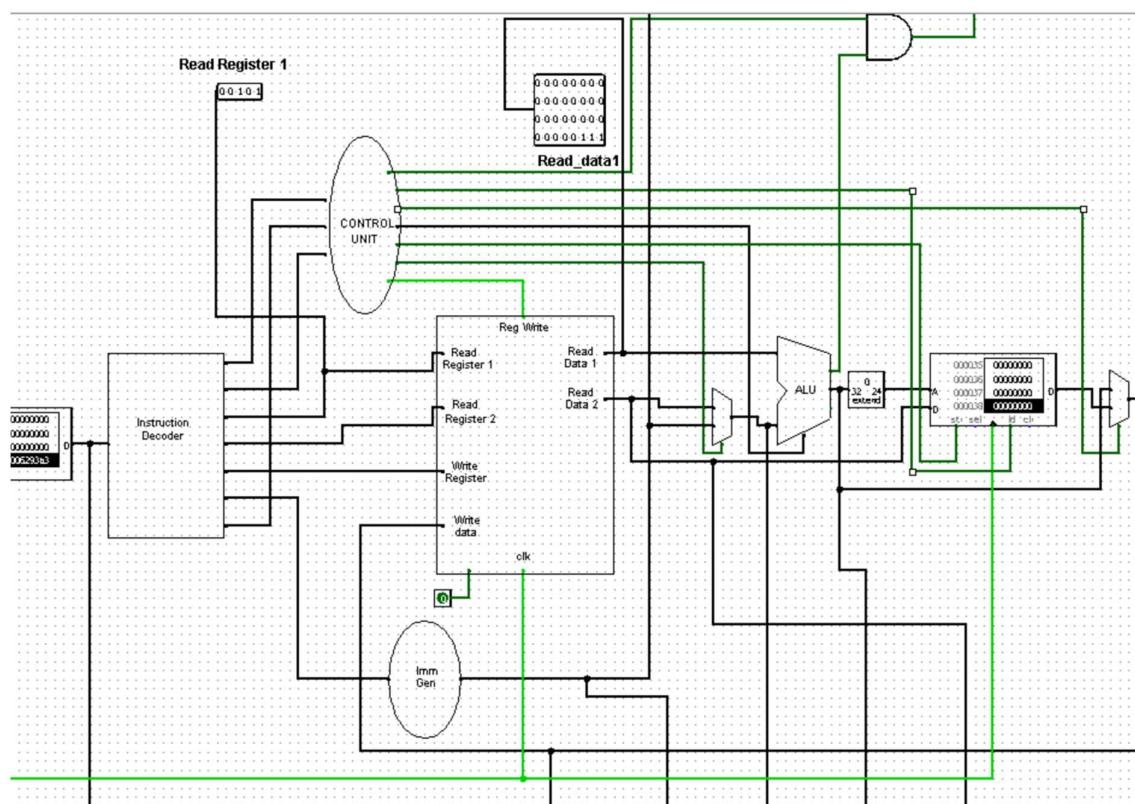
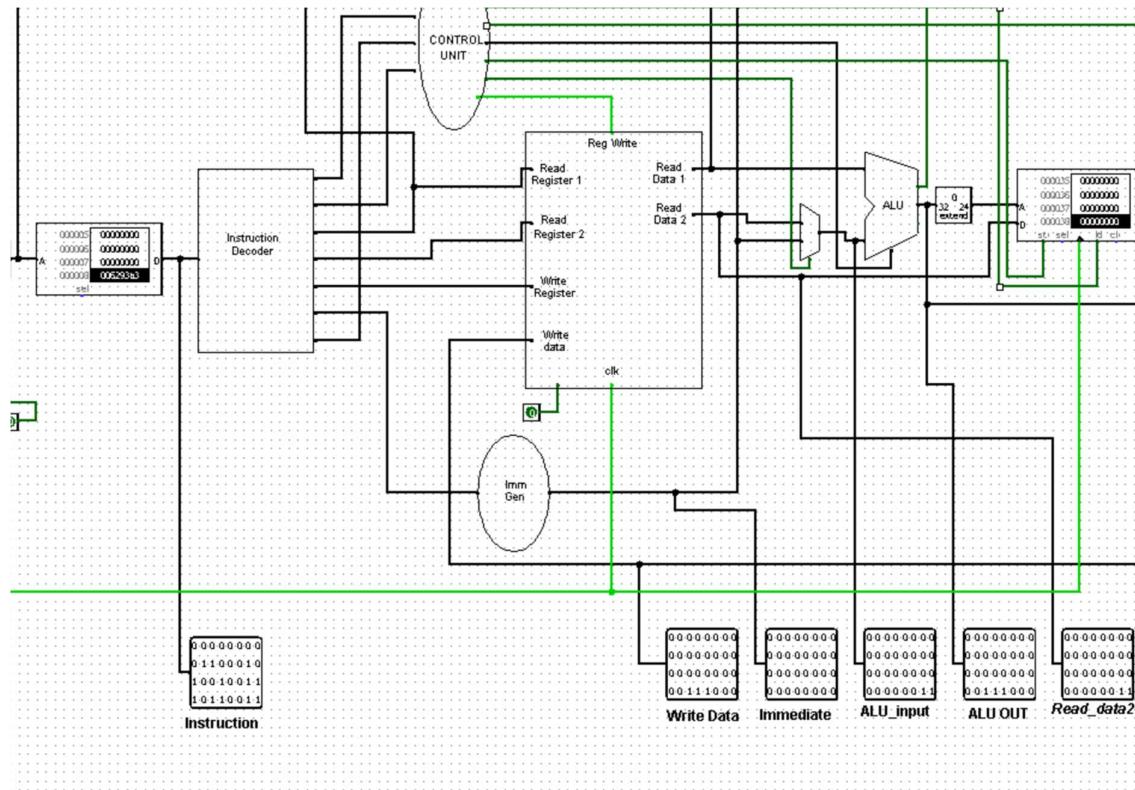


2. SLL

addi x5,x5,7

addi x6,x6,3

sll x7,x5,x6

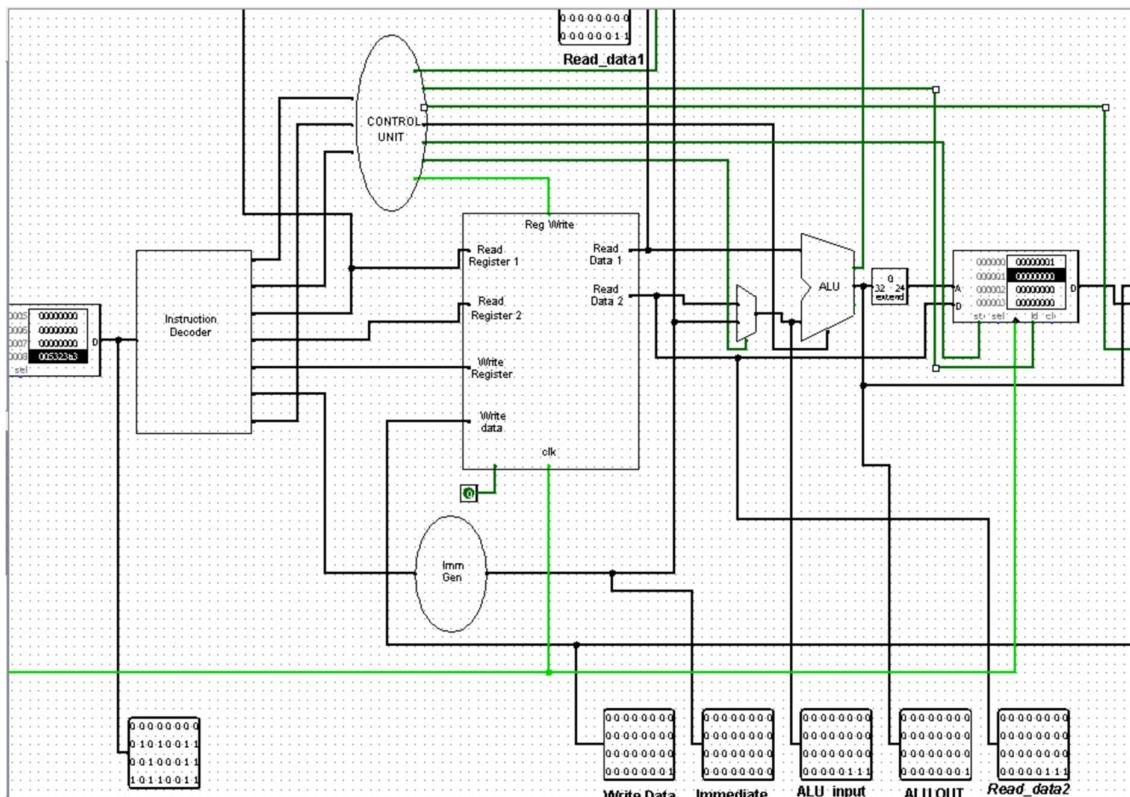


3. SLT

addi x5,x5,7

addi x6,x6,3

slt x7,x6,x5

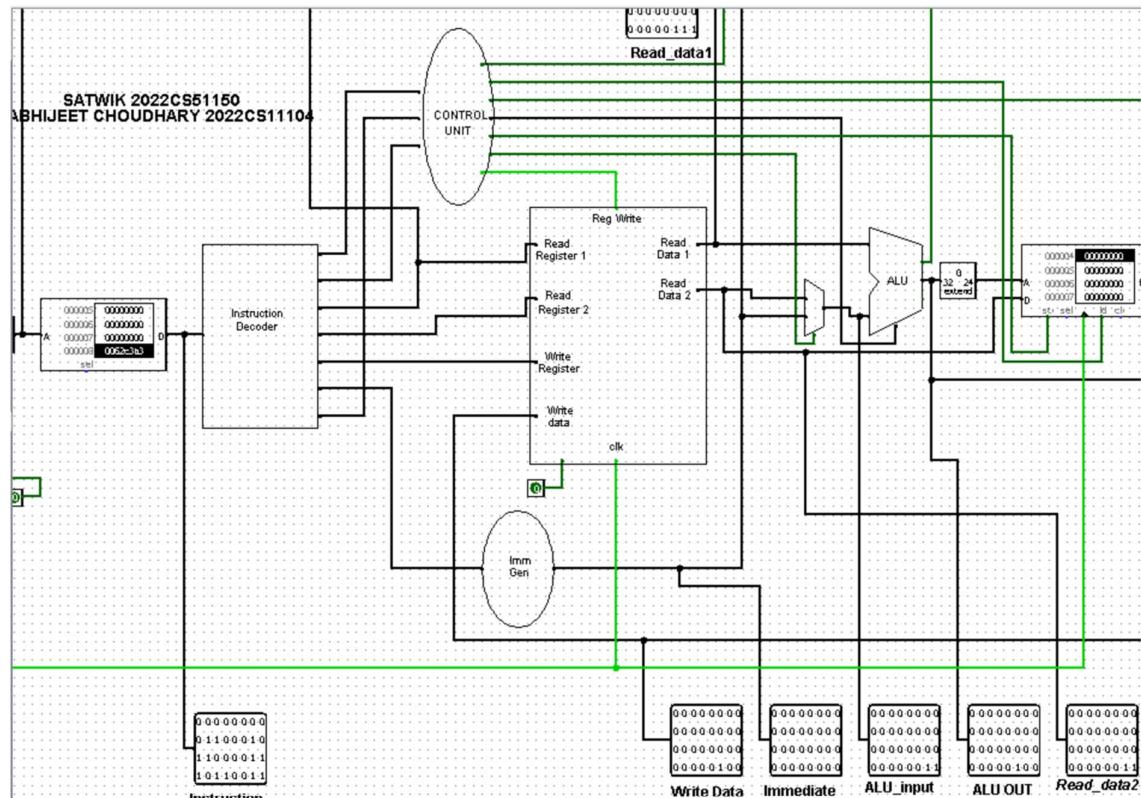


4. XOR

addi x5,x5,7

addi x6,x6,3

xor x7,x5,x6

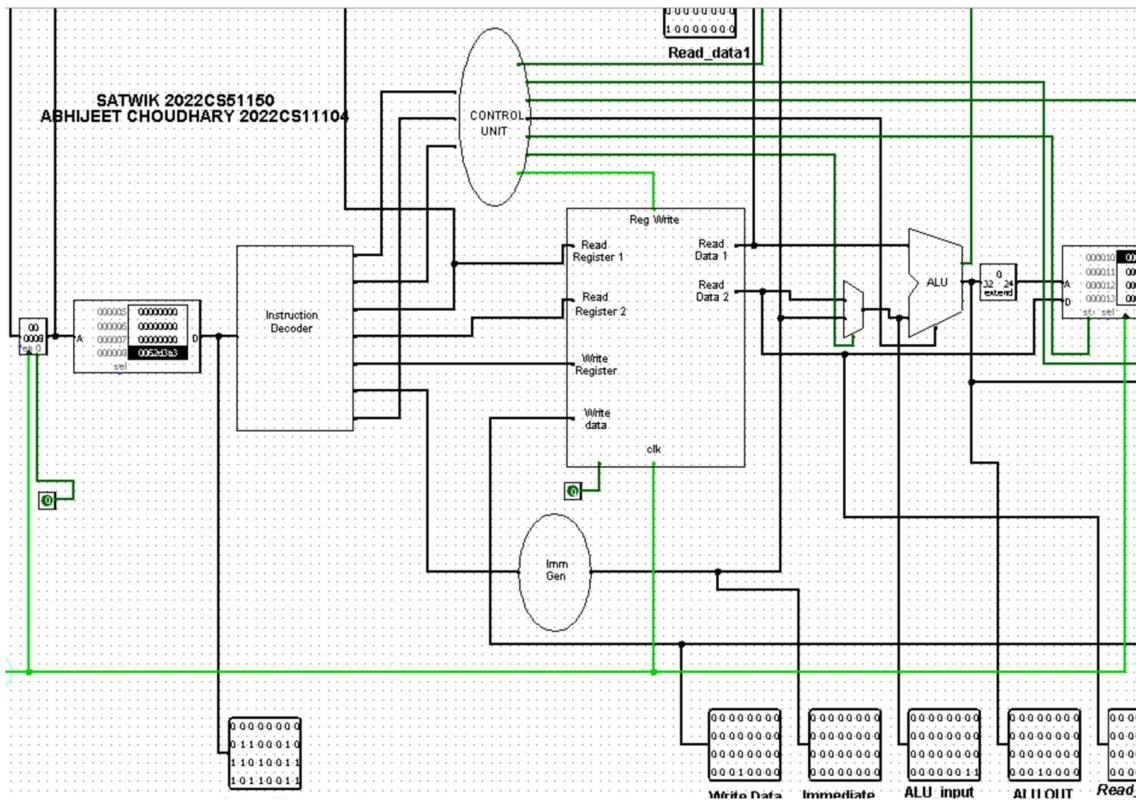


6. SRL

`addi x5,x5,128`

`addi x6,x6,3`

`srl x7,x5,x6`

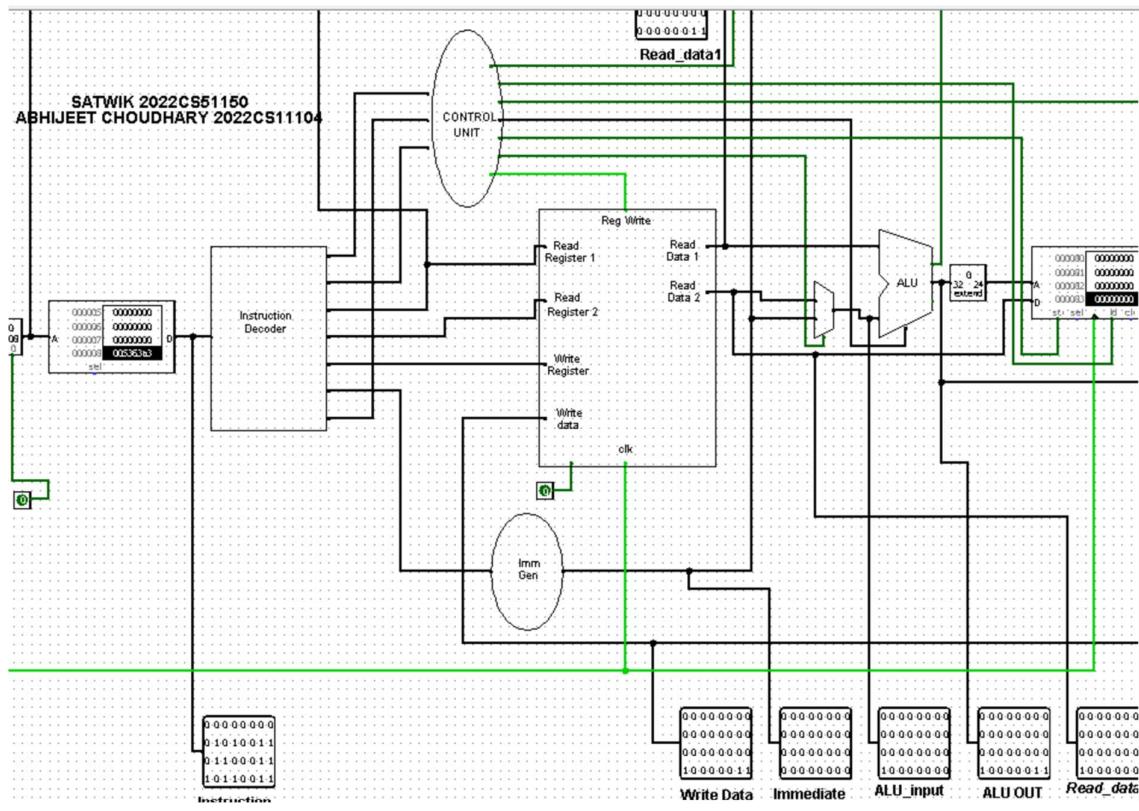


7. OR

addi x5,x5,128

addi x6,x6,3

or x7,x6,x5

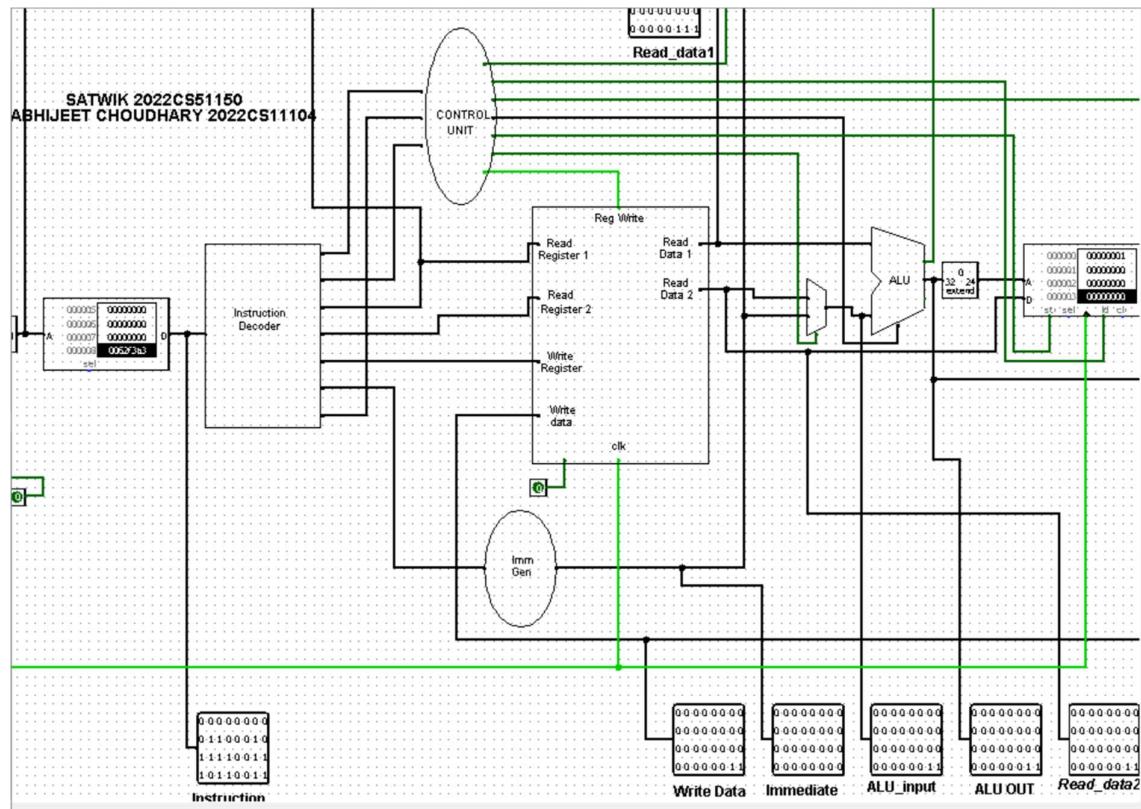


8. AND

`addi x5,x5,7`

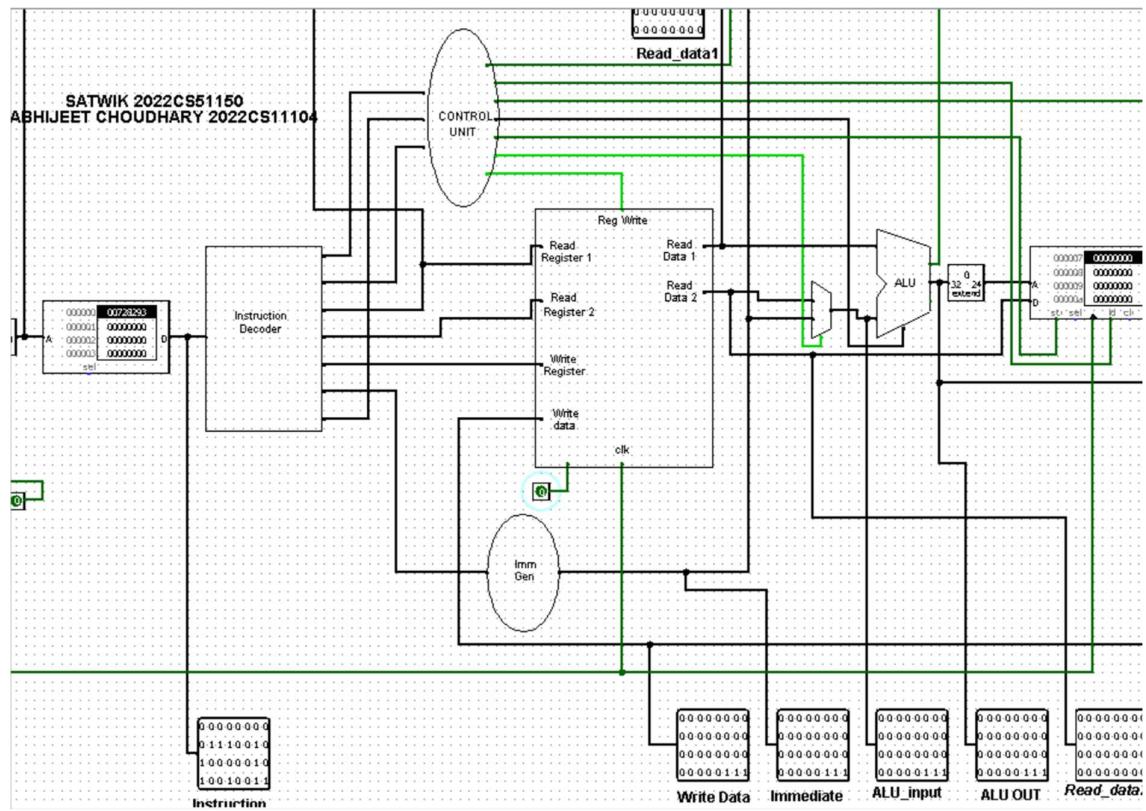
`addi x6,x6,3`

`and x7,x5,x6`



9. ADDI

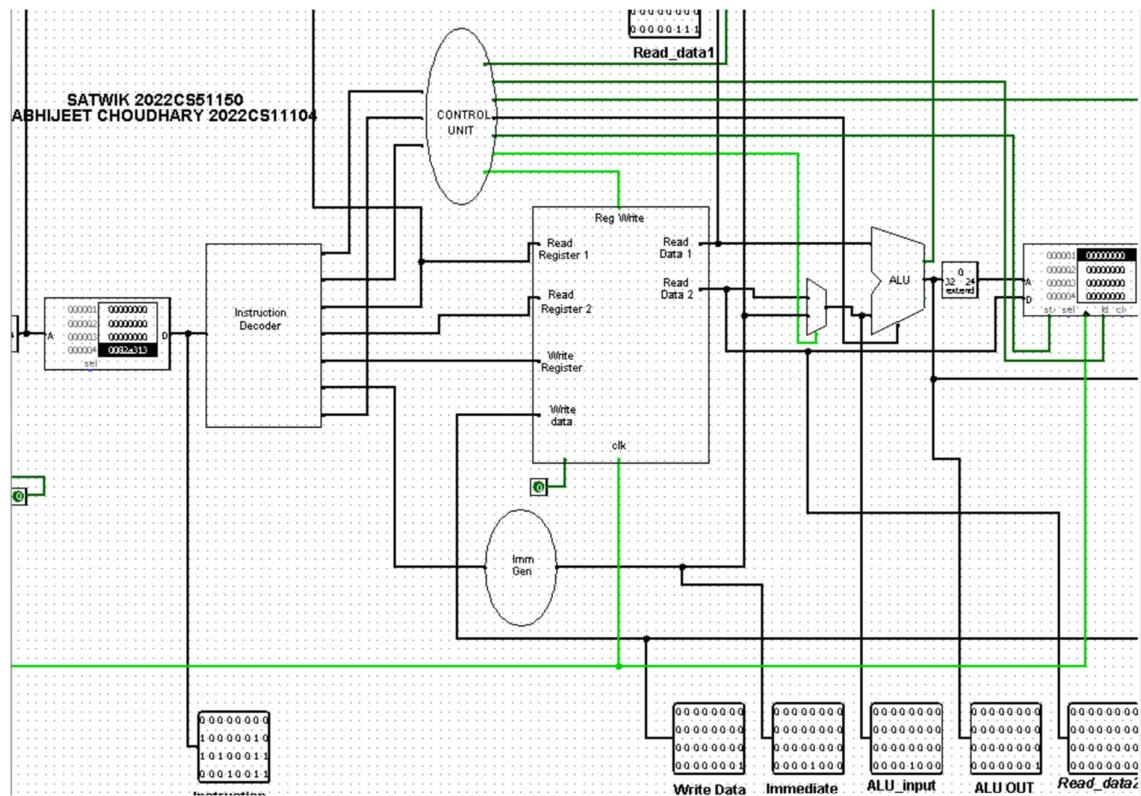
addi x5,x5,7



10. SLTI

`addi x5,x5,7`

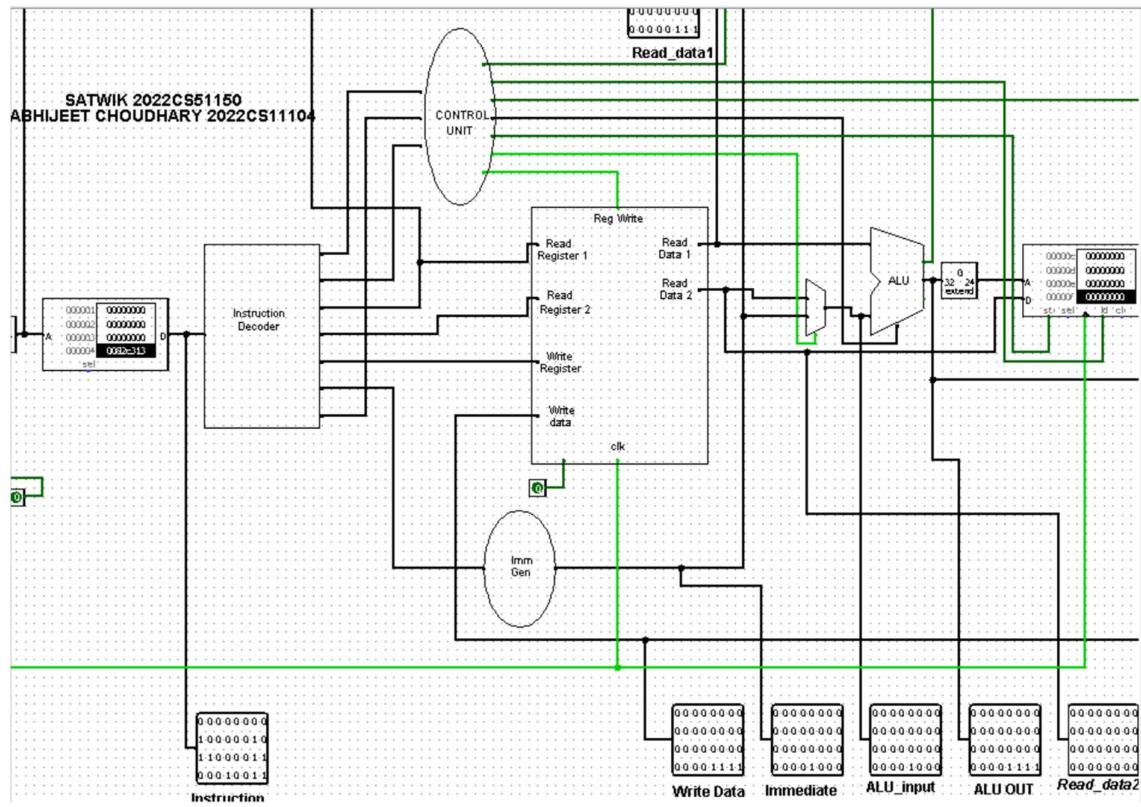
`slti x6,x5,8`



11. XORI

`addi x5,x5,7`

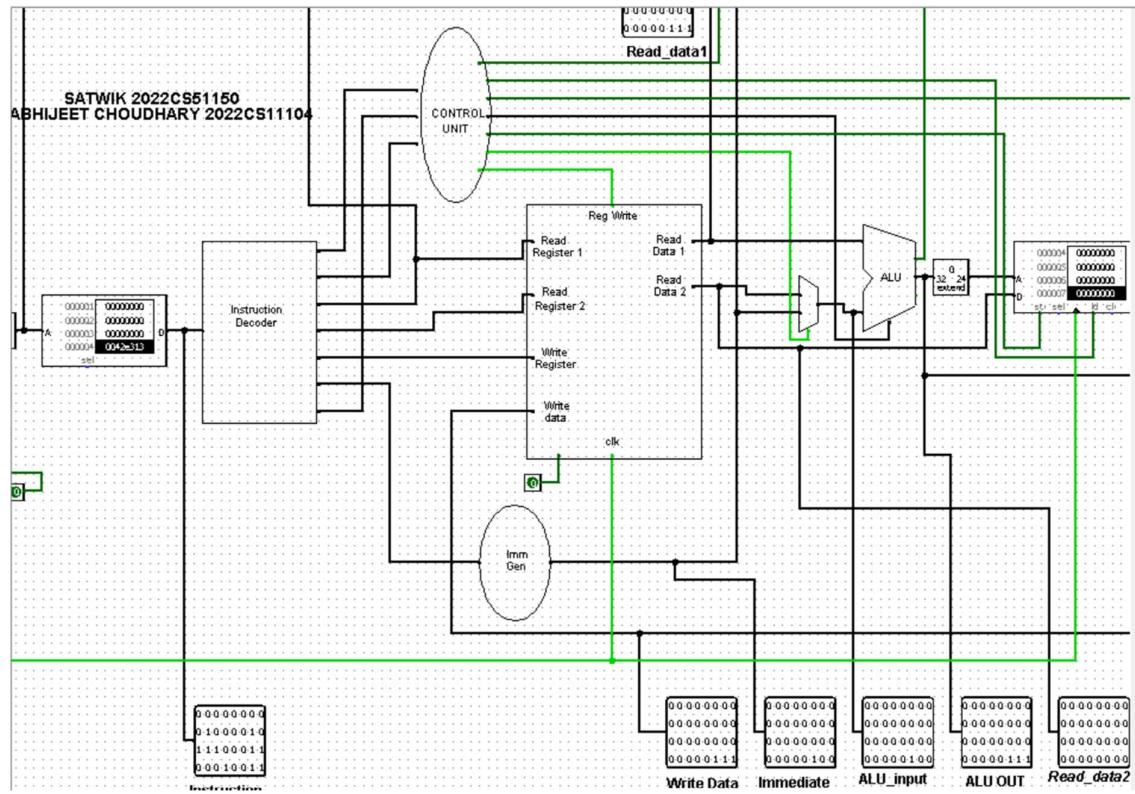
`xori x6,x5,8`



12. ORI

addi x5,x5,7

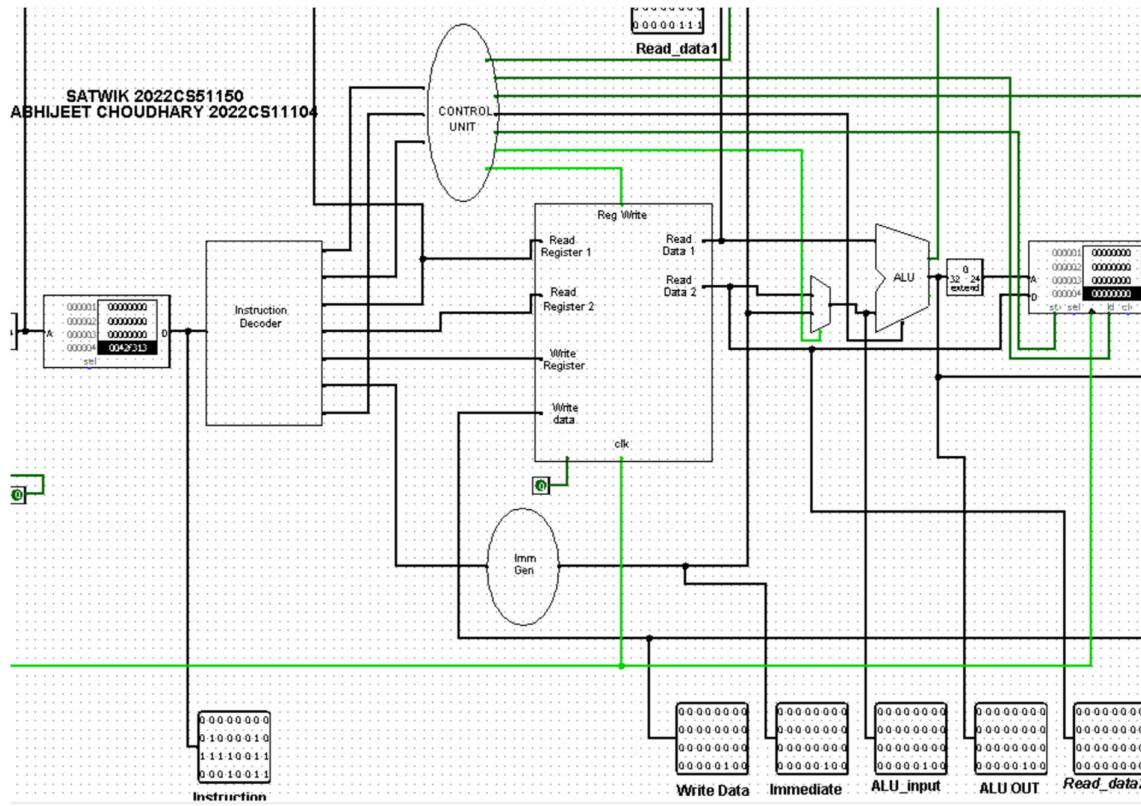
ori x6,x5,4



13. ANDI

addi x5,x5,7

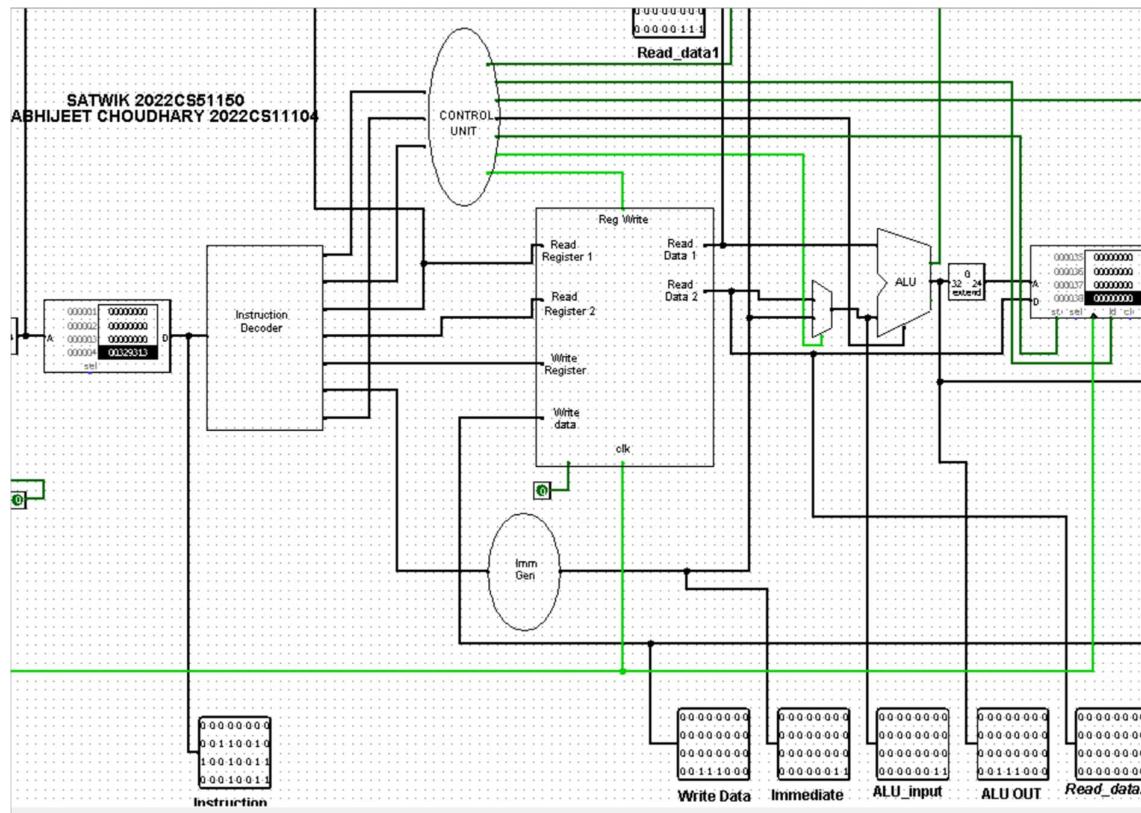
andi x6,x5, 4



14. SLLI

addi x5,x5,7

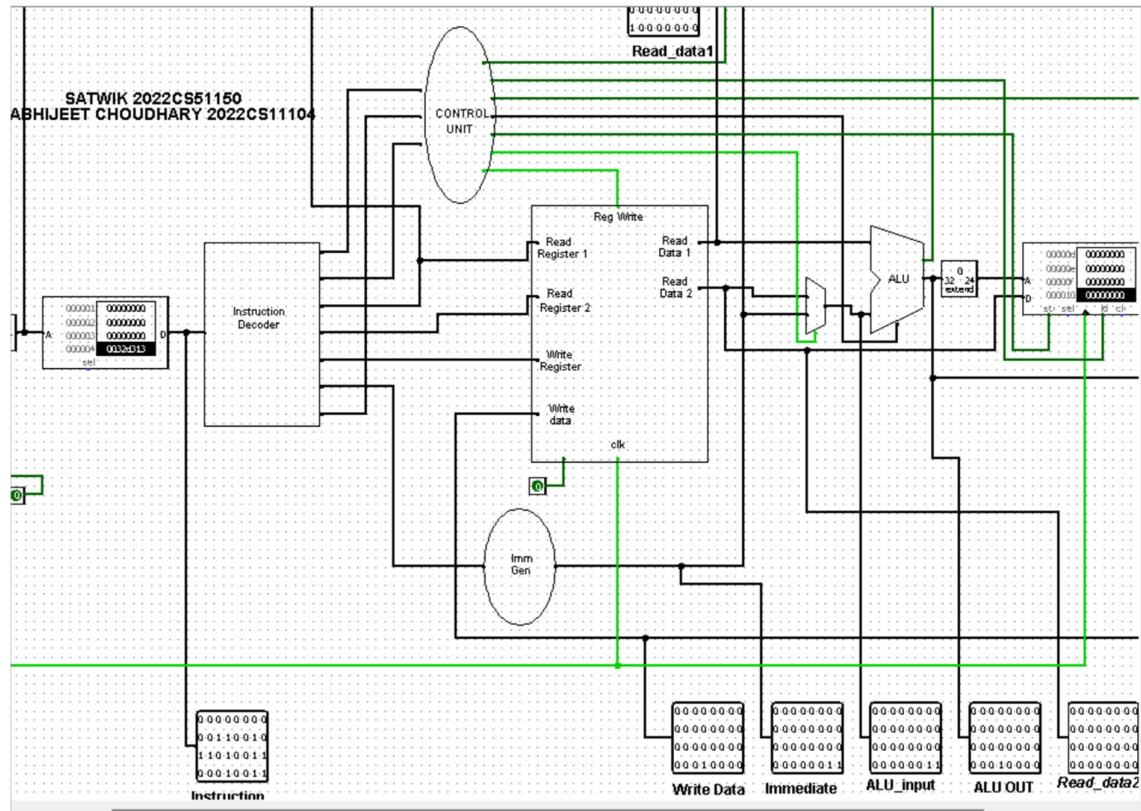
slli x6,x5,3



15. SRLI

`addi x5,x5,128`

`srlx x6,x5,3`

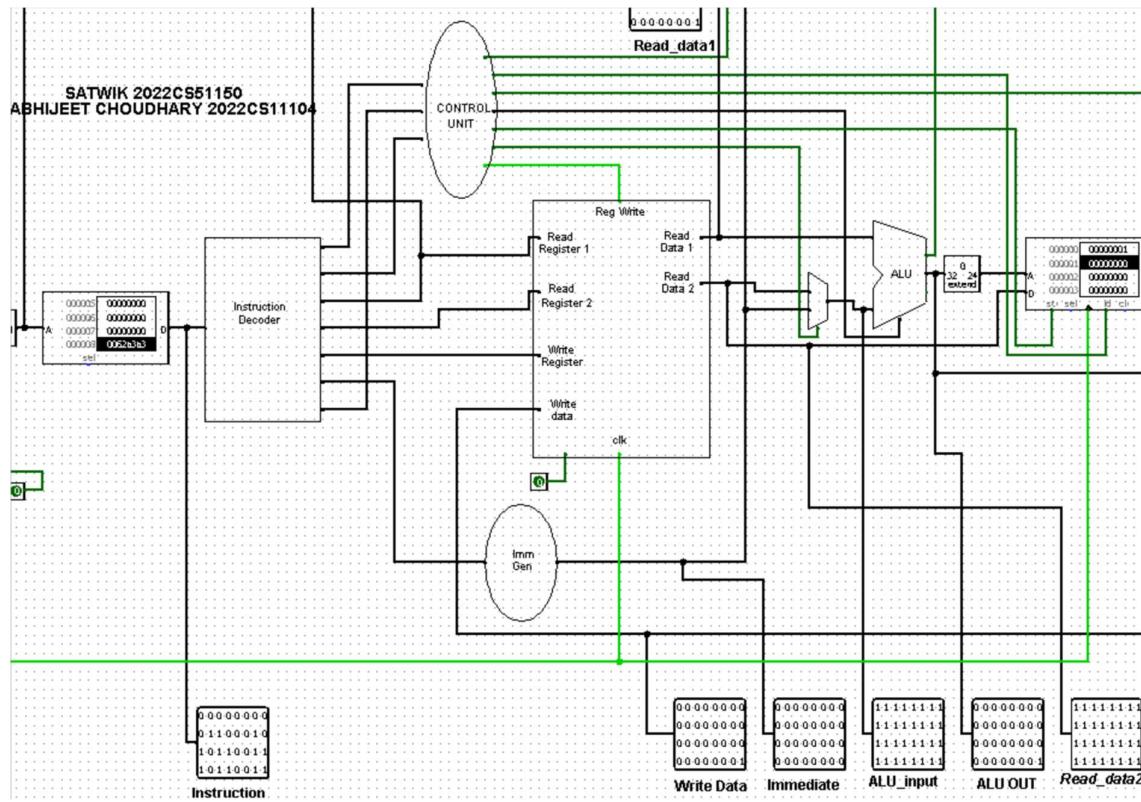


16. SLTU

addi x5,x5,1

addi x6,x6,-1

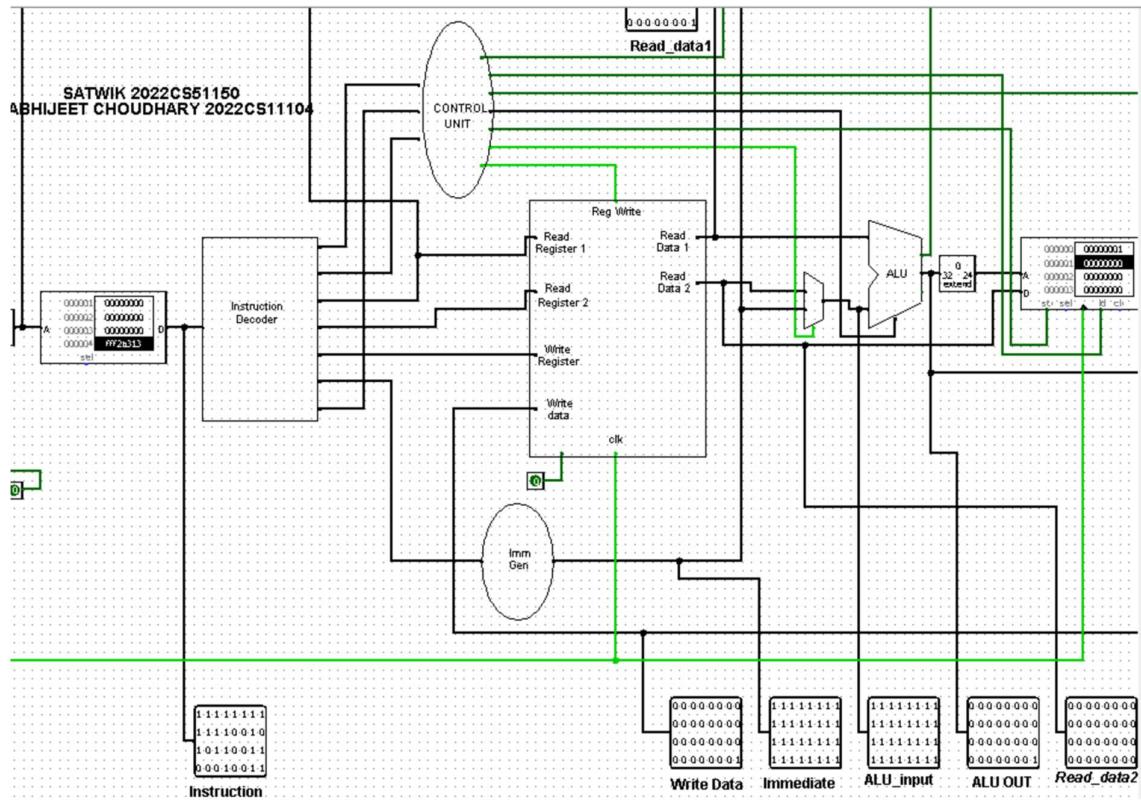
sltu x7,x5,x6



17. SLTIU

`addi x5,x5,1`

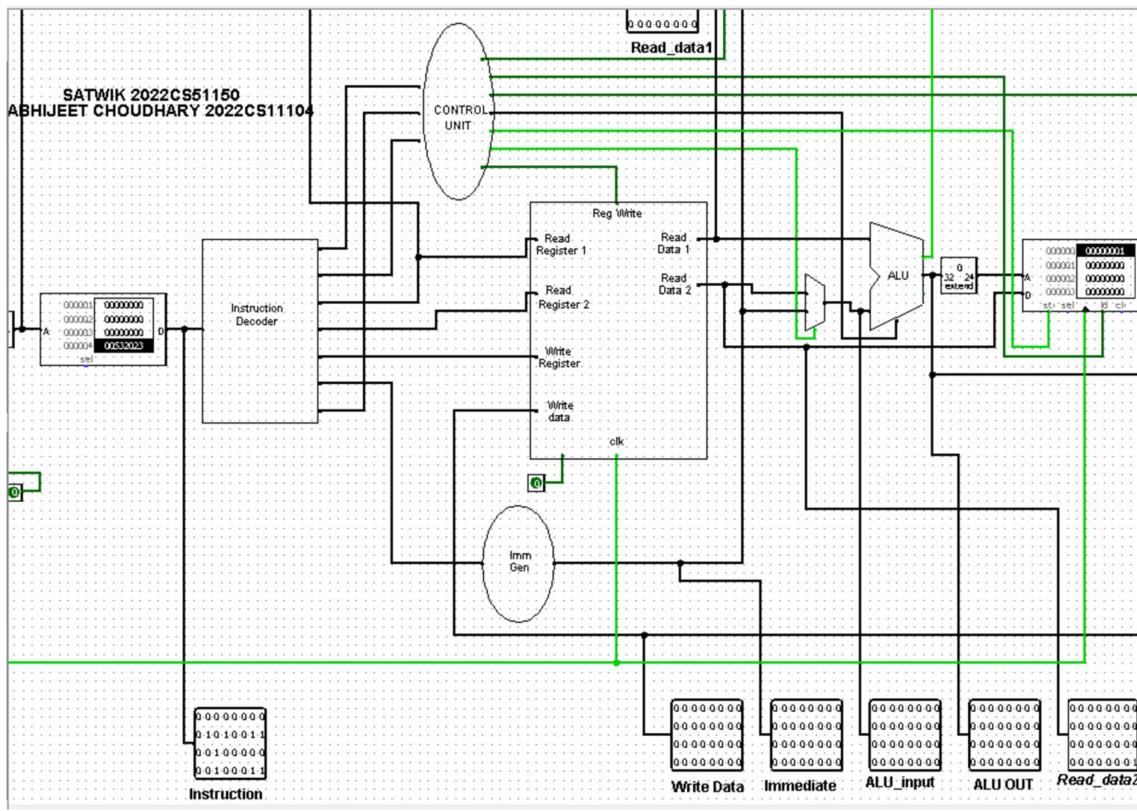
`sltiu x6,x5,-1`



18. SW

addi x5,x5,1

sw x5,0(x6)

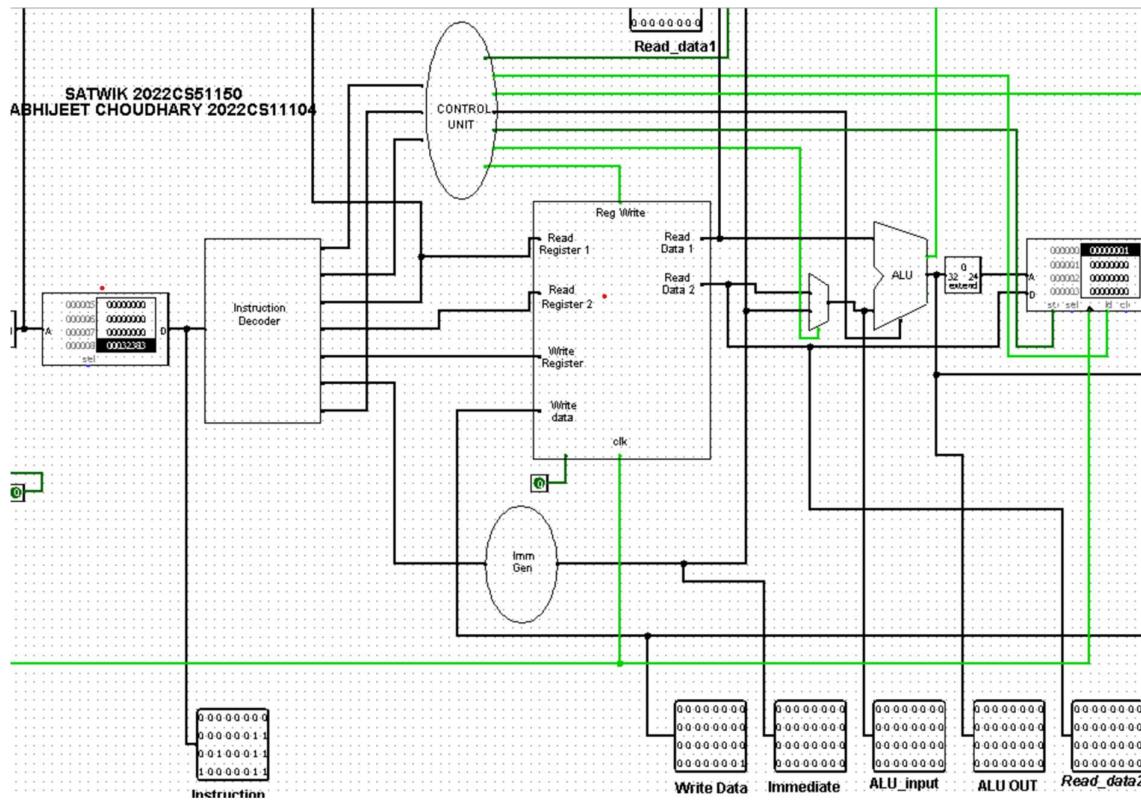


19. LW

`addi x5,x5,1`

`sw x5,0(x6)`

`lw x7,0(x6)`



20. BEQ

addi x5,x5,1

addi x7,x7,1

beq x5,x7,2

