Abhijit Karale

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Profile

Final-year B.Tech ECE student passionate about **Design Verification**, **Analog IC Design**, RTL design, and ASIC flow. Seeking entry-level role to apply **SystemVerilog UVM**, **analog design**, simulation, and verification skills.

Education

MIT College of Railway Engg. and Research, Barshi 08/2023 – 07/2026
B.Tech E&TC — CGPA: 7.86/10 — Courses: Digital VLSI, Analog IC Design, Embedded Systems

Shivnagar Vidya Prasarak Mandal, Baramati 06/2019 – 08/2022
Diploma in Electrical Engg. — 74.40%

Skills

DV: SystemVerilog, UVM, SVA, Functional Coverage, Testbench Architecture
Analog: CMOS physics, Small/Large-signal, Current mirrors, Diff pairs, Op-amps, Bandgap, Stability, Monte Carlo, Layout matching
EDA: Cadence Virtuoso, Spectre, QuestaSim, ModelSim, Vivado, Synopsys DC, Calibre/Assura DRC/LVS
Protocols: AXI4, AXI4-Lite, UART, SPI, I2C
Other: Python, MATLAB, Git, Linux, LaTeX

Experience

Digital Electronics & VLSI Intern — Bengaluru 07/2025

- Designed/simulated combinational & sequential circuits in Verilog.
- Implemented ALUs, FSMs; verified RTL in QuestaSim.
- Optimized designs for area/power; analyzed timing diagrams.

Projects

AXI4-Lite UVM Verification Env (2025) — Constrained-random stimulus, coverage, scoreboard; achieved 95% coverage.
Two-stage CMOS Op-Amp (2025) — 180 nm CMOS, gain ¿ 60 dB, PM ¿ 70°, low power using Cadence Virtuoso.
Smart Traffic Controller FSM (2025) — Adaptive traffic logic in Verilog.
Self-Healing FPGA Circuit (2024) — Partial reconfig. in Verilog/Vivado, patent filed.

Certificates

VLSI SoC Design — Verilog HDL — VLSI Design & Verification (SV/UVM) — Analog CMOS Circuit Design

Languages

English – Professional Marathi – Full Professional Hindi – Native/Bilingual