

ARCHITECTURE IMPLEMENTATION

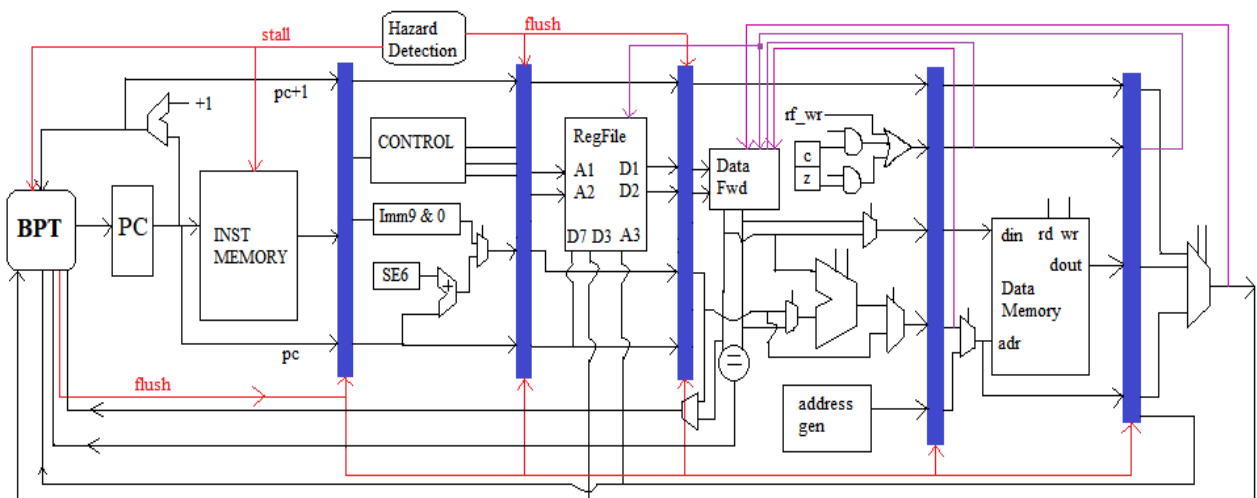


FIG 1. DATAPATH OF 16-BIT RISC PROCESSOR

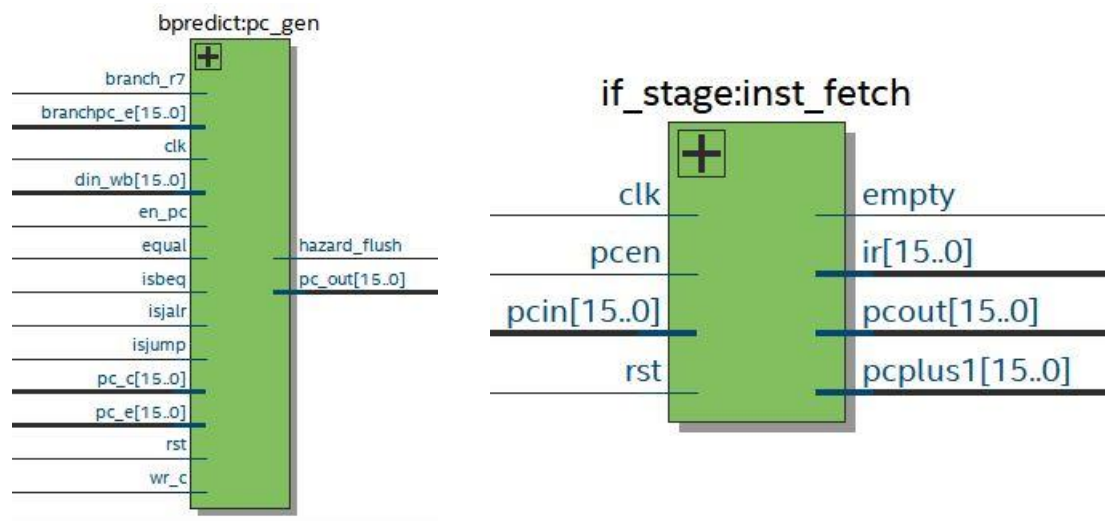


FIG 2. STAGE 1: BRANCH PREDICTION MODULE AND INSTRUCTION FETCH STAGE

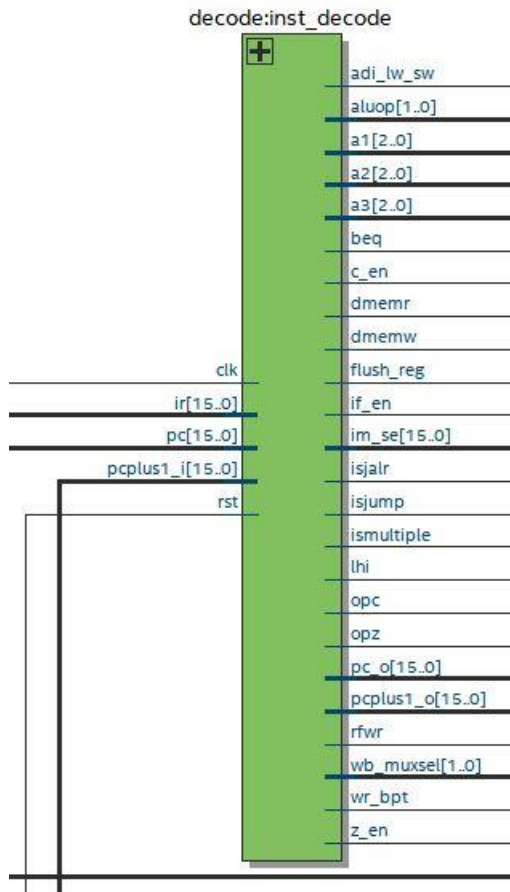


FIG 3. STAGE 2: CONTROL/DECODE STAGE

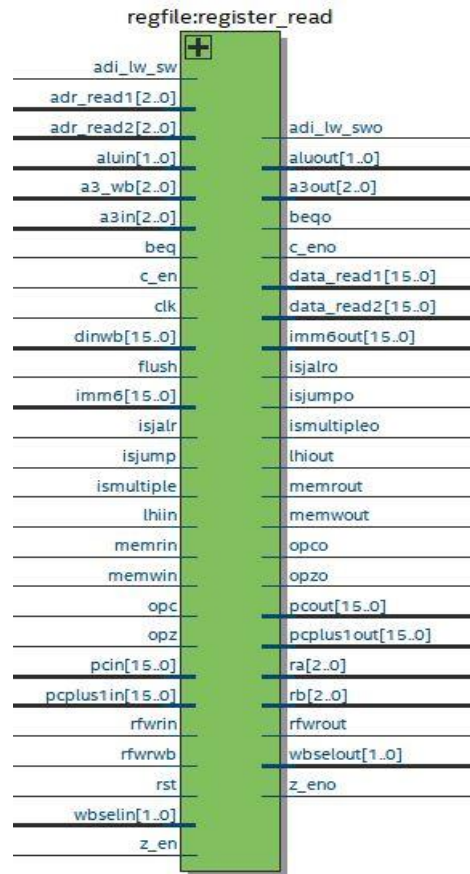


FIG 4. STAGE 3: REGISTER READ(OPERAND FETCH)



FIG 5. STAGE 4: EXECUTE MODULE

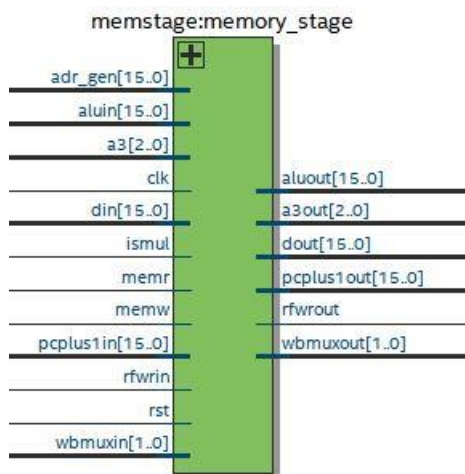


FIG 6. STAGE 5: DATA MEMORY READ

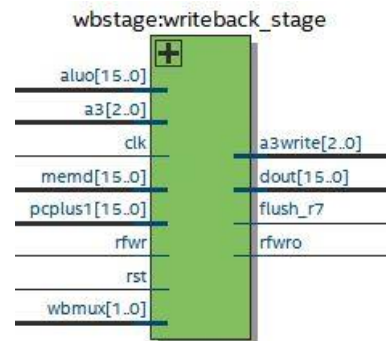


FIG 7. STAGE 6: WRITEBACK



FIG 8. SIMULATION WAVEFORMS FOR VARIOUS TEST CASES

FOLLOWING ARE THE CORRESPONDING TEST CASE FOR THE ABOVE FIGURES:

- 0 => "0011000000000001", --LHI R0 X0080
- 1 => "0011001000000010", --LHI R1 X0100
- 2 => "0011010000000100", --LHI R2 X0200
- 3 => "0011011000001000", --LHI R3 X0400
- 4 => "0011100000010000", --LHI R4 X0800
- 5 => "0011101000100000", --LHI R5 X1000
- 6 => "0011110001000000", --LHI R6 X2000

- 0 => "0011000000000001", --LHI R0 X0080
- 1 => "1000001000100010", --JAL R1 X0020
- 35 => "1100010011100000", --BEQ R2 R3 X0020

- 0 => "0101000010000000", --SW R0 R2+X00
- 1 => "0000100101110000", --ADD R4 R5 R6
- 2 => "0000001010011000", --ADD R1 R2 R3
- 3 => "0000011110110010", --ADC R3 R6 R6
- 4 => "0000001101110001", --ADZ R1 R5 R6
- 5 => "0001100101000001", --ADI R4 R5 X01
- 6 => "0100011010000000", --LW R3 R2+X00
- 7 => "1100011100000000", --BEQ R3 R4 X00

- 0 => "0111000000111010", --SM R0 11111010
- 1 => "0000100101110000", --ADD R4 R5 R6
- 2 => "0000001010011000", --ADD R1 R2 R3

3 => "0000000110110010",	--ADC R3 R6 R6
4 => "0000001101110001",	--ADZ R1 R5 R6
5 => "0001100101000001",	--ADI R4 R5 X01
6 => "0100011010000000",	--LW R3 R2+X00
7 => "1100011100000000",	--BEQ R3 R4 X00

- x"3212", --LHI
- x"3212", --LHI
- x"3401", --LHI
- x"029a", --ADC
- x"5281", --SW
- x"4881", --LW
- x"0858", --ADD
- x"8a05", --JAL
- x"0000", --ADD
- x"1234", --ADI
- x"1234", --ADI
- x"1234", --ADI
- x"1d42", --ADI
- x"7abf", --SM
- x"7823", --SM
- x"3001", --LHI
- x"6a75", --LM
- x"6c85", --LM
- x"7a3a", --SM
- x"c207", --BEQ
- x"8af2", --JAL
- x"3212", --LHI