Name:-Suhas Madhukar Kolse.

Roll no.:-3039

VHDL Code:- library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_Unsigned.ALL;

entity ALU\_3039 is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

sel : in STD\_LOGIC\_VECTOR (2 downto 0);

y : out STD\_LOGIC\_VECTOR (3 downto 0));

end ALU\_3039;

architecture Behavioral of ALU\_3039 is

begin

process (a,b,sel)

begin

case sel is

when "000"=>y<=a+b;

when "001"=>y<=a-b;

when "010"=>y<=a;

when "011"=>y<=a+1;

when "100"=>y<=a nand b;

when "101"=>y<=a nor b;

when "110"=>y<=a xor b;

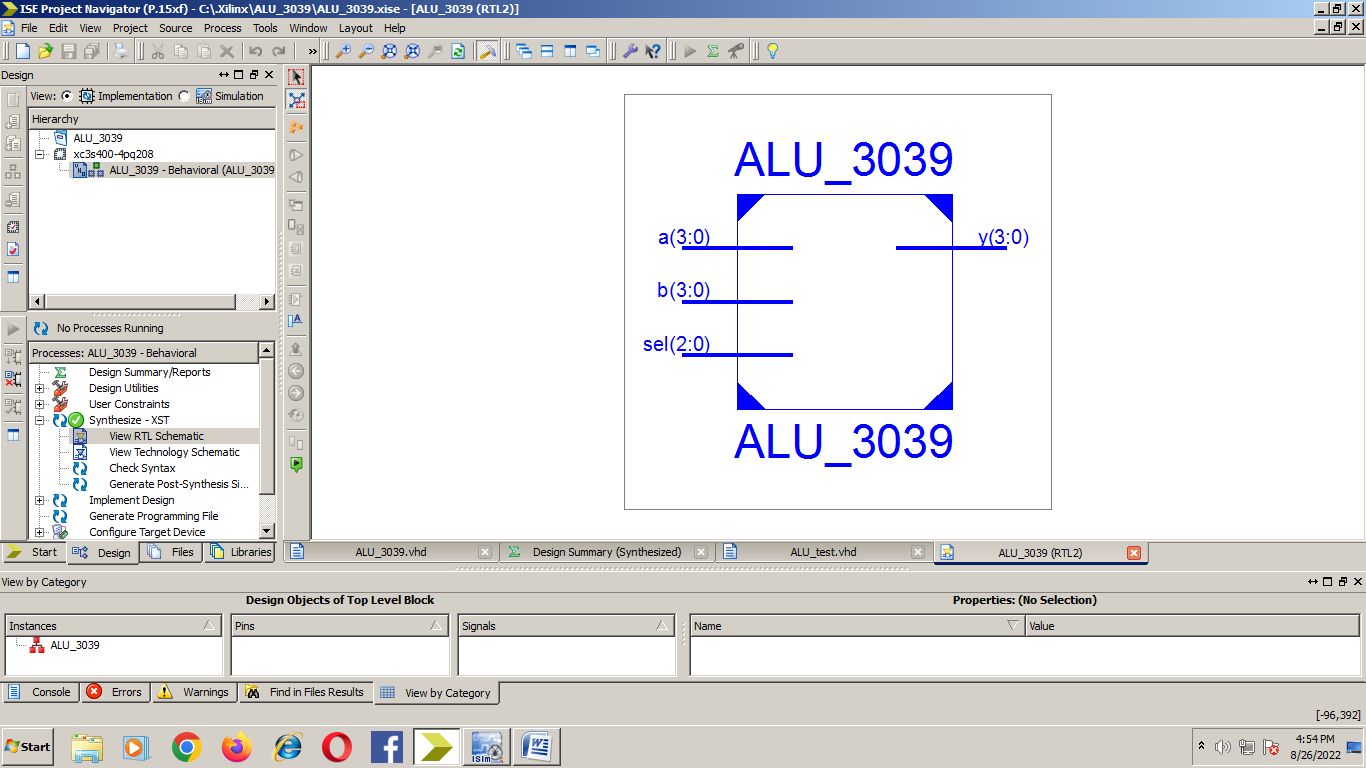
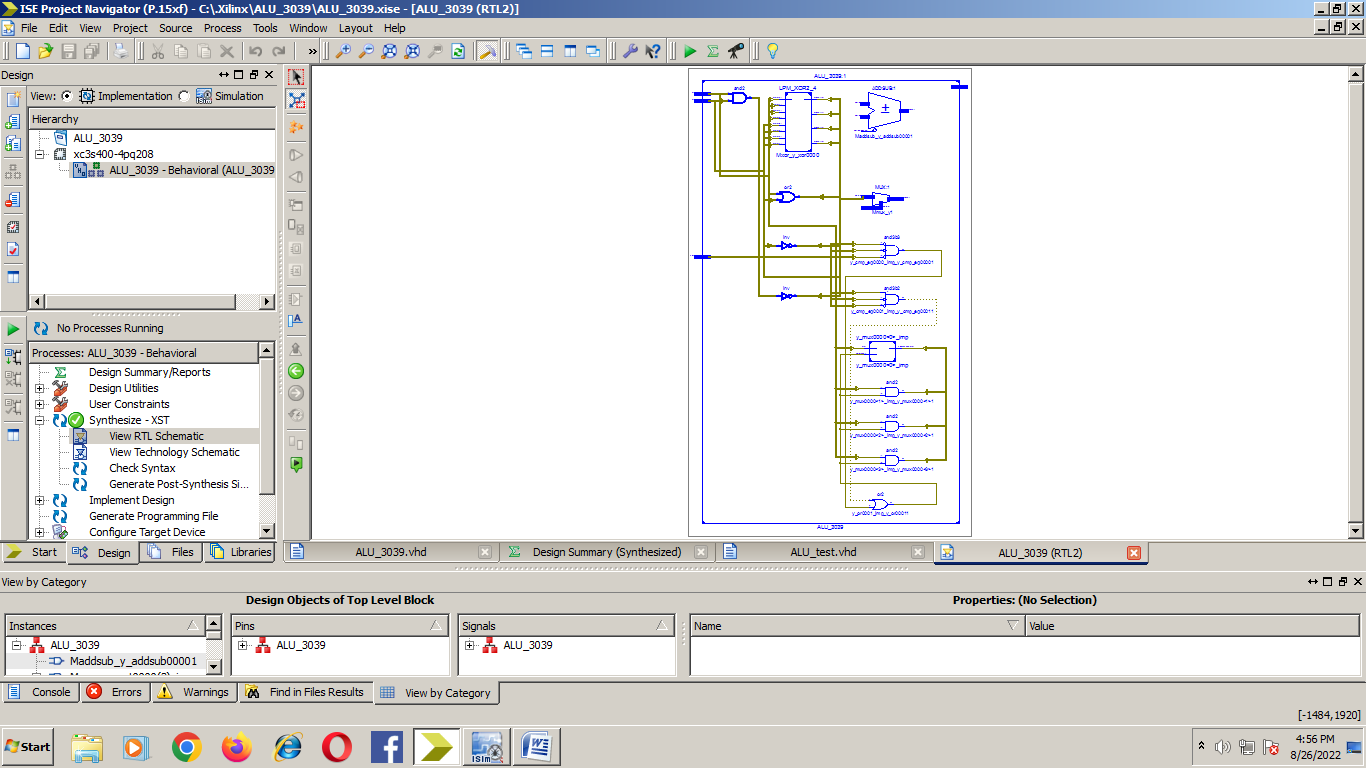
when "111"=>y<=a or b;

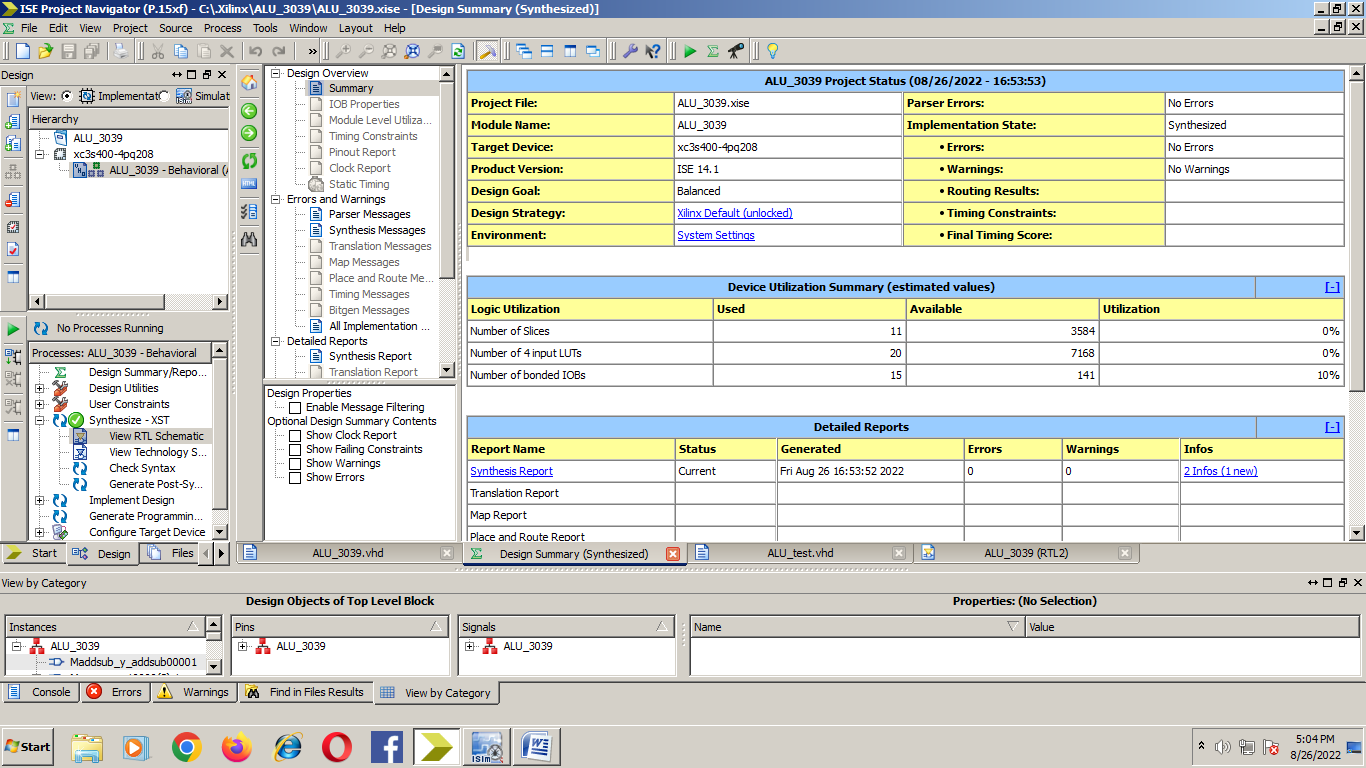
when others =>y<="0000";

end case;

end process;

end Behavioral;

RTL Schematic:- 

Design Summary:-

VHDL Testbench:- LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY ALU\_test IS

END ALU\_test;

ARCHITECTURE behavior OF ALU\_test IS

COMPONENT ALU\_3039

PORT(

a : IN std\_logic\_vector(3 downto 0);

b : IN std\_logic\_vector(3 downto 0);

sel : IN std\_logic\_vector(2 downto 0);

y : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

signal a : std\_logic\_vector(3 downto 0) := (others => '0');

signal b : std\_logic\_vector(3 downto 0) := (others => '0');

signal sel : std\_logic\_vector(2 downto 0) := (others => '0');

signal y : std\_logic\_vector(3 downto 0);

BEGIN

uut: ALU\_3039 PORT MAP (

a => a,

b => b,

sel => sel,

y => y

);

stim\_proc: process

begin

a<="0100";

b<="0011";

sel<="000";

wait for 100 ns; a<="0100";

b<="0011";

sel<="001";

wait for 100 ns a<="0100";

b<="0011";

sel<="010";

wait for 100 ns; a<="0100";

b<="0011";

sel<="011";

wait for 100 ns; a<="0100";

b<="0011";

sel<="100";

wait for 100 ns; a<="0100";

b<="0011";

sel<="101";

wait for 100 ns; a<="0100";

b<="0011";

sel<="110";

wait for 100 ns; a<="0100";

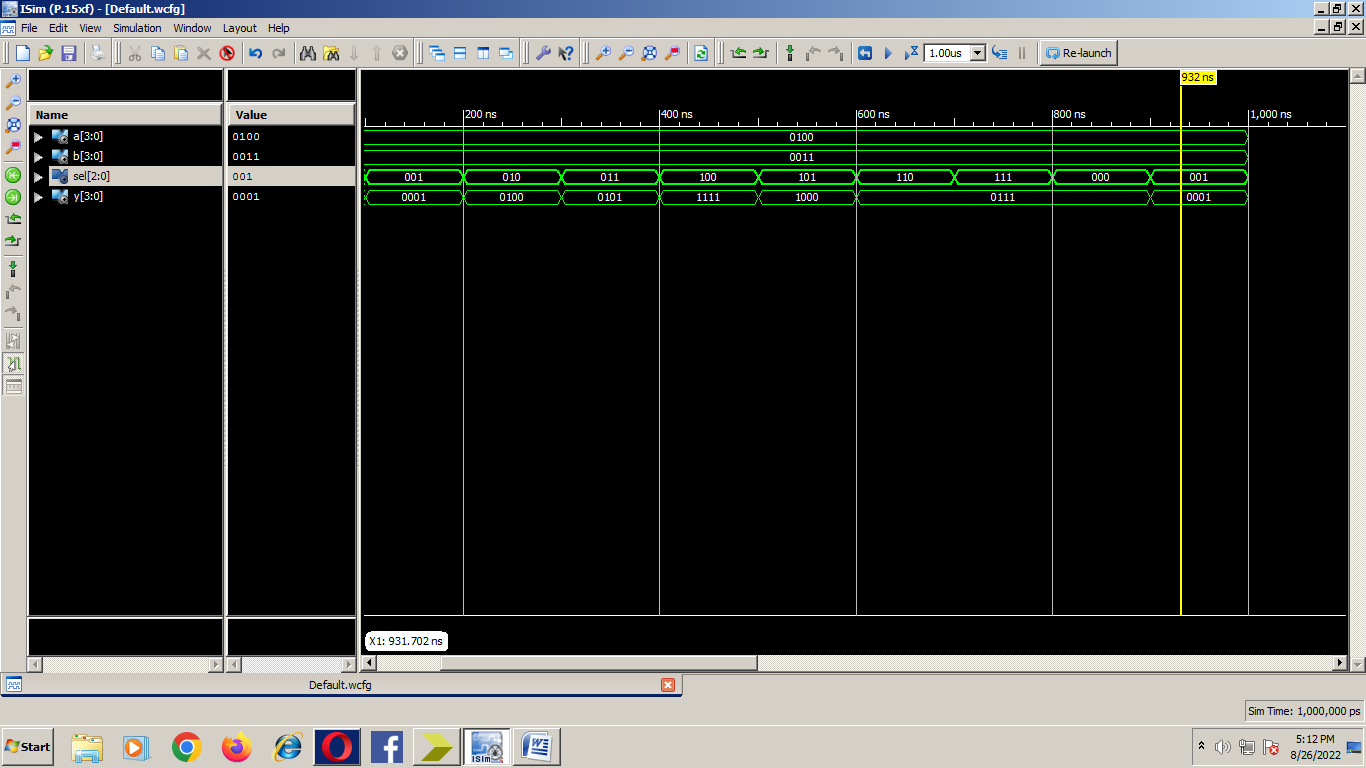
b<="0011";

sel<="111";

wait for 100 ns;

end process;

END;

Simulation:- 

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\* Final Report \*

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Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 17.414ns

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Process "Synthesize - XST" completed successfully