Name:-Suhas Madhukar Kolse.

Roll No.:-E43039

VHDL Code:-library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity USR\_3039 is

Port ( Si : in STD\_LOGIC;

Pi : in STD\_LOGIC\_VECTOR(7 downto 0);

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

Mode : in STD\_LOGIC\_VECTOR(1 downto 0);

So : out STD\_LOGIC;

Po : out STD\_LOGIC\_VECTOR(7 downto 0));

end USR\_3039;

architecture Behavioral of USR\_3039 is

Signal temp:STD\_LOGIC\_VECTOR(7 downto 0);

begin

Process(Clk,Rst)

begin

if (Rst='1')then

temp<="00000000";

elsif(Clk'event AND clk ='1') then

case mode is

when "00"=>

temp(7)<=Si;

temp(6 downto 0)<= temp(7 downto 1);

So<=temp(0);

when "01"=>

temp <=Pi;

temp(6 downto 0)<= temp(7 downto 1);

So<=temp(0);

when "10"=>

temp(7)<=Si;

temp(6 downto 0)<= temp(7 downto 1);

Po <=temp ;

when "11"=>

Po<=Pi;

When others =>

temp<="00000000";

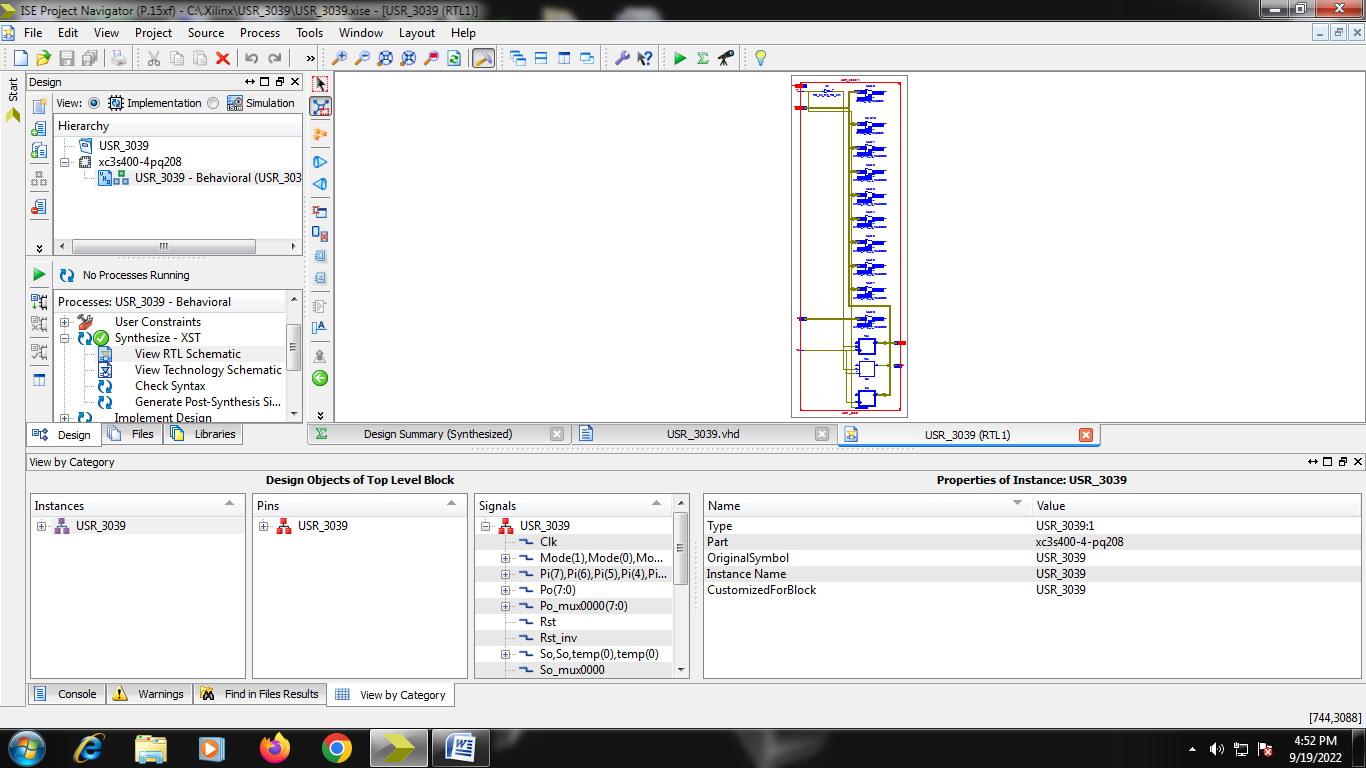
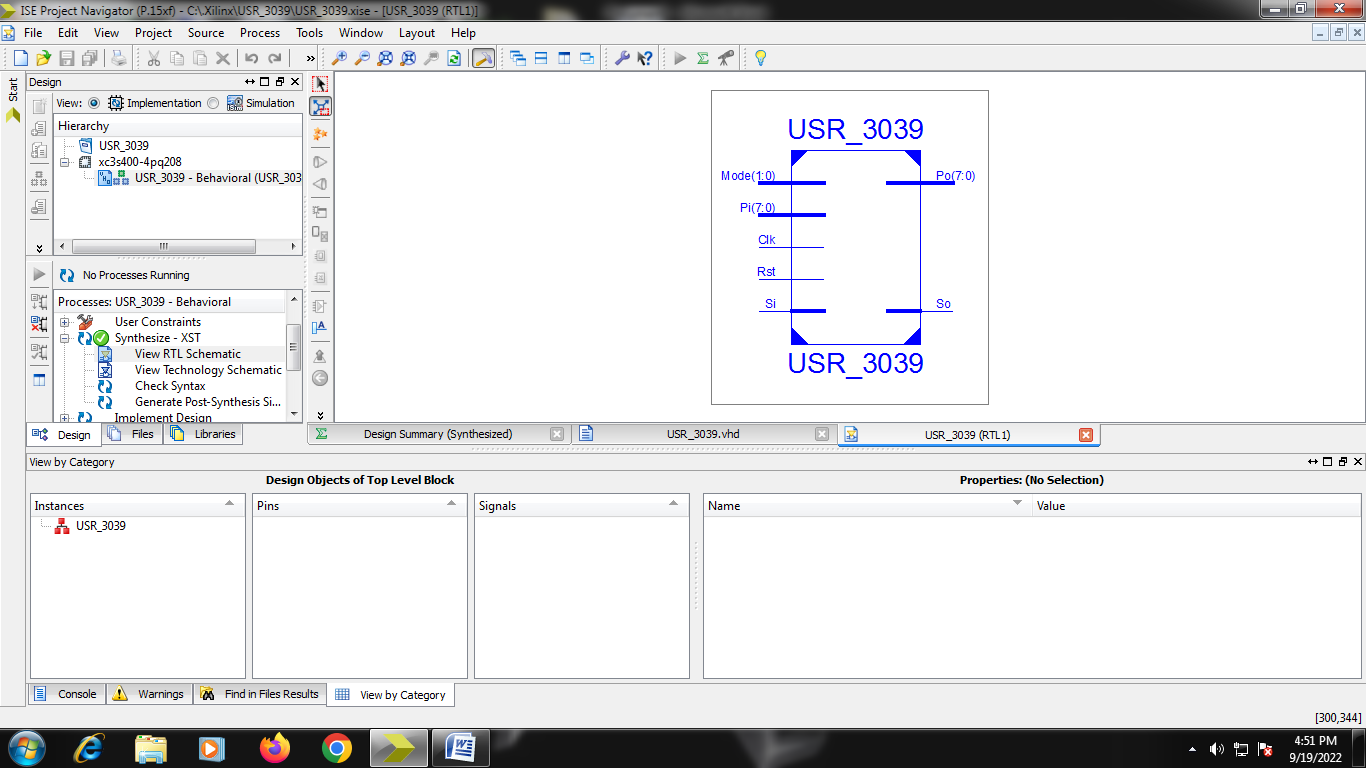
end case;

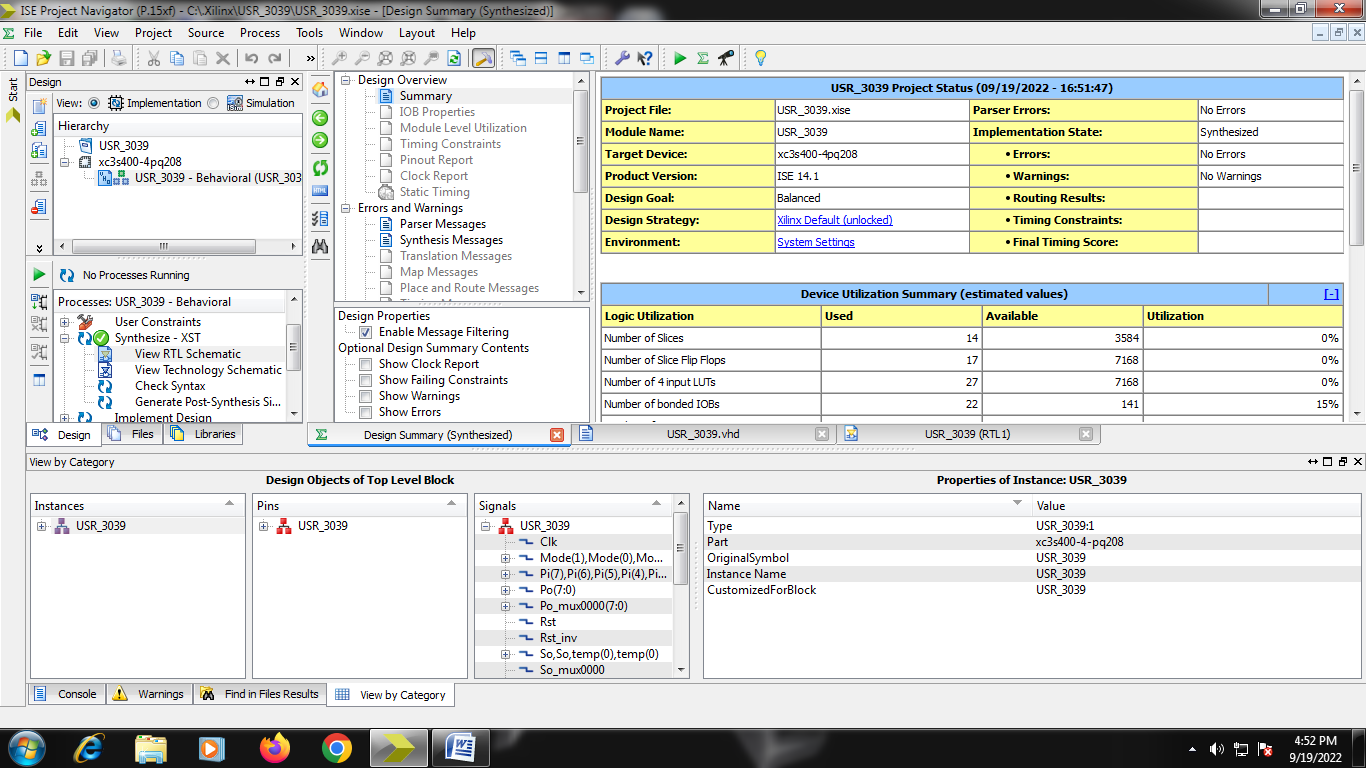
end if;

end process;

end Behavioral;

RTL Schematic:-



Design Summary:-

Testbench:-

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY us\_testbench IS

END us\_testbench;

ARCHITECTURE behavior OF us\_testbench IS

COMPONENT USR\_3039

PORT(

Si : IN std\_logic;

Pi : IN std\_logic\_vector(7 downto 0);

Mode : IN std\_logic\_vector(1 downto 0);

Rst : IN std\_logic;

Clk : IN std\_logic;

So : OUT std\_logic;

Po : OUT std\_logic\_vector(7 downto 0)

);

END COMPONENT;

--Inputs

signal Si : std\_logic := '0';

signal Pi : std\_logic\_vector(7 downto 0) := (others => '0');

signal Mode : std\_logic\_vector(1 downto 0) := (others => '0');

signal Rst : std\_logic := '0';

signal Clk : std\_logic := '0';

--Outputs

signal So : std\_logic;

signal Po : std\_logic\_vector(7 downto 0);

-- Clock period definitions

constant Clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: USR\_3039 PORT MAP (

Si => Si,

Pi => Pi,

Mode => Mode,

Rst => Rst,

Clk => Clk,

So => So,

Po => Po);

-- Clock process definitions

Clk\_process :process

begin

Clk <= '0';

wait for Clk\_period/2;

Clk <= '1';

wait for Clk\_period/2;

end process;

-- Stimulus process

stim\_proc: process

begin

-- hold reset state for 100 ns.

wait for 100 ns;

Rst<='1';

wait for 10 ns;

Rst<='0';

Mode<="00";

Si<='1';

wait for 10 ns;

Rst<='0';

Mode<="00";

Si<='0';

wait for 80 ns;

Rst<='0';

Mode<="10";

Pi<="10101010";

wait for 100 ns;

Rst<='1';

wait for 10 ns;

Rst<='0';

Mode<="11";

Pi<="11001100";

wait for 80 ns;

wait for Clk\_period\*10;

-- insert stimulus here

wait;

end process;

END;

=========================================================================

\* Final Report \*

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Final Results

RTL Top Level Output File Name : USR\_3039.ngr

Top Level Output File Name : USR\_3039

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 22

Cell Usage :

# BELS : 28

# INV : 1

# LUT3 : 9

# LUT3\_L : 8

# LUT4 : 9

# MUXF5 : 1

# FlipFlops/Latches : 17

# FDC : 8

# FDE : 9

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 21

# IBUF : 12

# OBUF : 9

Waveform:-

