Tutorial 8

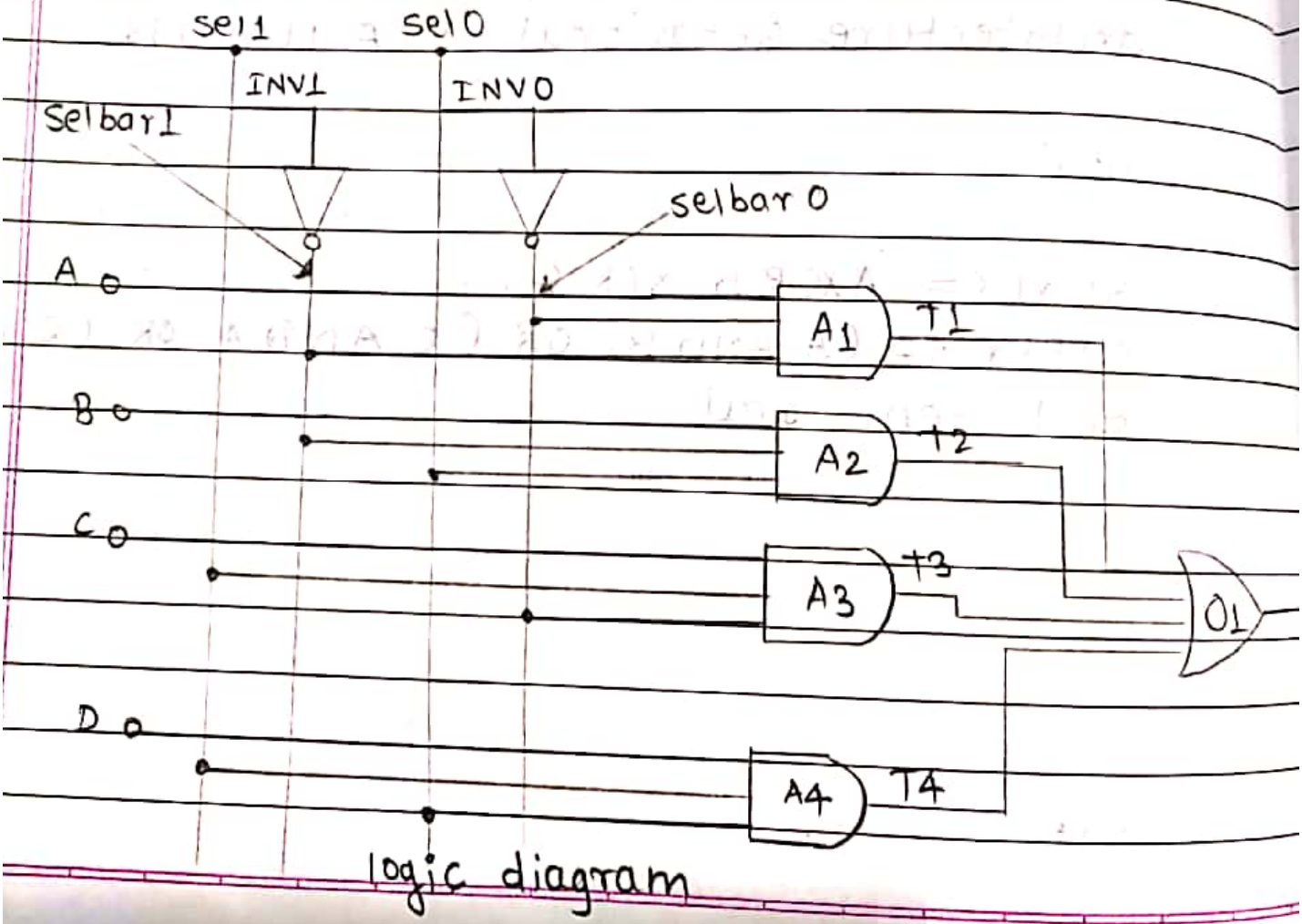
Simulation of Full Adder using behavioural modelling style of VHDL.

```
library IEEE;
use IEEE.STD-LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity FULLADD is
    Port (A: in STD_LOGIC;
          B: in STD-LOGIC;
          C: in STD-LOGIC
          SUM: out STD-LOGIC;
          CARRY: out STD-LOGIC);
end FULLADD

architecture Behavioral of FULLADD is

begin

SUM <= A XOR B XOR C;
CARRY <= (A AND B) OR (C AND A) OR (C AND
end Behavioral.
```

Tutorial 9

simulation of 4:1 mux using data flow modelling style of VHDL.

```
architecture dataflow of MUX4_1 is
signal selbar0, selbar1, t1, t2, t3, t4: std_logic;

begin
   selbar0 <= not sel0;
   selbar1 <= not sel1;
   t1 <= A AND selbar0 and selbar1;
   t2 <= B AND sel0 and selbar1;
   t3 <= C and selbar0 and sel1;
   t4 <= D and sel0 and sel1;
   Y <= t1 or t2 or t3 or t4;
end dataflow;
```



logic diagram