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Custom RISC-V DSP Processor - Complete Documentation

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1. Project Overview

What is this project?

This project implements a **custom RISC-V based Digital Signal Processing (DSP) processor** optimized for real-time signal processing applications. It's not just using Verilog to connect existing modules - it's a complete processor architecture design with custom DSP extensions.

Key Features

32-bit RISC-V ISA

Base RISC-V instruction set with custom DSP extensions

Hardware MAC Unit

Single-cycle multiply-accumulate operations with saturation

SIMD Instructions

Parallel processing (4x 8-bit or 2x 16-bit operations)

5-Stage Pipeline

With hazard detection and forwarding

Complete Software Stack

C code and DSP algorithms

FPGA-Ready

Synthesis scripts and constraints

Why it's impressive

- **Custom processor design** - not just module assembly
- **Hardware-software co-design** - C code optimized for hardware features

- **Real DSP algorithms** - FIR filters, FFT, convolution
- **Professional verification** - comprehensive testbenches
- **Production-ready** - synthesis scripts and documentation

2. Architecture Design

Processor Pipeline

```
IF (Instruction Fetch) → ID (Decode) → EX (Execute) → MEM (Memory) → WB (Write Back)
```

Memory Organization

Component	Size	Type	Description
Instruction Memory	16KB	ROM	Program storage
Data Memory	8KB	RAM	Data storage
Register File	32 x 32-bit	Registers	General-purpose registers
Special Features	-	-	Circular addressing, bit-reverse addressing

DSP Optimizations

- **Single-cycle MAC operations**
- **Parallel SIMD processing**
- **Saturation arithmetic**
- **Hardware-accelerated DSP functions**

3. File Structure

```
DSPProjec/
├── src/ # Verilog source files
│ ├── riscv_dsp_core.v # Main processor core
│ ├── alu.v # Arithmetic Logic Unit
│ ├── mac_unit.v # MAC unit
│ ├── simd_unit.v # SIMD unit
│ ├── register_file.v # Register file
│ ├── instruction_decoder.v # Instruction decoder
│ ├── control_unit.v # Control unit
│ └── memory_interface.v # Memory interface
├── software/ # C software implementation
│ ├── main.c # Main application
│ ├── fir_filter.c # FIR filter implementation
│ ├── fft.c # FFT implementation
│ └── dsp_math.h # DSP math library
├── testbench/ # Testbenches
│ ├── mac_unit_tb.v # MAC unit testbench
│ ├── simd_unit_tb.v # SIMD unit testbench
│ ├── alu_tb.v # ALU testbench
│ └── processor_tb.v # Processor testbench
├── scripts/ # Synthesis scripts
│ └── synthesize.tcl # Vivado synthesis script
├── constraints/ # Timing constraints
│ └── riscv_dsp_constraints.xdc
├── docs/ # Documentation
│ ├── architecture.md # Architecture documentation
│ ├── instruction_set.md # Instruction set documentation
│ └── Project_Documentation.md # This file
└── README.md # Project overview
```

4. Hardware Components

1. Main Processor Core

`src/riscv_dsp_core.v`

Purpose: Main processor module that integrates all components

Key Features:

- 5-stage pipeline implementation
- Component integration (ALU, MAC, SIMD, memory, control)
- Pipeline register management
- Hazard detection and forwarding
- Branch and jump control logic

Key Signals:

- `clk`, `rst_n` : Clock and reset
- `external_data_in/out` : External data interface
- `processor_ready` : Processor ready signal

Pipeline Stages:

1. **IF**: Instruction fetch from memory
2. **ID**: Instruction decode and register read
3. **EX**: Execute (ALU/MAC/SIMD operations)
4. **MEM**: Memory access
5. **WB**: Write back to register file

2. Arithmetic Logic Unit

`src/alu.v`

Purpose: Extended ALU with DSP-specific operations

Key Features:

- Standard RISC-V operations (ADD, SUB, AND, OR, XOR, shifts, comparisons)
- DSP-specific operations (SAT, CLIP, ROUND, bit manipulation)
- Saturation arithmetic support

- Status flags (zero, overflow, carry, negative)

Operations:

Category	Operations
Standard	ADD, SUB, AND, OR, XOR, SLL, SRL, SRA, SLT, SLTU
DSP	SAT (saturate to 16-bit), CLIP (clip to range), ROUND (round to nearest)
Bit ops	BIT_TEST, BIT_SET, BIT_CLEAR, BIT_TOGGLE

3. MAC Unit

`src/mac_unit.v`

Purpose: Hardware Multiply-Accumulate unit for DSP operations

Key Features:

- Single-cycle MAC operations
- Multiple modes (signed, unsigned, mixed)
- Saturation and rounding support
- Overflow/underflow detection

Operation:

```
result = a * b + c
```

Modes:

Mode	Description
00	Signed × Signed
01	Unsigned × Unsigned
10	Signed × Unsigned
11	Reserved

4. SIMD Unit

`src/simd_unit.v`

Purpose: Single Instruction, Multiple Data unit for parallel processing

Key Features:

- 4x 8-bit or 2x 16-bit parallel operations
- Multiple operation types (ADD, SUB, MUL, AND, OR, XOR, SHIFT)
- Overflow detection per element
- Configurable data width

Operations:

- **8-bit:** ADD4, SUB4, MUL4, AND4, OR4, XOR4, SHIFT4
- **16-bit:** ADD2, SUB2, MUL2

Example:

`ADD4` performs 4 parallel additions:

```
Input A: [a3, a2, a1, a0]
Input B: [b3, b2, b1, b0]
Output:  [a3+b3, a2+b2, a1+b1, a0+b0]
```

5. Register File

`src/register_file.v`

Purpose: 32 general-purpose registers with dual-port read

Key Features:

- 32 x 32-bit registers
- Dual-port read, single-port write
- Register x0 always returns zero
- Synchronous write, combinational read

6. Instruction Decoder

`src/instruction_decoder.v`

Purpose: Decodes RISC-V instructions and DSP extensions

Key Features:

- Standard RISC-V instruction decoding
- Custom DSP instruction extensions
- Control signal generation
- Immediate extraction and sign extension

7. Control Unit

`src/control_unit.v`

Purpose: Pipeline control, hazard detection, and forwarding

Key Features:

- Load-use hazard detection
- Data forwarding logic
- Stall and flush control
- Branch and jump handling

8. Memory Interface

`src/memory_interface.v`

Purpose: DSP-optimized memory access

Key Features:

- 16KB instruction memory
- 8KB data memory
- Circular addressing mode
- Bit-reverse addressing for FFT
- Byte/halfword/word access

5. Software Implementation

1. DSP Math Library

`software/dsp_math.h`

Purpose: Header file with hardware-optimized DSP functions

Key Features:

- Hardware MAC instruction wrappers
- SIMD operation wrappers
- Saturation and clipping functions
- DSP utility functions

Hardware Intrinsics:

```
static inline int32_t mac(int32_t acc, int16_t a, int16_t b);
static inline int32_t simd_mac4(int16_t *coeffs, int16_t *samples);
static inline int16_t saturate_16(int32_t value);
```

2. FIR Filter Implementation

`software/fir_filter.c`

Purpose: Hardware-optimized FIR filter implementation

Key Features:

- MAC-optimized processing
- SIMD parallel processing
- Filter design functions
- Real-time processing support

Filter Structure:

```
typedef struct {
    int16_t *coeffs;        // Filter coefficients
    int16_t *delay_line;    // Delay line buffer
    int16_t tap_count;      // Number of filter taps
    int16_t index;          // Current delay line index
} fir_filter_t;
```

3. FFT Implementation

`software/fft.c`

Purpose: Hardware-accelerated FFT implementation

Key Features:

- Radix-2 FFT algorithm
- Bit-reverse addressing
- Hardware MAC for complex operations
- Power spectrum calculation

4. Main Application

`software/main.c`

Purpose: Main DSP application demonstrating FIR filtering and FFT

Key Features:

- Test signal generation
- FIR filter processing
- FFT analysis
- Results display
- Interrupt service routines

6. Verification & Testing

Testbenches

File	Purpose	Test Cases
`testbench/mac_unit_tb.v`	MAC unit testing	Basic MAC, accumulation, overflow, saturation
`testbench/simd_unit_tb.v`	SIMD unit testing	8-bit/16-bit operations, overflow detection
`testbench/alu_tb.v`	ALU testing	Standard ops, DSP ops, saturation, flags
`testbench/processor_tb.v`	Full processor testing	Integration tests, DSP algorithms

7. Synthesis & Implementation

1. Synthesis Script

`scripts/synthesize.tcl`

Purpose: Automated synthesis and implementation

Features:

- Project creation

- Source file addition
- Constraint file addition
- Synthesis launch
- Implementation launch
- Report generation
- Bitstream generation

2. Timing Constraints

`constraints/riscv_dsp_constraints.xdc`

Purpose: Timing and physical constraints

Features:

- Clock constraints (100MHz target)
- Input/output delay constraints
- DSP-specific timing constraints
- Pin assignments for Basys 3 board
- Power constraints

8. Usage Instructions

Simulation

```
# Run individual testbenches
make test-mac      # Test MAC unit
make test-simd     # Test SIMD unit
make test-alu      # Test ALU
make test-processor # Test full processor

# Run all tests
make test
```

Synthesis

```
# Synthesize for FPGA
make synth

# View results
vivado synth/riscv_dsp_processor.xpr
```

Software Development

```
# Compile C code
make software

# Run application
./software/dsp_app
```

9. Performance Analysis

Hardware Performance

Metric	Value
Clock Frequency	100MHz target
MAC Latency	1 cycle
SIMD Latency	1 cycle
Memory Access	1 cycle
Pipeline Depth	5 stages

Resource Usage (Xilinx 7-series)

Resource	Usage
LUTs	~2,000
FFs	~1,500
BRAMs	4
DSPs	8

DSP Performance

Algorithm	Performance
FIR Filter	1 cycle per tap
FFT	Hardware-accelerated
SIMD	4x parallel processing
Saturation	Hardware-accelerated

10. Future Enhancements

Planned Features

- **Floating-Point Unit**: IEEE 754 support
- **Cache Memory**: Instruction and data caches
- **DMA Controller**: Direct memory access
- **Interrupt Controller**: Real-time processing
- **Debug Interface**: JTAG support

Optimization Opportunities

- **Pipeline Optimization**: Reduce stalls
- **Memory Bandwidth**: Increase throughput
- **Power Optimization**: Reduce consumption
- **Area Optimization**: Reduce resource usage

Conclusion

This Custom RISC-V DSP Processor project demonstrates:

- **Complete System Design**: From hardware to software
- **Professional Quality**: Comprehensive verification and documentation
- **Real-world Applications**: Practical DSP algorithms
- **Educational Value**: Learning processor design and DSP
- **Production Ready**: Synthesis scripts and constraints

The project showcases advanced digital design skills, DSP knowledge, and hardware-software co-design capabilities. It's an excellent example of a custom processor architecture optimized for specific applications.

Project Repository: [GitHub Link]

Documentation: [Documentation Link]

Issues: [Issues Link]

This documentation was generated for the Custom RISC-V DSP Processor project.

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