HW 1 of the course Automated Software Validation

Date handed out: May 25, 2007
To be returned: June 5, 2007

This assignment should be solved individually. No late submissions will be accepted.

In this assignment, you are required to model the AMBA AHB system-on-chip bus protocol discussed in class. This is a real-life protocol from ARM. You should model and verify the protocol using Cadence SMV. You may download Cadence SMV from http://www.kenmcmil.com/smv.html

The requirements document of the protocol runs into 60+ pages. You can get the official AMBA 2.0 specification from
http://www.arm.com/products/solutions/AMBA_Spec.html
This site might require you register first. If you download the protocol from here, consider only the AMBA AHB protocol (Chapter 3).

To help you get started, I am providing a small model (in SMV itself) which shows a starvation error in the protocol. You can download this small model from
http://www.comp.nus.edu.sg/~abhik/software/amba/ahb.smv

You should go through the requirements document, and model the protocol with multiple masters and multiple slaves. Please do not try to mimic the small model I have given --- instead you should go through the process of system modeling from an actual real-world requirements document. In fact, in your report you will need to explain the steps you went through in the process of modeling the protocol.

In your submission, you should submit the following files.

1. The SMV code, including all the temporal properties you tried out
2. A report (pdf file) detailing your experiences in modeling the protocol, whatever simplifications you made from the requirements to the modeling, justification of those simplifications and summary of verification results.

Please e-mail these files via one single e-mail to abhik@csa.iisc.ernet.in