Preface

This volume contains the proceedings of the First international Workshop on Software Verification and Validation (SVV). SVV took place on December 14, 2003 as a post-conference satellite workshop of the Nineteenth International Conference on Logic Programming (ICLP) that took place at the Tata Institute of Fundamental Research (TIFR), Mumbai, India, December 9–13, 2003.

The goal of SVV is to promote discussion on novel methodologies for software verification as well as study novel combinations of (known) methodologies. An outstanding example of a combined verification methodology is the recent research direction that combines abstraction (of infinite-state programs into finite-state ones) with model checking (of finite-state systems). There is a growing conviction in the research community that such hybrid methodologies are imperative for the process of analyzing full-fledged software systems.

SVV 2003 received 14 submissions out of which 9 papers were selected for presentation at the workshop. The papers were subjected to rigorous review by at least three independent reviewers. In addition to the standard criteria for acceptability, contributions have also been selected on the basis of their conceptual significance in neighboring areas. The topics addressed by the accepted contributions ranged from theoretical techniques and practical methods to case studies for verification of conventional and embedded software systems. Dr Ramesh Bharadwaj from the Naval Research Laboratories delivered an invited talk titled " Rigorous Methods for Software Construction: Retrofitting "Engineering" into Software Engineering".

We would like to thank the program committee and all the referees for their assistance in selecting the papers and the local organizers for mastering the coordination of the workshop as well as the ICLP.

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