

Assignment: 2

Design of CORDIC Processor



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1 Introduction

1.1 Referenced documents

M. Chinnathambi, N. Bharanidharan and S. Rajaram, "FPGA implementation of fast and area efficient CORDIC algorithm," 2014 International Conference on Communication and Network Technologies, Sivakasi, India, 2014, pp. 228-232, doi: 10.1109/CNT.2014. 7062760.

1.2 Design library name

We have used UMC 65 Libraries in our assignment.

1.3 People involved in the block

Arjit Awadhiya

Kushagra Sharma

Abhilash

Abhijeet Kumar

2 Function

2.1 Brief overview

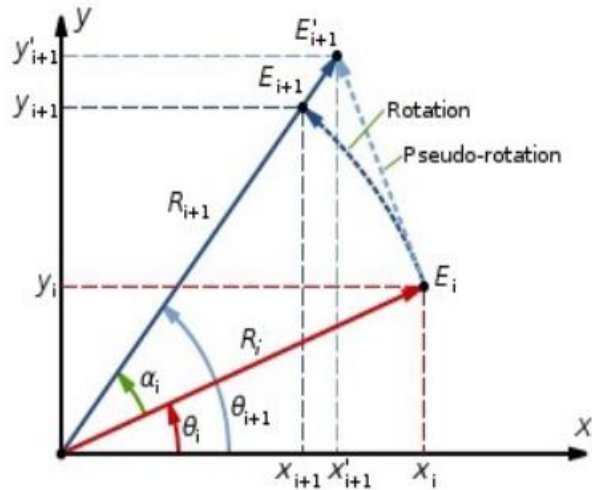
Coordinate Rotation Digital Computer (CORDIC) is a simple and efficient algorithm to compute arithmetic, trigonometric and hyperbolic functions. in many fields such as DSP, image processing, communication or in industrial sectors, researchers are using CORDIC algorithm to optimize design performance CORDIC was conceived in 1956 by Jack E. Volder thus it sometimes called as Volder's algorithm.

The CORDIC algorithm is one of the iterative methods to perform vector rotations for arbitrary angles using shifts and adds. Planar rotation for any vector A of (Xj, Yj) can be defined in matrix form as:

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X_j \\ Y_j \end{bmatrix}$$

With a small rearrangement, the stepwise rotation is performed by:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -\tan \theta_n \\ \tan \theta_n & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}$$

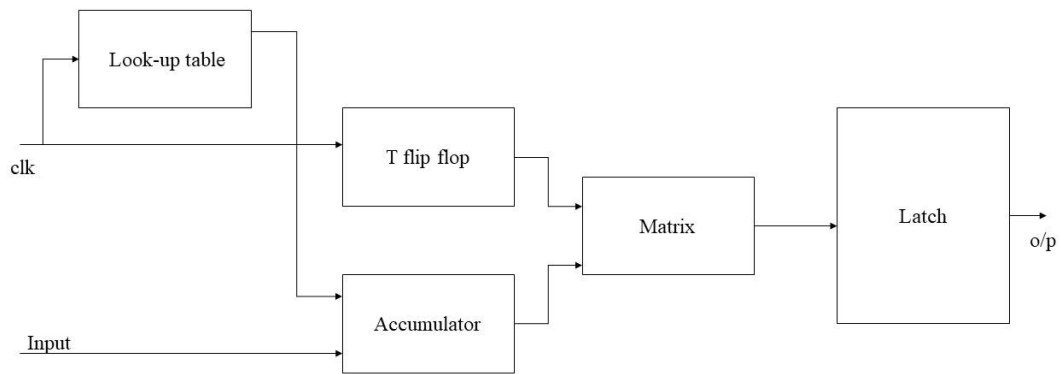


Fig, Cordic angle rotation

2.2 Interfaces

Signal Name	I/O	Description
Rst	IN	ACTIVE HIGH Reset
Clk	IN	Positive edge clock
target [7:0]	IN	Angle in radians
cos [7:0]	OUTPUT	Cosine
sin [7:0]	OUTPUT	Sine

2.3 Architecture



2.4 Detailed functional description

- Look-up table is used to compare the value of arc tan angle.
- Accumulator is used to store the value of angle after each iteration.
- Matrix is used to rotate the angle according to either positive or negative direction.
- Latch is used to give the final output values.

3 Design parameters

3.1 Performance Requirements

- Clock frequency of 100MHz.
- If possible, the accuracy should be within 1 percent.
- No slack or no Setup and hold violations.
 - Processor should be of 8 bit.

3.2 Clock Distribution

In the design the single clock is taken. Flip flops in design are positive edge triggered and having reset.

Clock Name	Frequency
Clk	100 MHz
Duty Ratio	0.5

3.3 Reset

Reset is active high. With response from the counter the reset enables HIGH. All the outputs will be forced to zero during reset.

4 Verification Strategy

4.1 Objectives

The design contains LUT and a accumulator. So, first we have test the LUT with different inputs and then, further test it with the accumulator block which will give the final result.

4.2 Tools and Version

Icarus Verilog and Xilinx Vivado is used for simulation of RTL and dumping the output in file. GTKWAVE is used for the generating the waveforms.

The RTL to GDS Flow:

The model is synthesized and netlist is generated using cadence genus and then the layout is done using cadence innovus.

4.3 Checking mechanisms

The following checking mechanism is used for verifying the model:

- Test bench is made for checking the functionality of the Cordic processor.
- Timing analysis and clock analysis is done in cadence environment.

- Layout verification is done in cadence innovus.

4.5 Functional Checklist

- Verification of Accumulator unit for Cordic processor.
- Time slack should be within required limit
- .

5 Testbench

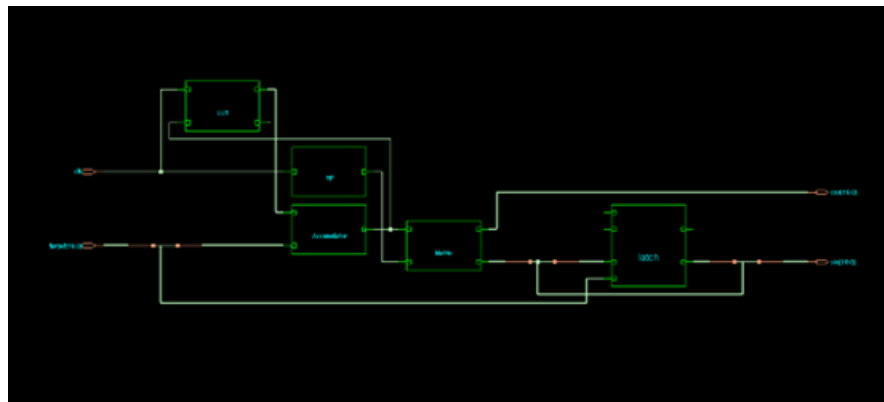
5.1 Overview

In test bench, we have design under test(DUT), we have given inputs and clock in the test bench. I have used dump file(tb.vcd) and dump Vars(0,tb) for generating waveform in GTK Wave.

6 Tests Specification

N/A

7 Design Microarchitecture



7.1 Top Level Interface

Described in the interface section 2.

7.2 Sub-Block Description

1. Look-Up Table

Counter	Angle (if direction =1)	Angle (if Direction=0)
2	45 or 0.785398163	-45 or -0.785398163
4	26.56 or 0.463647609	-26.56 or -0.463647609
6	14.0362 or 0.244978663	-14.0362 or -0.244978663
8	7.1250 or 0.124354994	-7.1250 or -0.124354994
10	3.5763 or 0.06241881	-3.5763 or -0.06241881
12	1.7899 or 0.031239833	-1.7899 or -0.031239833
14	0.8951 or 0.015623728	-0.8951 or -0.015623728
16	0.4476 or 0.00781234106	-0.4476 or -0.00781234106
18	0.2238 or 0.003906230132	-0.2238 or -0.003906230132
20	0.1119 or 0.001953122516	-0.1119 or -0.001953122516
22	0.0559 or 0.0009765621896	-0.0559 or -0.0009765621896
24	0.0279 or 0.0004882812112	-0.0279 or -0.0004882812112
26	0.0139 or 0.0002441406201	-0.0139 or -0.0002441406201
28	0.0069 or 0.0001220703119	-0.0069 or -0.0001220703119
30	0.00349 or 0.00006103515617	-0.00349 or -0.00006103515617
32	0.00174 or 0.00003051757812	-0.00174 or -0.00003051757812

7.3 Structural Mapping Process

For the conversion of gate-level netlist from RTL we have used genus tool.

Proof that RTL and netlist correspond.

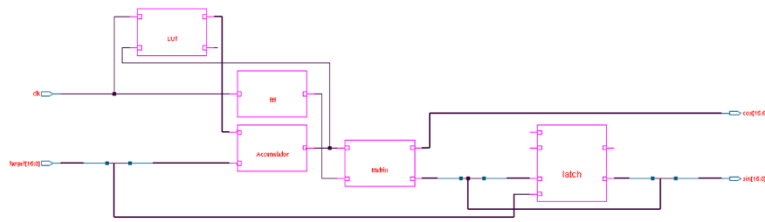


Fig. Cordic Schematic

8 Physical hierarchy

8.1 Floor planning

Floor Planning design dimension:

Aspect Ratio	1.0
Core Utilization	0.70
Core to die boundary(left)	4.5
Core to die boundary(right)	4.5
Core to die boundary(top)	4.5
Core to die boundary(bottom)	4.5

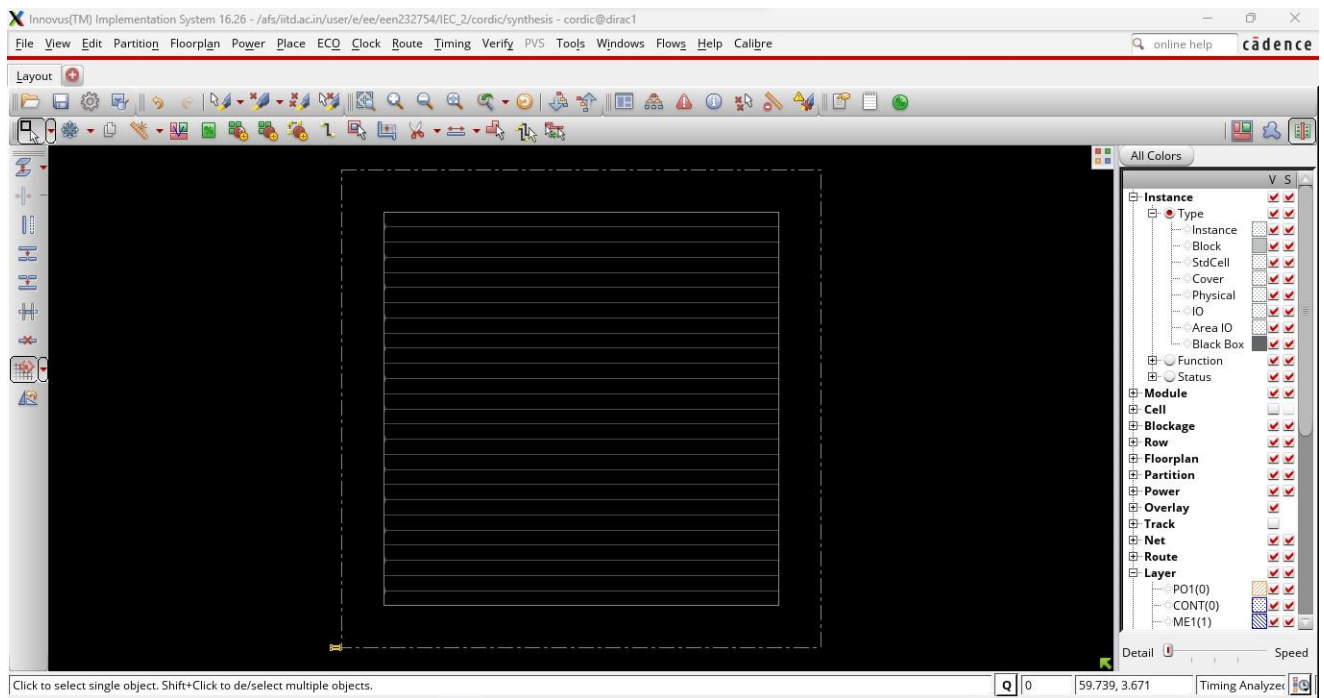


Fig. Floor Planning

8.2 Clock tree insertion

8.3 Layout Strategy

- **Floorplanning**

Aspect Ratio	1.0
Core Utilization	0.7
Core to die boundary(left)	4.5
Core to die boundary(right)	4.5
Core to die boundary(top)	4.5
Core to die boundary(bottom)	4.5

- **Power Planning**

Ring Configuration

	Layer	Width	Spacing
Top	ME8	0.7	0.985
Bottom	ME8	0.7	0.985
Left	ME7	0.7	0.985
Right	ME7	0.7	0.985

Stripes Configuration

Layer	ME 6(Vertical)
Width	0.3
Spacing	0.4
Set-to-Distance	2.5

Routing:

Top Layer	Metal 8
Bottom Layer	Metal 1

Nano Route: SI Driven
 Timing driven

Metal Count:

Metal	Count
Metal 1	1761
Metal 2	1128
Metal 3	276
Metal 4	8
Total	3173

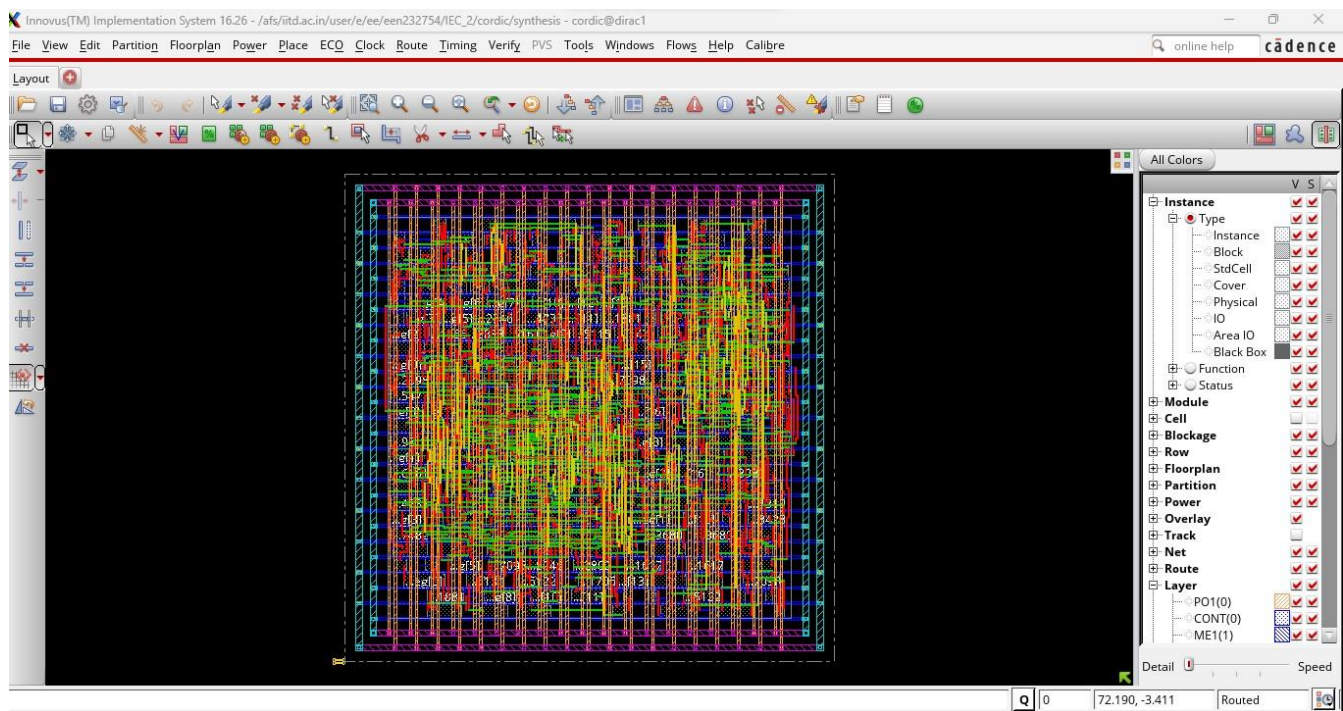
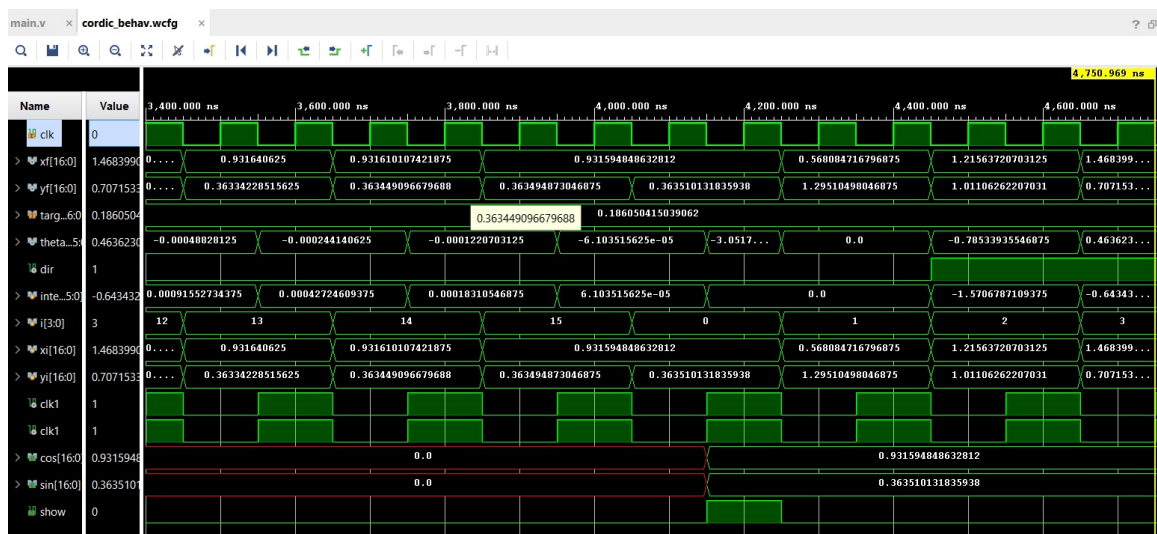


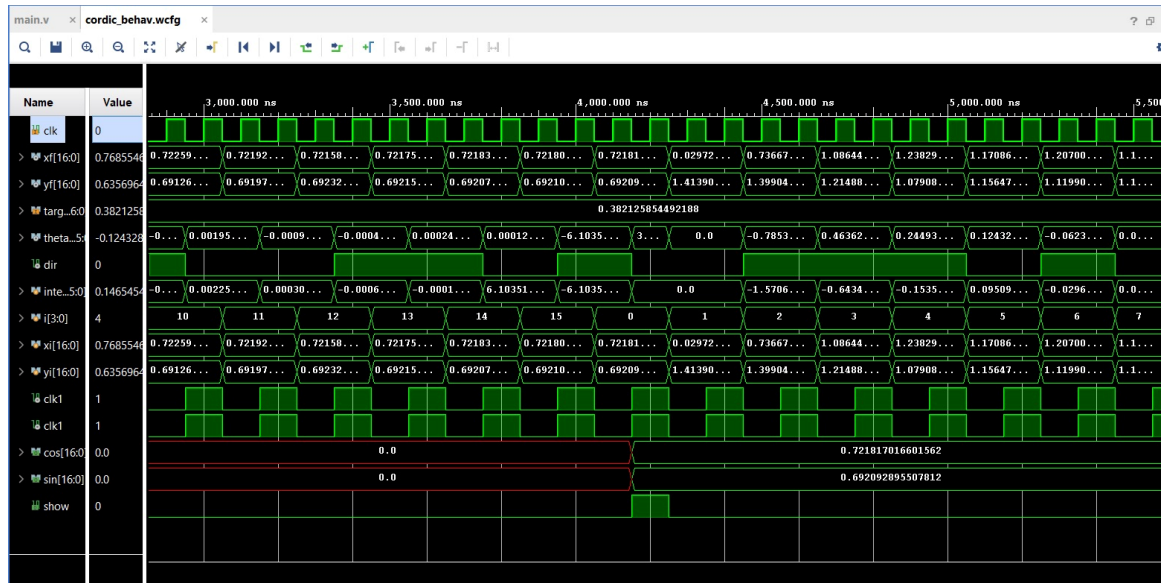
Fig. Layout after nano route

9 Results

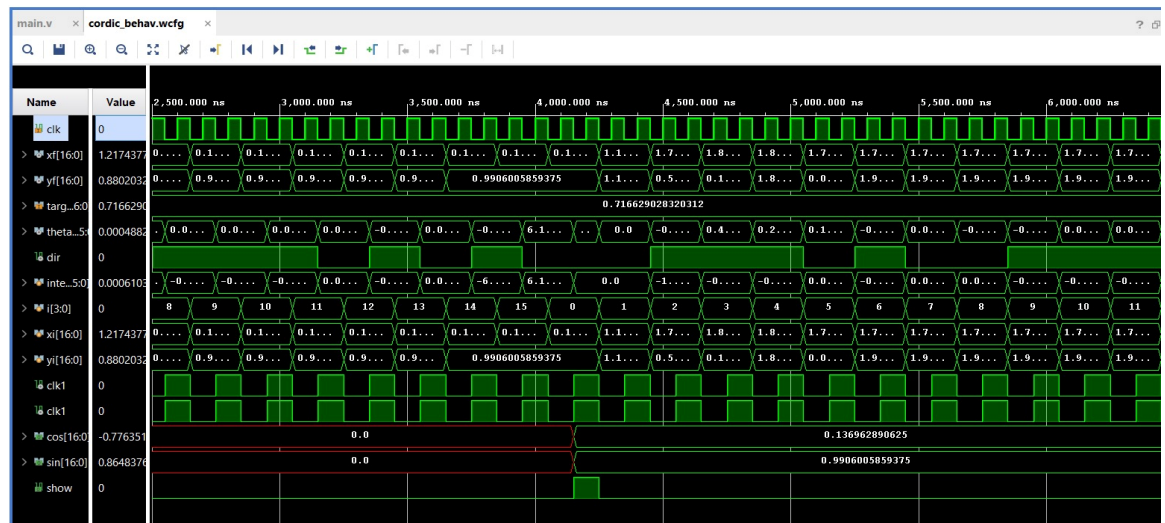
- 21.32 Degree



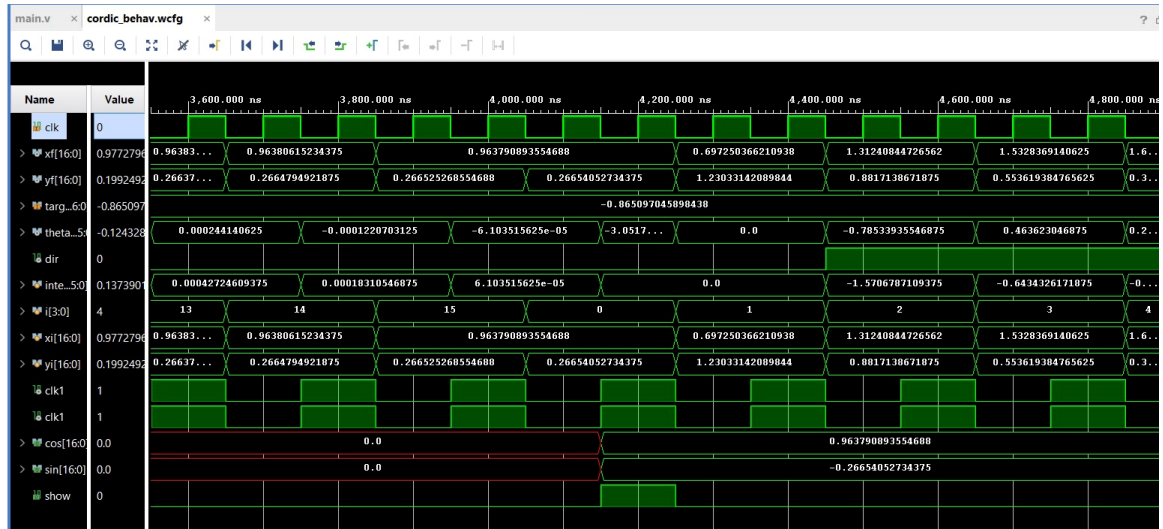
- 43.79 Degree



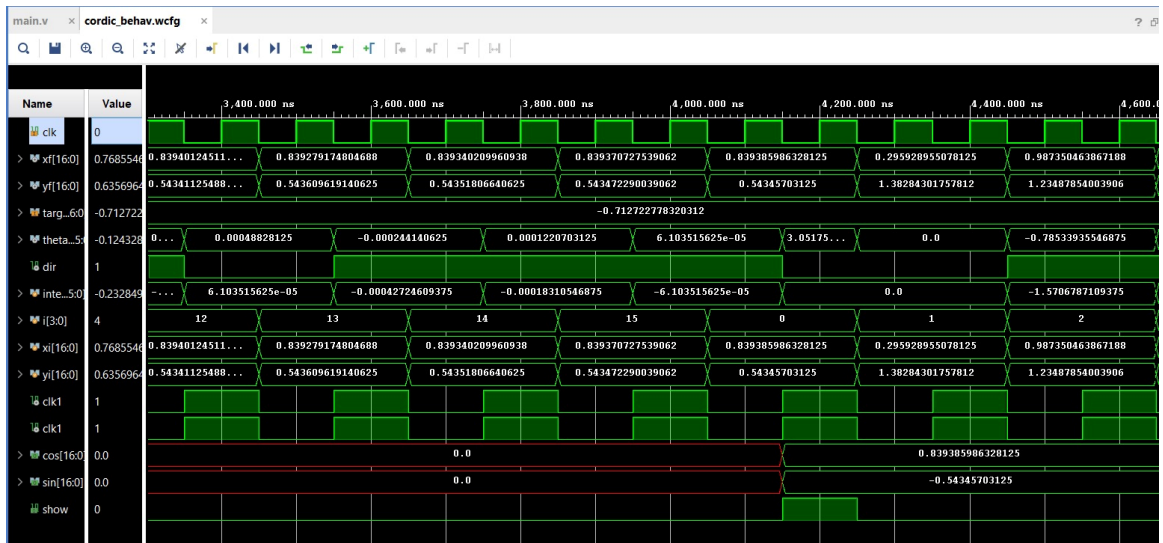
- 82.12 Degree



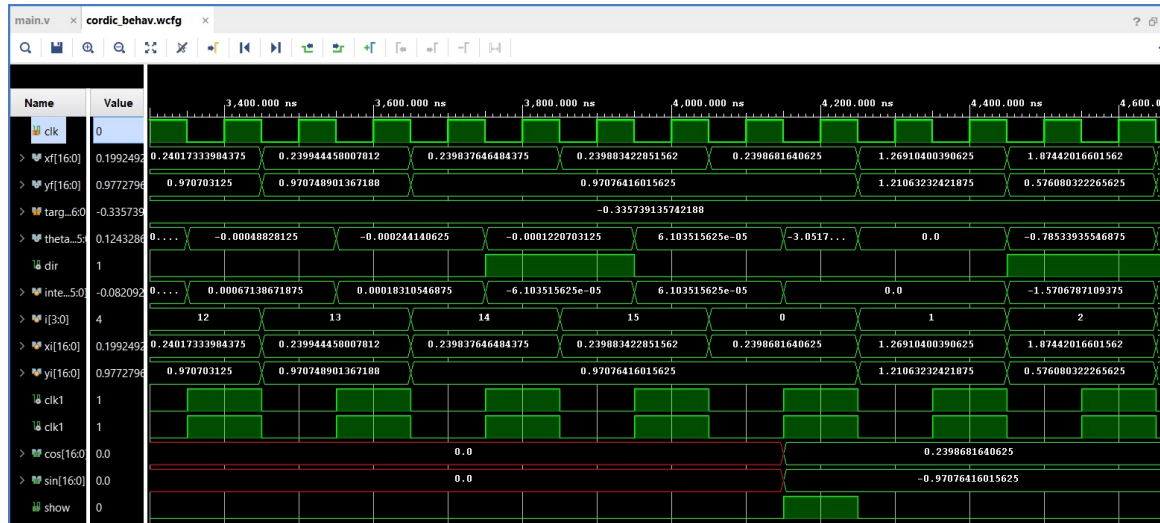
- -15.46 Degree



- -32.92 Degree



- -76.12 Degree



Angle (in Degrees)	Cordic processor output	
	cos	sin
21.32	0.931594	0.363510
43.79	0.721817	0.692092
82.12	0.136962	0.990600
-15.46	0.963790	-0.266540
-32.92	0.839385	-0.543457
-76.12	0.239868	-0.970764

9.1 Area

Block Name	Inst	Area (um ²)
Cordic	452	1553.04
m1	243	962.28
l1	111	307.08
a1	32	137.52
tf1	1	7.56
l11	64	136.44

10.2 Timing

Pre- CTS Analysis:

Setup Time:

```

End delay calculation. (MEM=2167.89 CPU=0:00:00.6 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:01.0 real=0:00:01.0 totSessionCpu=0:08:15 mem=2167.9M)

-----
timeDesign Summary
-----

Setup views included:
worst_case

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns):  | 3.921 | 3.921 | 7.411 |
| TNS (ns):  | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1275 | 732 | 684 |
+-----+-----+-----+

+-----+-----+-----+
|          | Real | Total |
+-----+-----+-----+
| DRV's    | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap  | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 70.606%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 1.51 sec
Total Real time: 2.0 sec
Total Memory Usage: 2108.660156 Mbytes
innovus 11>

```

Hold Time:

```

# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
AAE_INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
*** Calculating scaling factor for min timing libraries using the default operating c
**WARN: (IMPESI-3014): The RC network is incomplete for net target[16]. As a result,
se timing accuracy. To resolve this, check parasitics for completeness, re-extraction
Total number of fetched objects 586
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2167.89 CPU=0:00:00.4 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.8 real=0:00:01.0 totSessionCpu=0:08:28 me

-----
timeDesign Summary
-----

Hold views included:
best_case

+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 0.078 | 0.078 | 0.000 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 732 | 732 | 0 |
+-----+-----+-----+

Density: 70.606%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 1.28 sec
Total Real time: 1.0 sec
Total Memory Usage: 2090.511719 Mbytes
innovus 11>

```

Post- CTS Analysis: Setup Time

```
3. een232754@dirac.vlsi.ee.iitd.ac.in
Terminal Sessions View X_server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick co 3. een232754@dirac.vlsi.ee.iitd.ac.in X +
End delay calculation. (MEM=2167.89 CPU=0:00:00.4 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:01.1 real=0:00:01.0 totSessionCpu=0:08:37 mem=2167.9M)
-----
timeDesign Summary
-----
Setup views included:
worst_case
-----
+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 3.921 | 3.921 | 7.411 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1275 | 732 | 684 |
+-----+-----+-----+-----+
+-----+-----+-----+-----+
| DRV | Real | Total |
|-----|-----|-----|
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+
Density: 70.606%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 1.8 sec
Total Real time: 2.0 sec
Total Memory Usage: 2108.660156 Mbytes
innovus 11>
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
```

Hold Time

```
3. een232754@dirac.vlsi.ee.iitd.ac.in
Terminal Sessions View X_server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick co 3. een232754@dirac.vlsi.ee.iitd.ac.in X +
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
*** Calculating scaling factor for min_timing libraries using the default operating condition of each library.
**WARN: (IMPESI-3014): The RC network is incomplete for net target[16]. As a result, a lumped model will be used du
se timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
Total number of fetched objects 586
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2167.89 CPU=0:00:00.2 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.7 real=0:00:00.0 totSessionCpu=0:08:45 mem=2167.9M)
-----
timeDesign Summary
-----
Hold views included:
best_case
-----
+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.078 | 0.078 | 0.000 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 732 | 732 | 0 |
+-----+-----+-----+-----+
Density: 70.606%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 1.23 sec
Total Real time: 2.0 sec
Total Memory Usage: 2090.511719 Mbytes
innovus 11>
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
```


Timing	Pre-CTS	Post-CTS
Set-up	3.921	3.921
Hold	0.078	0.078

10.3 Power Report

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick co 3. een232754@dirac.vlsi.ee.iitd.ac.in

Total Power						
Total Internal Power:	0.02562405	55.3670%				
Total Switching Power:	0.02040504	44.0900%				
Total Leakage Power:	0.00025129	0.5430%				
Total Power:	0.04628039					

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.01047	0.003851	8.278e-05	0.0144	31.11
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.01516	0.01655	0.0001685	0.03188	68.89
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.02562	0.02041	0.0002513	0.04628	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.02562	0.02041	0.0002513	0.04628	100

Power Distribution Summary:

- Highest Average Power: l1/counter_reg[1] (DFCM1RA): 0.0007438
- Highest Leakage Power: a1/add_96_21/g1587__2398 (XOR3M2RA): 2.023e-06
- Total Cap: 2.18534e-12 F
- Total instances in design: 452
- Total instances in design with no power: 0
- Total instances in design with no activity: 0

10.4 DRC rule violations

No DRC violations are found.

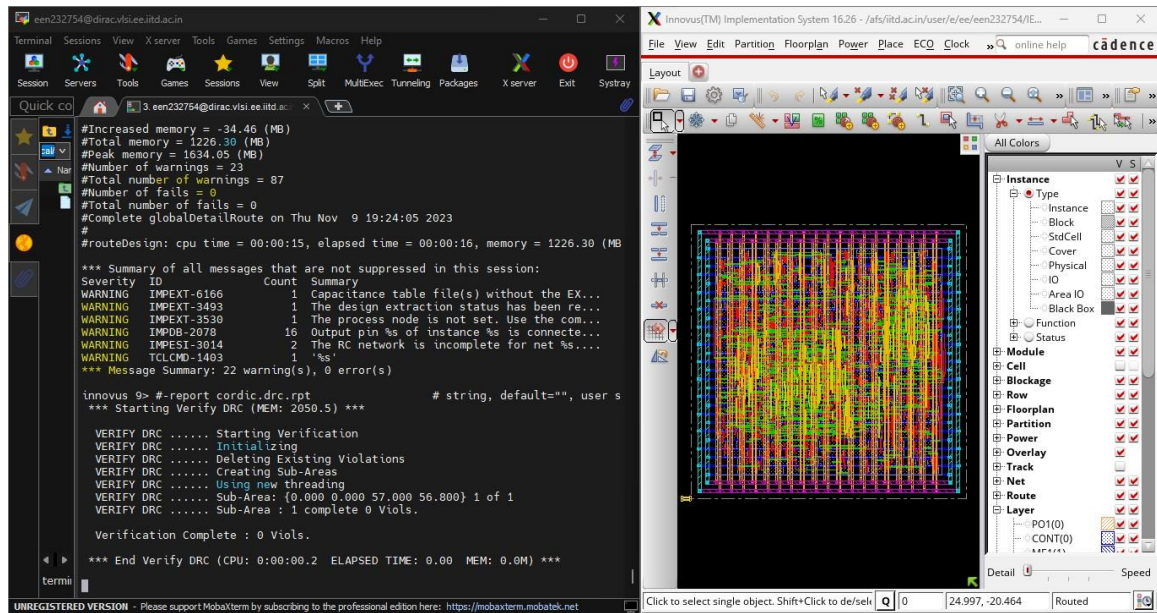


Fig. No DRC violations

11 Bugs known at submission date

N/A