VERIPOINT™

SdCvP-X™

Specification Driven Comprehensive Verification Acceleration AI Tool

Verification Challenges - Business Impact

- **Research** : Siemens EDA/Wilson Research Group 2024 Functional Verification Study/DVCon
  - First-Time Silicon success dropped to **14% in 2024**
  - **75%** of Design Projects are **behind SCHEDULE** !!
- **Industry Surveys** (e.g., Wilson Research, Accellera): Verification consumes **60-70%** of total design effort

Challenges	Business Impact
Increasing Design Complexity	Longer cycles, higher risk, strained resources
Manual Verification Planning	Inefficiency and higher costs
Unstructured Debug & Root Cause Analysis	Delays and risk of re-spins
Lack of Traceability to Specifications	Coverage gaps, missed bugs
Inconsistent Verification Reuse	Rework, cost overruns, delays

Introducing SdCvP-X™ - Solving Verification at Once

Verification Challenge	SdCvP-X™ Tool
Manual, fragmented planning	Auto-generated, spec-aligned comprehensive segregated verification plans for IP/SOC/ASIC
Specification alignment	Plan evolves with specification + version traceability
Manual Plan Alignment with Specification and upgrades	Aligns manual plans to eliminate gaps and ensure consistency and boost productivity.
Debug inefficiencies	Traceability matrix + mapping to features/test points
Configuration explosion	Smart filtering, collapsing, and prioritization
Reuse across derivatives	Scalable planning across standard & custom designs

Who Benefits – Across the Project Hierarchy

Role	Pain Point	SdCvP-X™ Benefit
Design Verification Engineers	Long debug cycles, manual test list creation	Faster test planning + structured debug : Boost Productivity
Architects	Hard to validate spec implementation	Full traceability from spec to test
Program/Project Managers	Poor visibility on verification progress	Actionable insights, milestone-based views
Business Leaders & Industries	Risk of re-spin, time-to-market delays	Higher First Silicon Success, faster TTM

SdCvP-X™ - Tool Highlights

Features	Description
Auto Verification Plan Generator	Features, test points, scenarios by config
Auto Constraints, Coverage and Assertion	Constraints, Coverage and Assertion planning
Debug Assist Engine	Traceability matrix, root-cause accelerators
Specification Evolver	Adapts plans as spec updates
Smart Manual Plan Alignment	Aligns manual plans to eliminate gaps and ensure consistency and boost productivity.

SdCvP-X™ - Tiered Product Options

Standard	Advanced	Premium	Premium+
Comprehensive Verification Plan **Features, Test Points, Test Scenarios and Configurations** Per Design Specification	Standard Features **Constraints and Assertions** Per Design Specification	Advanced Features **Coverage and Mapping Specification Variables (Debugging)** Per Design Specification	Premium Features Alignment of existing manual plan *Traceability Matrix - Efficient Debugging *Enhance Verification plan with Specification evolution *Automatically Generated Verification Test Bench and Sequences

SdCvP-X™ Statistics Highlights

PCIe 6.2 IP Verification

- In **~2 Hours**
  - SdCvP-X™ generated comprehensive, configurable verification plan having 4000+ Rows with constraints, coverage, and assertions.

CXL 3.0 IP Verification

- In **~1 hour**
  - SdCvP-X™ generated comprehensive, configurable verification plan having 2000+ Rows with constraints, coverage, and assertions.

ARM Cortex -A Series Version: 4.0 (Open Source)

- In **~1 hour**
  - SdCvP-X™ generated comprehensive, configurable verification plan having 700+ Rows with constraints, coverage, and assertions.

Custom RISC SOC Verification (Version 20250508: Open Source)

- In **~1 hour**
  - SdCvP-X™ generated comprehensive, configurable verification plan having 800+ Rows with constraints, coverage, and assertions.

Custom PIPE Interface (Version 7.0: Intel Open Source - PCIe, SATA, USB3.x, USB4.x, DP2.x)

- In **~1 hour**
  - SdCvP-X™ generated comprehensive, configurable verification plan having 1200+ Rows with constraints, coverage, and assertions.

Design Verification Success at a Glance

Metric	Before SdCvP-X™	After SdCvP-X™
Verification effort	100% (baseline)	↓ 40% reduction
Debug cycle time	4–6 weeks or more	↓ 50% reduction
Time to First Silicon	Slipping	On-time or early
Manual planning effort	Extensive	Near-zero with automation

SdCvP-X™: Accelerate Verification, Design Success

- Start with a free demo
- Identify 1–2 designs and see the impact in <1 week
- Scale across IPs, ASICs, SoCs and Custom Interfaces
- Seamless integration in existing verification workflow

Request For Demo

Thank You!

VERIPOINT™

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