SdCvP-X™

Specification Driven Comprehensive Verification Acceleration AI Tool

Verification Challenges - Business Impact

- **Research** : Siemens EDA/Wilson Research Group 2024 Functional Verification Study/DVCon
  - First-Time Silicon success dropped to **14% in 2024**

  - **75%** of Design Projects are **behind SCHEDULE** !!

- **Industry Surveys** (e.g., Wilson Research, Accellera): Verification consumes **60-70%** of total design effort

Challenges	Business Impact
Increasing Design Complexity	Longer cycles, higher risk, strained resources
Manual Verification Planning	Inefficiency and higher costs
Unstructured Debug & Root Cause Analysis	Delays and risk of re-spins
Lack of Traceability to Specifications	Coverage gaps, missed bugs
Inconsistent Verification Reuse	Rework, cost overruns, delays

Introducing SdCvP-X™ - Solving Verification at Once

Verification Challenge	SdCvP-X™ Tool
Manual, fragmented planning	Auto-generated, spec-aligned comprehensive segregated verification plans for IP/SOC/ASIC
Specification alignment	Plan evolves with specification + version traceability
Manual Plan Alignment with Specification and upgrades	Aligns manual plans to eliminate gaps and ensure consistency and boost productivity.
Debug inefficiencies	Traceability matrix + mapping to features/test points
Configuration explosion	Smart filtering, collapsing, and prioritization
Reuse across derivatives	Scalable planning across standard & custom designs

Who Benefits – Across the Project Hierarchy

Role	Pain Point	SdCvP-X™ Benefit
Design Verification Engineers	Long debug cycles, manual test list creation	Faster test planning + structured debug : Boost Productivity
Architects	Hard to validate spec implementation	Full traceability from spec to test
Program/Project Managers	Poor visibility on verification progress	Actionable insights, milestone-based views
Business Leaders & Industries	Risk of re-spin, time-to-market delays	Higher First Silicon Success, faster TTM

SdCvP-X™ - Tool Highlights

Features	Description
Auto Verification Plan Generator	Features, test points, scenarios by config
Auto Constraints, Coverage and Assertion	Constraints, Coverage and Assertion planning
Debug Assist Engine	Traceability matrix, root-cause accelerators
Specification Evolver	Adapts plans as spec updates
Smart Manual Plan Alignment	Aligns manual plans to eliminate gaps and ensure consistency and boost productivity.

SdCvP-X™ - Tiered Product Options

VERIPOINT™

Standard

- ✓ Comprehensive Verification Plan
- ✓ Features, Test Points & Scenarios
- ✓ Configuration Management
- ✓ Specification Alignment

Advanced

- ✓ All Standard Features
- ✓ Constraints and Assertions
- ✓ Enhanced Specification Evolution
- ✓ Advanced Traceability Matrix

Most Popular

Premium

- ✓ All Advanced Features
- ✓ Coverage and Mapping
- ✓ Specification Variables Debugging
- ✓ Priority Support

Premium+

- ✓ All Premium Features
- ✓ Auto-Generated Test Bench
- ✓ Custom Integration Support
- ✓ Dedicated Success Manager

SdCvP-X™ Statistics Highlights

VERIPOINT™

PCIe 6.2 IP ★★★★★

Generation Time:	~2 Hours
Verification Plan:	4000+ Rows
Industry:	Data Center

Complete verification plan with constraints, coverage, and assertions for high-speed PCIe 6.2 protocol

CXL 3.0 IP ★★★★★

Generation Time:	~1 Hour
Verification Plan:	2000+ Rows
Industry:	Memory & Storage

Comprehensive verification framework for next-generation memory coherence interfaces

ARM Cortex-A Series ★★★★★

Generation Time:	~1 Hour
Verification Plan:	700+ Rows
Industry:	Mobile & Embedded

Open source processor verification with comprehensive coverage analysis for ARM architecture

Custom RISC SoC ★★★★★

Generation Time:	~1 Hour
Verification Plan:	800+ Rows
Industry:	IoT & Edge Computing

Custom SoC verification with comprehensive coverage for RISC-V based system-on-chip designs

Custom PIPE Interface ★★★★★

Generation Time:	~1 Hour
Verification Plan:	1200+ Rows
Industry:	Multi-Protocol

Intel PIPE 7.0 interface covering PCIe, SATA, USB3.x, USB4.x, and DisplayPort 2.x protocols

Universal Coverage

5+	12K+
Verified IPs	Total Rows

From IP to ASIC to SOC to FPGA and more - proven across all semiconductor verticals

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Design Verification Success at a Glance

Metric	Before SdCvP-X™	After SdCvP-X™
Verification effort	100% (baseline)	↓ 40% reduction
Debug cycle time	4–6 weeks or more	↓ 50% reduction
Time to First Silicon	Slipping	On-time or early
Manual planning effort	Extensive	Near-zero with automation

SdCvP-X: Accelerate Verification, Design Success

- Start with a free demo

- Identify 1–2 designs and see the impact in <1 week

- Scale across IPs, ASICs, SoCs and Custom Interfaces

- Seamless integration in existing verification workflow

Request For Demo

Thank You!

Contact Us

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