Abhinandana N Howle

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Summary

Motivated and technically adept Electronics and Communication Engineering currently in final year with strong foundations in , VLSI, digital communication,RISC-V,Antenna design and programming. Passionate about RTL design,and system verification. Looking for research opportunities to apply and grow my skills with the aim to contribute to leading firms in roles involving software engineering, infrastructure systems, or application development.

Education

PES University, Bangalore *2022 – 2026*
B.Tech in Electronics and Communication Engineering
Current CGPA: 7.7(till 6th sem)

Sri Siddaganga Independent Science PU College, Davanagere *2020 – 2022*
Intermediate (PCMB)
Percentage: 92.3%

Sri Siddaganga Composite High School, Davanagere *2019 – 2020*
10th Grade
Percentage: 96.8%

Projects

- **Pentaband Antenna Design for Sub-6GHz Applications (Ongoing)**
  Designing a compact microstrip patch antenna with 5 frequency bands, optimized for gain $>$ 6 dBi and high isolation. Simulated and tuned using **CST Studio Suite**. Focus on multiband integration, port decoupling, and performance enhancement for 5G IoT and wireless applications.
- **4-Bit Serial Multiplier**: Designed using SystemVerilog and simulated in Quartus Prime.
- **Priority Encoder with Layered Testbench**: Created and verified using EDA Playground.
  Link: edaplayground.com/x/UbGf
- **Single-Cycle RISC-V Processor**: Implemented all 5 stages with RTL and verified in Quartus Prime.
  GitHub: github.com/abhinan-ux/COD-Lab

Skills

Languages: SystemVerilog, C, C++, Python (basics).
Assembly: RISC-V.
Tools: CST Studio Suite, Quartus Prime, Cadence Virtuoso, MATLAB, Wireshark.
Domains:Antenna Design, RTL Implementation,Digital VLSI,High Performance Computing,Computer Organisation and Design,Formal Verification.

Certifications

- C++ Course - W3Schools C++ Certification