Design and Verification of RAM and ROM using Verilog HDL

Introduction

Memory plays a vital role in digital design and VLSI systems.

- **RAM (Random Access Memory):** Volatile memory used for temporary data storage. Both read and write operations are supported.
- **ROM (Read Only Memory):** Non-volatile memory with fixed data, used for look-up tables, firmware, etc.

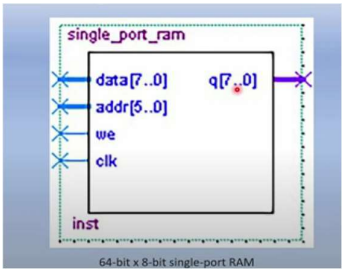
Objectives

- To design Single-Port RAM and ROM in Verilog HDL.
- To implement testbenches for both memory modules.
- To perform functional verification using EDA Playground and EPWave.
- To analyze read and write behavior of RAM and ROM.

Tools and Technologies Used

- HDL Language**:** Verilog
- Simulation Platform: EDA Playground
- Waveform Viewer: EPWave
- Verification Method: Testbench-based simulation.

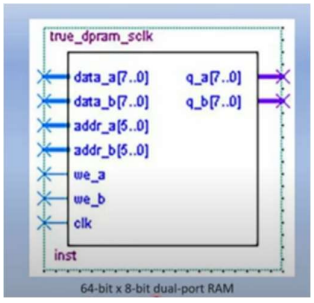
SINGLE PORT RAM Design:



https://www.edaplayground.com/x/WiTV -EDA Playground link

https://www.edaplayground.com/launchEpwave -EP wave link in EDA Playground

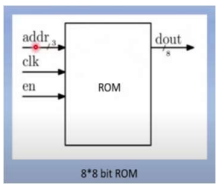
DUAL PORT RAM DESIGN:



https://www.edaplayground.com/x/nS88 - EDA Playground link

https://www.edaplayground.com/launchEpwave - EP Wave link in EDA Playground

ROM DESIGN:



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