Design and implementation of Half Adder Using Transmission gates

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Abstract

An adder is a digital circuit that performs addition of two binary numbers. Basically, adders are the part of Arithmetic logic unit (ALU), which is the processing part of a CPU. Adders are used, not only in ALU, but also in other parts of processors to calculate addresses, increment, decrement operators and many other similar operations. The main concern is to build half adder which is power efficient, energy efficient and uses less number of transistors. The proposed work shows implementation of Half Adder using Transmission gates.

1. Reference circuit Details

Half adder accepts two binary inputs namely A and B and produces the output Sum and Carry. The four possible combinations of two binary digits A and B are ,when A is 0 and B is 0 the Sum and Carry output are 0 respectively. When A is 0 and B is 1 the Sum output is 1, as there is no Carry hence Carry output is 0. When A is 1 and B is 0 we get the same output as of case 2 i.e., Sum =1 and Carry =0. when A is 1 and B is 1, the Sum output is 0 whereas the Carry output is 1.

Half adder can be easily implemented with the help of the XOR Gate for the output 'SUM' and an AND Gate for the 'CARRY'.

These XOR and AND gates are implemented using CMOS transmission gates. CMOS transmission gates consists of one NMOS and one PMOS transistor, connected in parallel. The gate voltages applied to these NMOS and PMOS transistors are set to be complementary signals. As such, CMOS Transmission Gates(TG) operates as a bidirectional switch between the nodes A and B which is controlled by signal C.

In the reference circuit, half adder is implemented using transmission gate with two inverter circuits. Using CMOS TG logic, we can reduce the number transistors in the circuit implementation as compared to traditional CMOS half adder circuit.

2. Reference Circuit

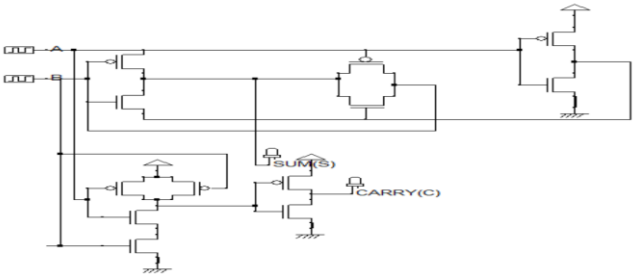

Fig 1: Half adder using transmission gate [1]

3. Reference Circuit Waveforms

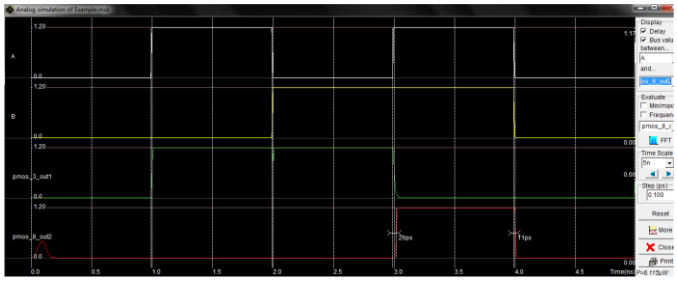

Fig 2: Simulation result of half adder using transmission gate [1]

References

[1] R. K. (2015). Design of area and power efficient half adder using Transmission Gate. International Journal of Research in Engineering and Technology, 04(04), 122–127. https://doi.org/10.15623/ijret.2015.0404021

[2] Balaji, G. N., V.A., & K.A. (2016). COMBINATIONAL CIRCUITS USING TRANSMISSION GATE LOGIC FOR POWER OPTIMIZATION. International Research Journal of Engineering and Technology (IRJET), 03(05). https://www.irjet.net