Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2020-21
Lab Sheet– 2 (23rd Feb. 2021)

Behavioral Modeling Style

In today's lab we shall implement a few sequential circuits which we have studied in digital design using dataflow modeling style and verify their functionality using a suitable test bench prepared using Behavioral Modeling.

Learning Outcome: By the end of this lab. session the learner will be able to

- Implement a sequential circuit design using behavioral modeling in Verilog HDL.
- List various constructs used in behavioral modeling and their function in Verilog HDL.
- Use the sensitivity list effectively for developing synchronous and asynchronous design.
- Write effective test cases for verifying a design in HDL.

Exercise Problems

1. Implement a D-flip flop with synchronous reset.
2. Convert the above flip-flop into asynchronous reset.
3. Implement a synchronous up/down counter (mod-10) using arithmetic operations. Assume positive edge triggered clock, active high synchronous reset signal which makes all the bits zero.
4. Implement a 2:4 decoder using a case statement.
5. Implement a 8-shift register Parallel in Serial Out (PISO). The shift register has a LOAD/SHIFT signal which will load when '1' and shift when '0'. Loading happens serially and shift is towards the right side one bit per clock cycle (positive edge).
6. Implement a BCD counter which counts from *00,01,02,….,59,00,01,02 ….*. The clock signal is a positive edge triggered, an active high synchronous reset signal is available to reset the counter. Note: You can't use the binary to BCD conversion logic here.

****** The End ******

-Prepared By
K. Babu Ravi Teja
Assistant Professor
EEE Department
BITS Pilani, Pilani Campus