Analog and Digital VLSI Design

Folded Cascode OPAMP

Analog Design Assignment

A PROJECT REPORT BY:

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EEE F313/ INSTRF313 – Analog & Digital VLSI Design

Under the Guidance of

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ACKNOWLEDGEMENTS

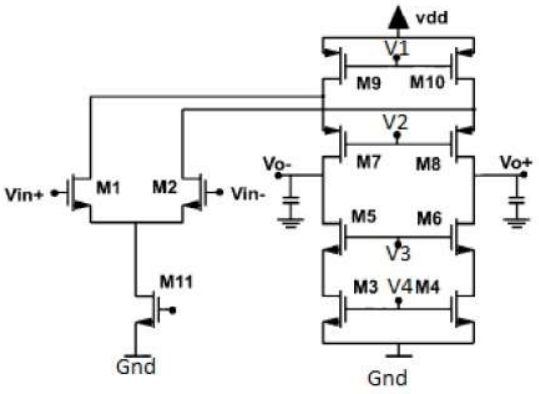
We would like to extend our gratitude to Dr Anu Gupta for giving us the opportunity to have hands on experience of amplifier design. Our theoretical concepts were put to practical use which was in itself an extremely satisfying job.

We would like to thank the team of teaching assistants for answering our queries and keeping demo sessions for LTSpice.

At last, we thank our parents and friends for moral support and encouragement.

PROBLEM 58

Ques 58. Design a folded Cascode OPAMP as shown in figure;



d) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
   iii) DC Gain ≥ 80dB
   iv) Power Dissipation ≤ 0.4mW
e) Show a biasing circuitry to bias all the voltages in your design (except the input).
f) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, ICMR plot, slew rate, Output voltage swing differential (dc + Transient), power consumption, and input and output offset voltage.

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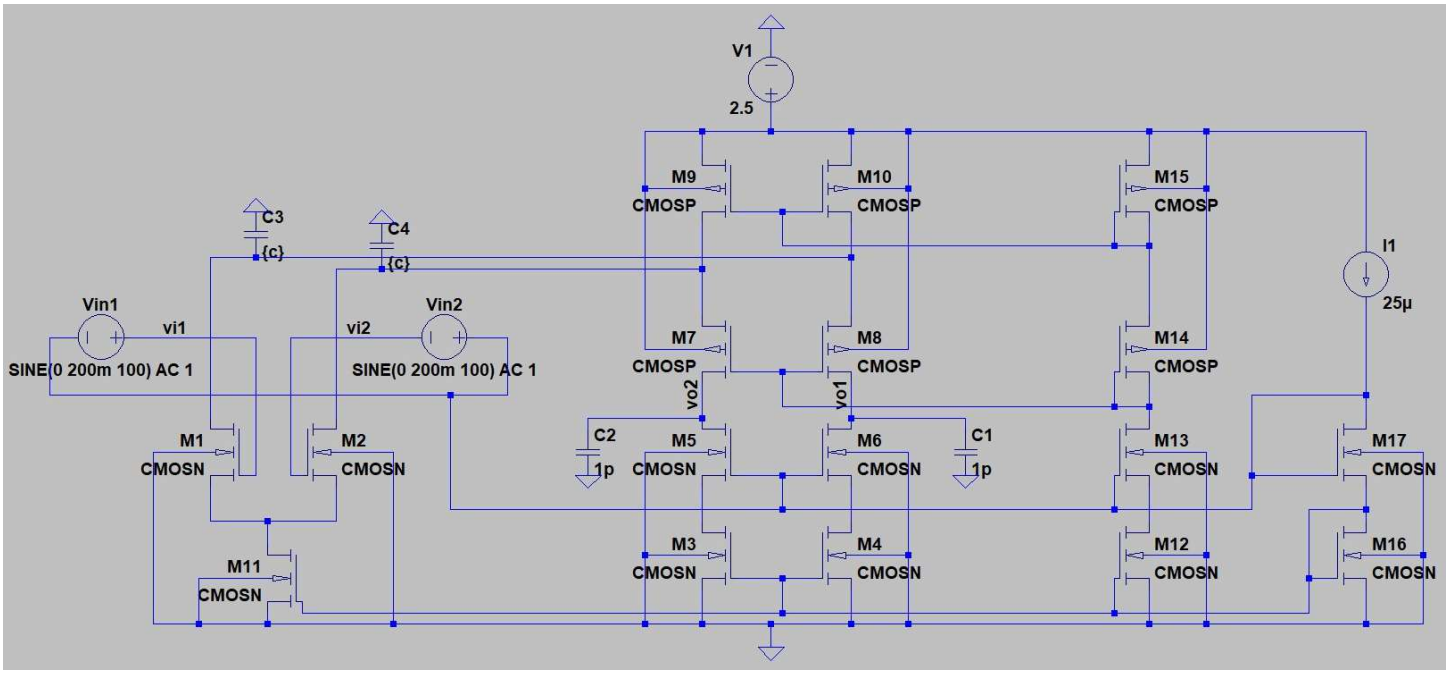
Additional requirements:

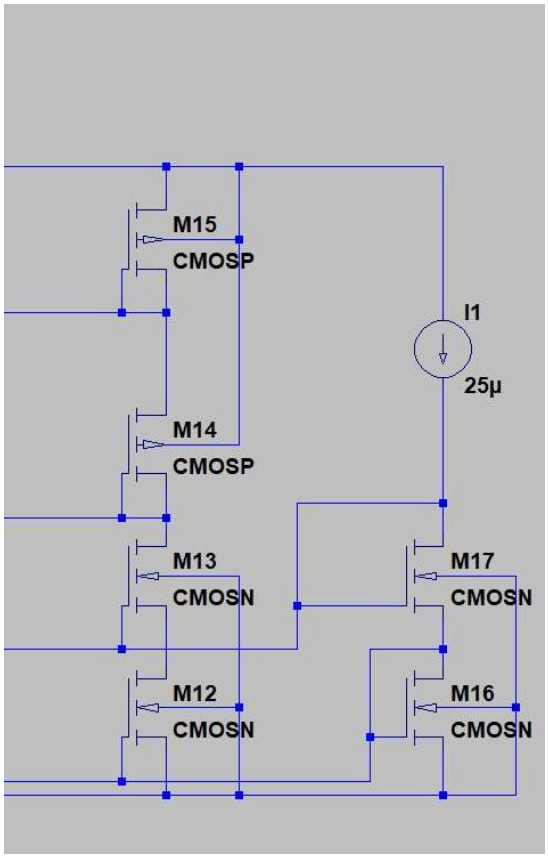
- You have to use **Cadence/ LTSPICE Schematic editor** to draw your circuit.
- For simulation you have to use **SPICE** simulators.
- Your design should **meet all the specifications**, at Schematic level.
- If you are not able to meet your specs, you can go ahead, but you need to explain why it has happened at the time of demonstration and in report.
- Validate your design for **all process corners** (SS, FF, TT) and temperatures 0, 27 and 100 ^{o}C.
- Min. channel length that can be used is 0.35um.
- 'Current sink' means that one of the nodes is connected to ground and 'current source' means that one of the nodes is connected to the supply.
- Your Design Should have only one ideal current Source/Sink .
- The suggested topologies are to be used unless there is a valid reason not to do the same.
- Make sure that all the transistors are working in saturation region.
- 'OTA' stands for Operational Transconductance Amplifier, which is basically an OPAMP with high output resistance.
- All OPAMPs/OTAs used feedback must be compensated for a phase margin of about 50^{o} to 60^{o}, unless your application requires it to be some other value.

*** Specifications and conclusions are towards the end

SCHEMATIC OF THE DESIGN



BIASING CIRCUITRY

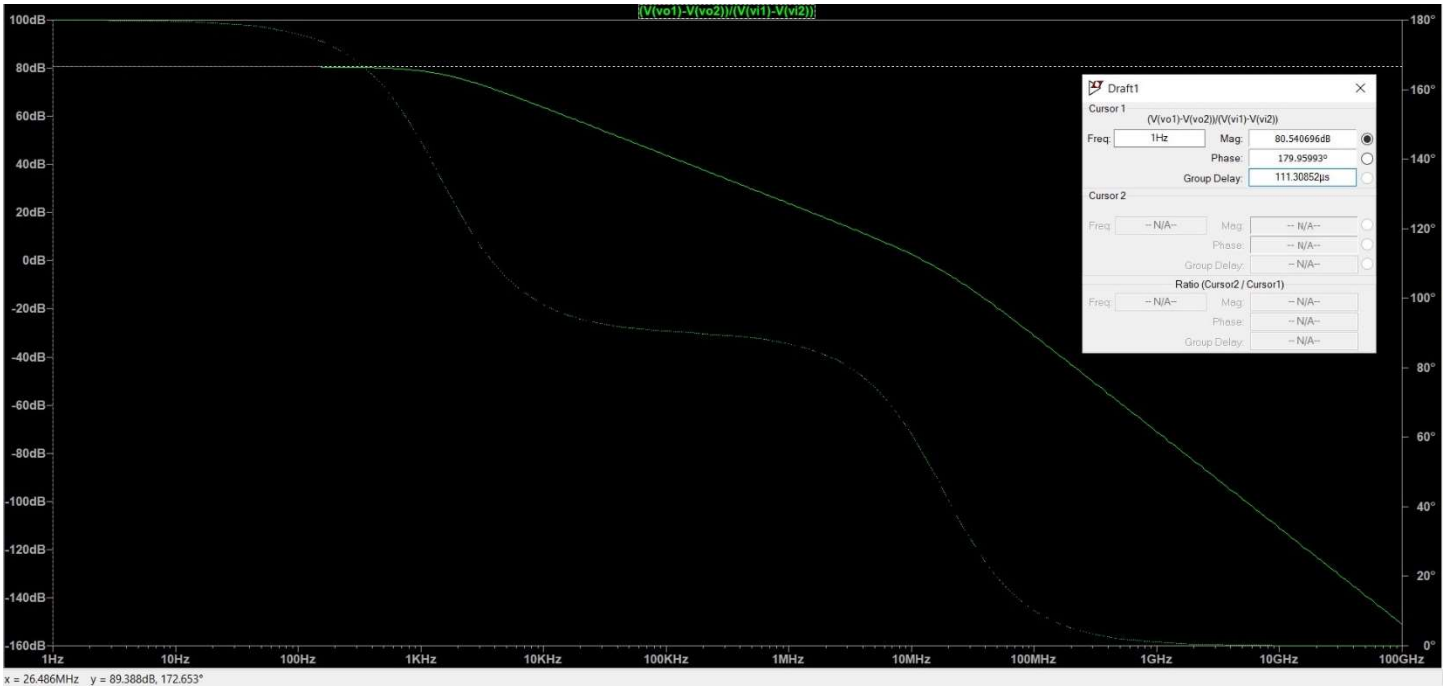


Dimensions of all the MOSFETs

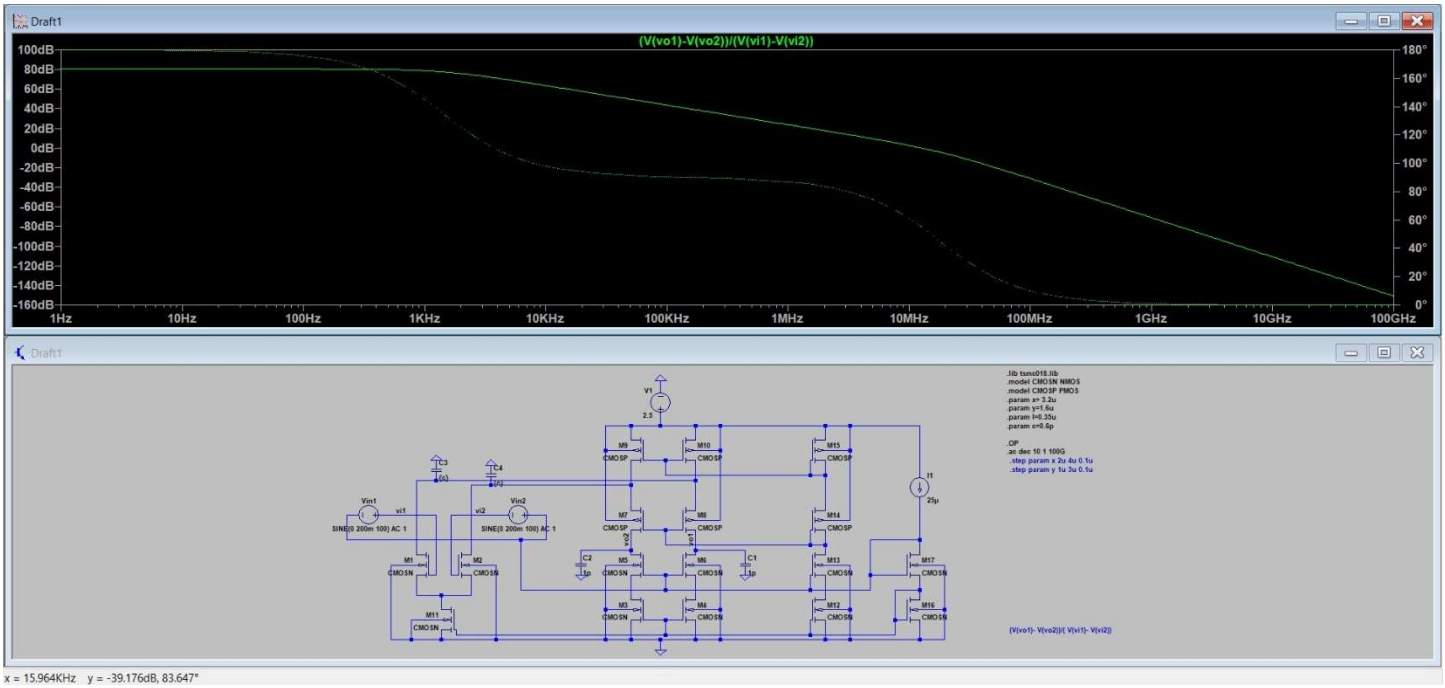
MOSFET Label	W	L	W/L
OPAMP			
M1	3.2 µm	0.35 µm	9.14
M2	3.2 µm	0.35 µm	9.14
M3	3.2 µm	0.35 µm	9.14
M4	3.2 µm	0.35 µm	9.14
M5	3.2 µm	0.35 µm	9.14
M6	3.2 µm	0.35 µm	9.14
M7	1.6 µm	0.35 µm	4.57
M8	1.6 µm	0.35 µm	4.57
M9	3.2 µm	0.35 µm	9.14
M10	3.2 µm	0.35 µm	9.14
M11	6.4 µm	0.35 µm	18.28
Biasing Circuitry			
M12	3.2 µm	0.35 µm	9.14
M13	3.2 µm	0.35 µm	9.14
M14	1.6 µm	0.35 µm	4.57
M15	1.6 µm	0.35 µm	4.57
M16	3.2 µm	0.35 µm	9.14
M17	3.2 µm	0.35 µm	9.14

1. DC Gain

For differential DC gain, we plot the bode plot and check the gain value at a frequency very close to zero (here, 1Hz). So, the DC Gain is 80.54 dB.

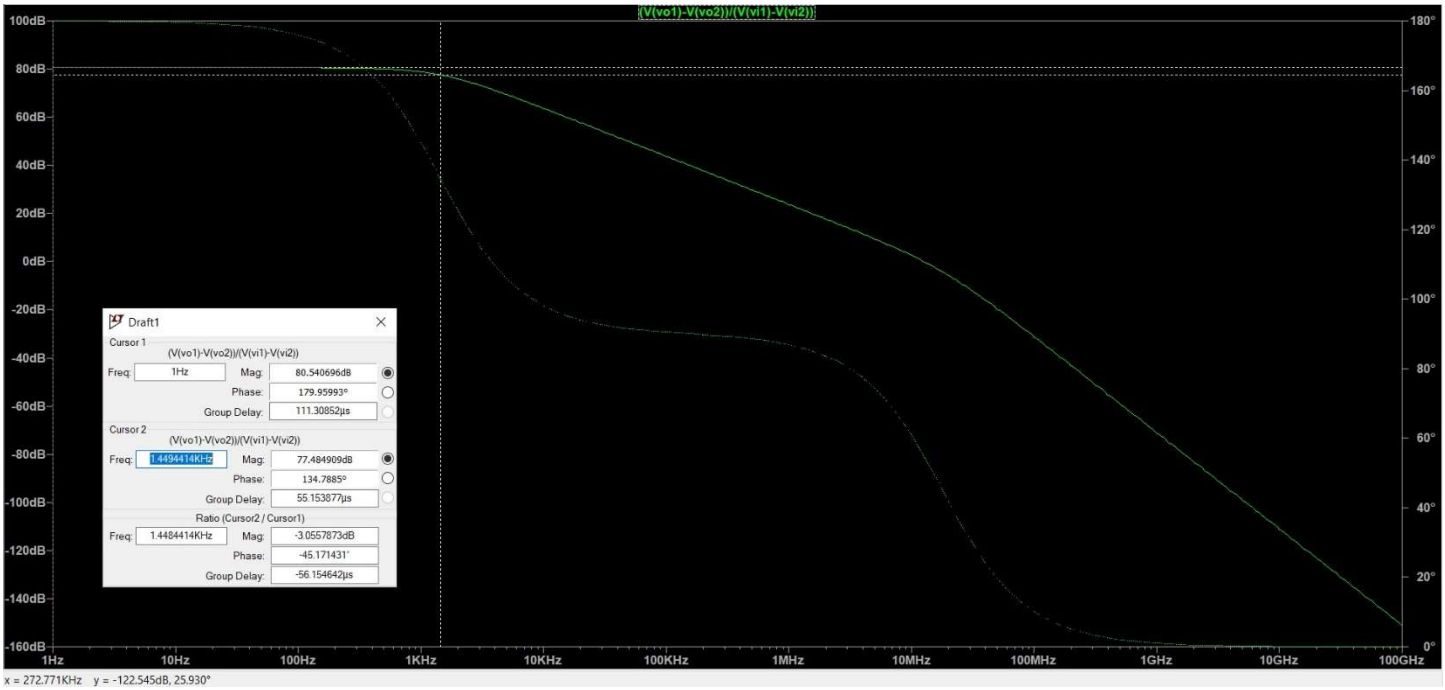


2. Bode Plot for AC gain and Phase



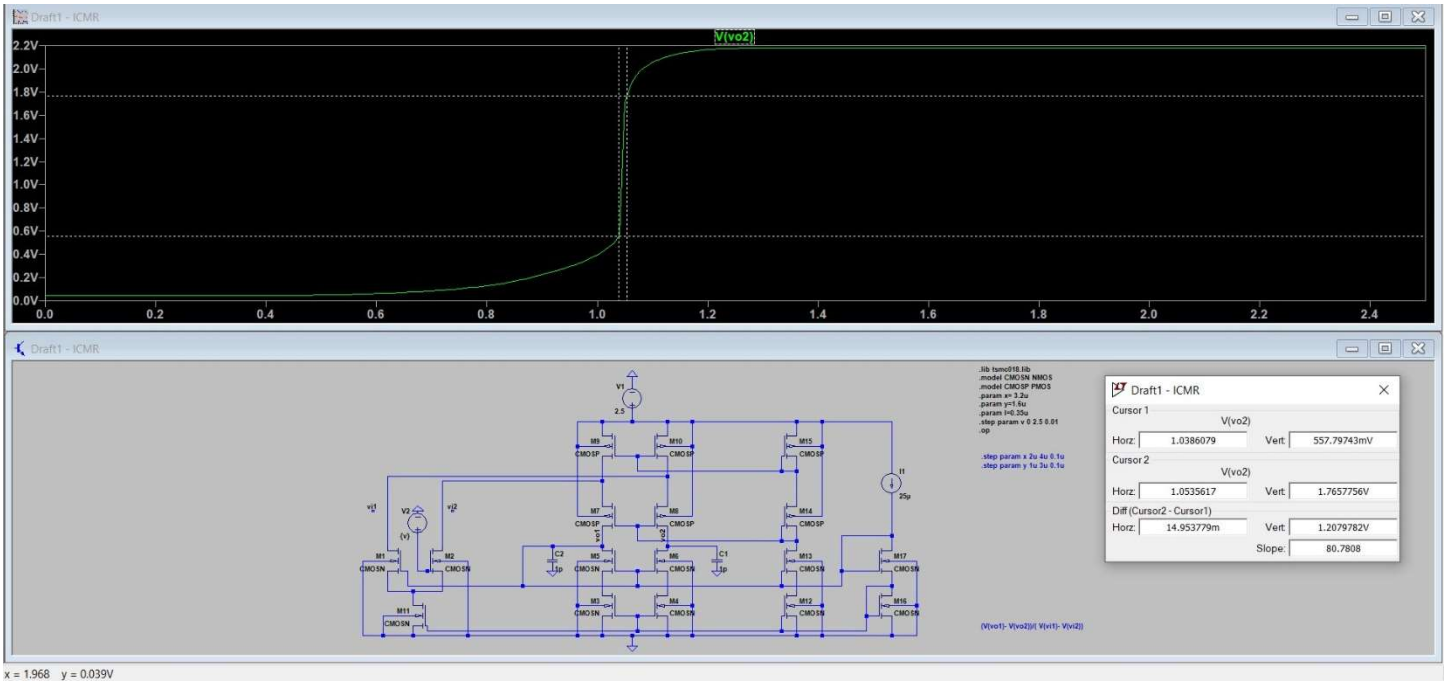
3. 3 dB Frequency

The 3 dB frequency is the frequency at which the gain reduces by 3 dB. Here, the 3 dB frequency is 1.45 Hz.



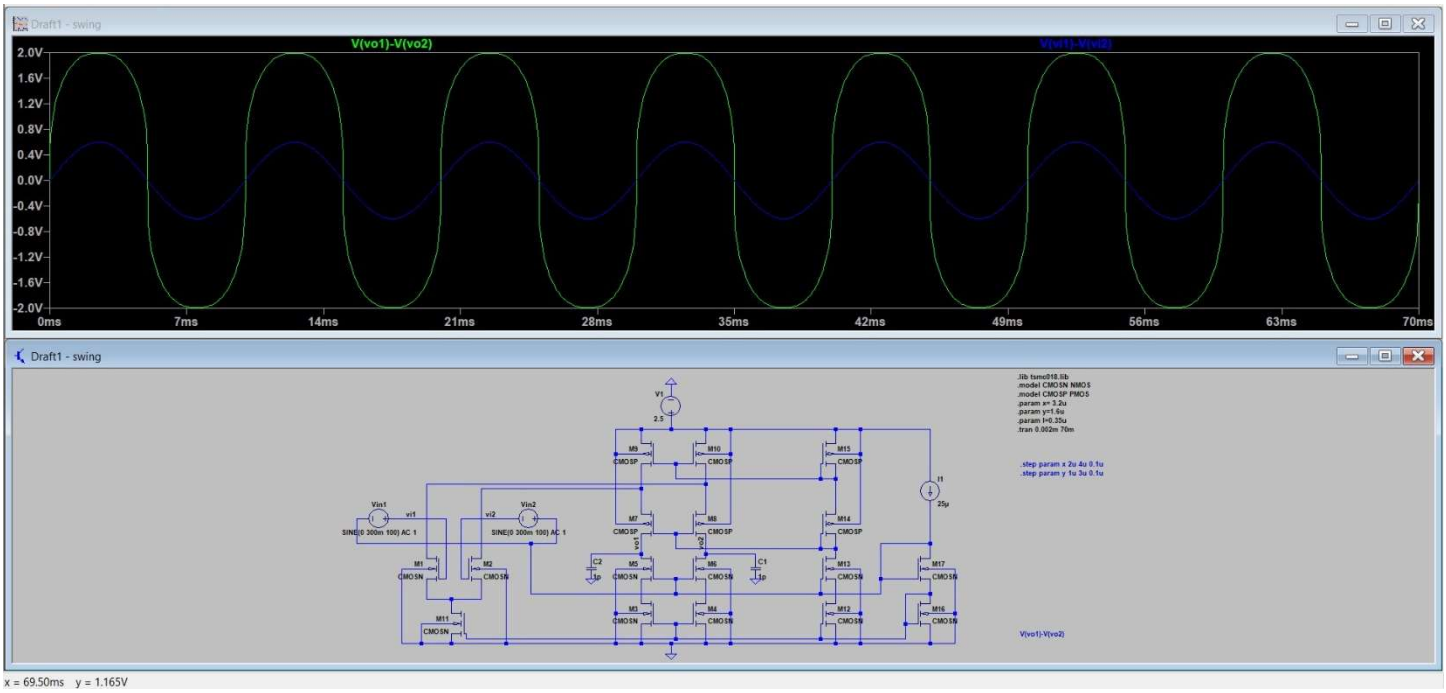
4. ICMR

The ICMR of the design is 0.557V to 1.76V



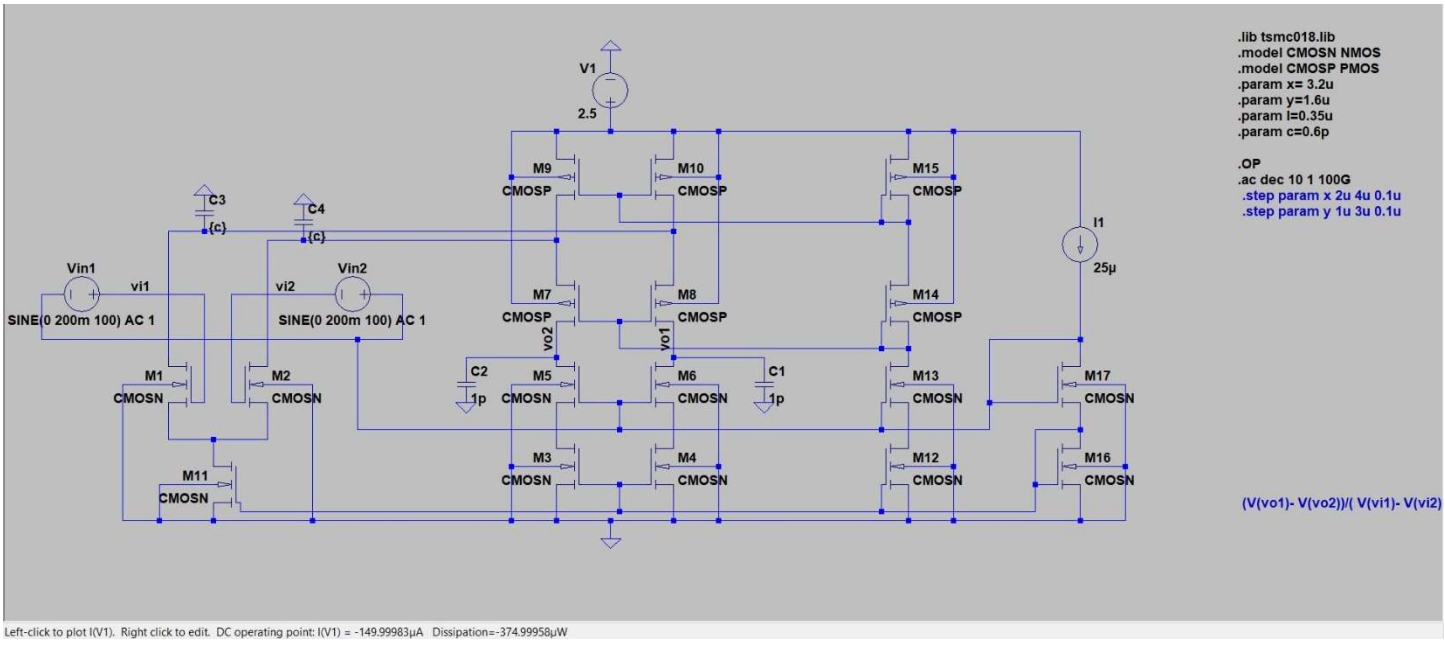
5. Differential Output Voltage Swing

The Differential output voltage swing achieved by the circuit is 2V. Beyond this, clipping would happen.



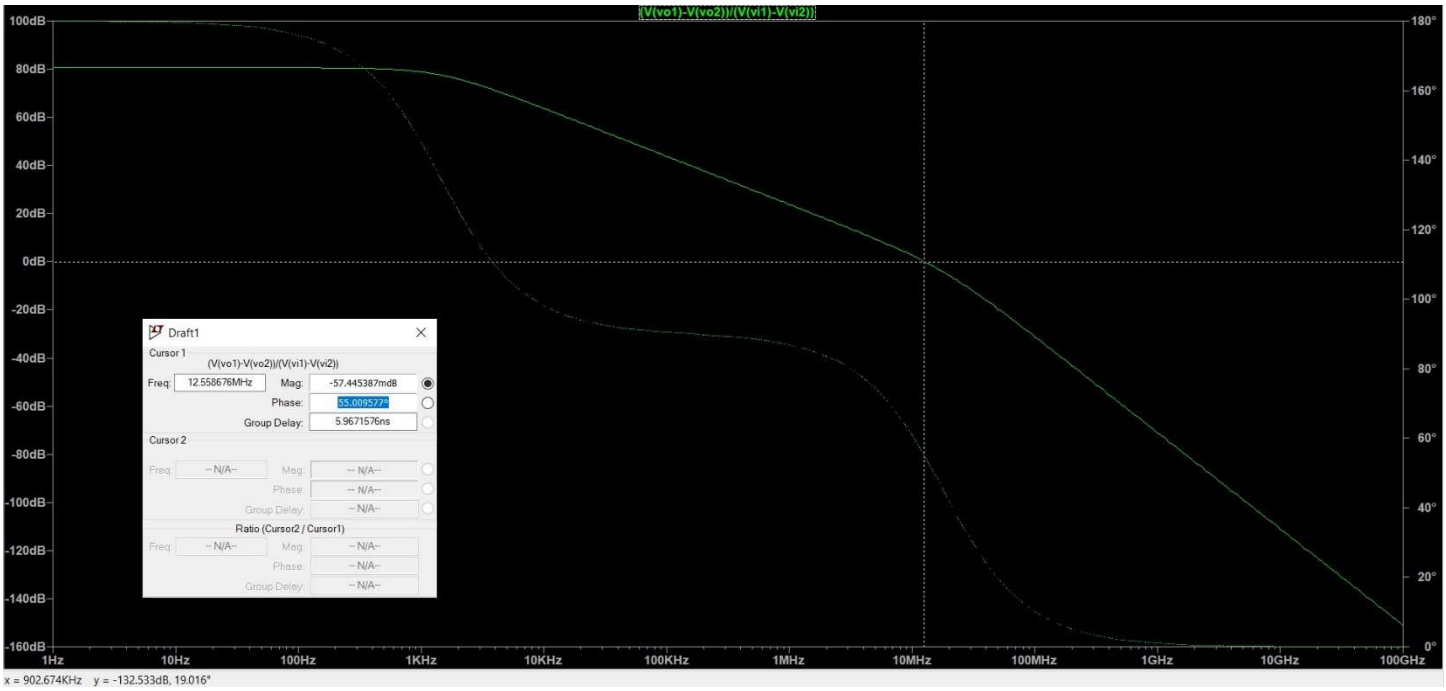
6. Power Dissipation

As mentioned in the bottom bar, the total power dissipation of the circuit is 0.375mW, as the total current drawn by the 2.5V voltage source is 150 µA.



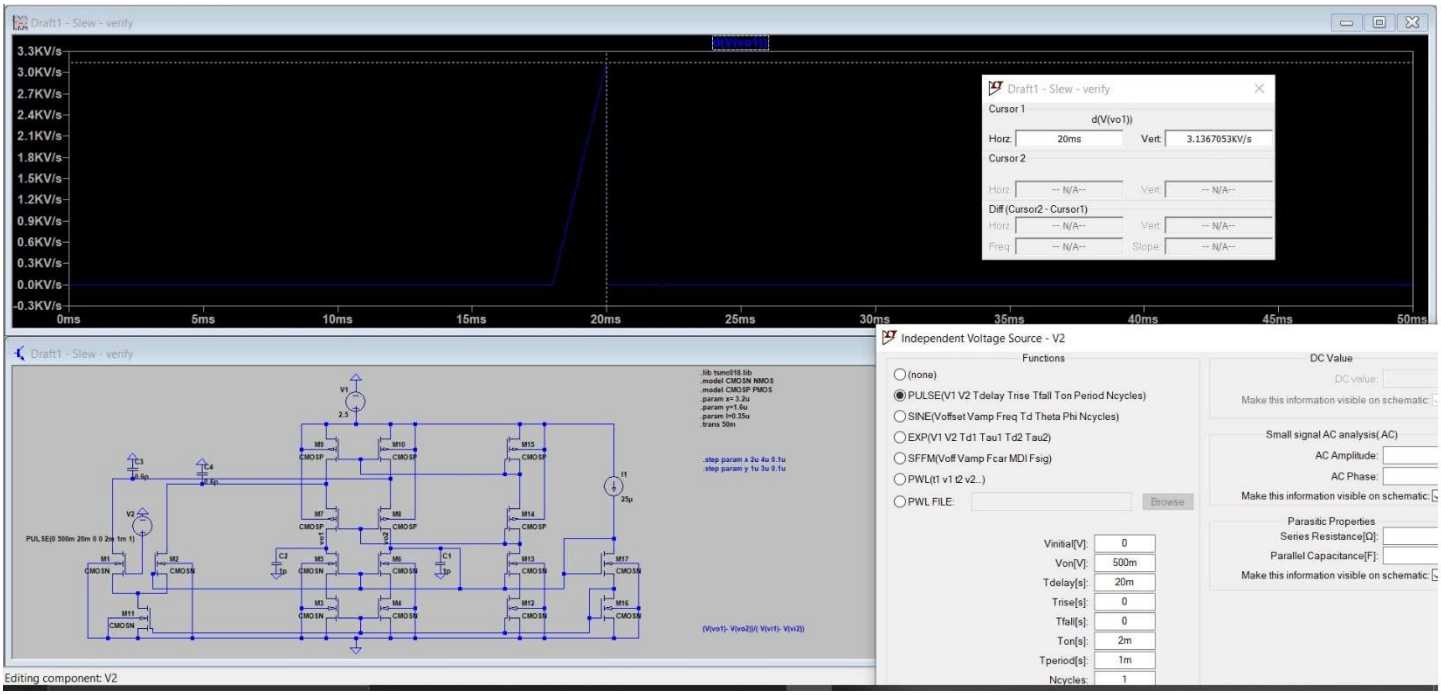
7. Phase Margin

To improve the phase margin, we attached capacitors with capacitance 0.6pF at the drain of the input MOSs. In this way, we achieved a phase margin of 55 degrees.



8. Slew Rate

The slew rate achieved is 0.003 V/μs .



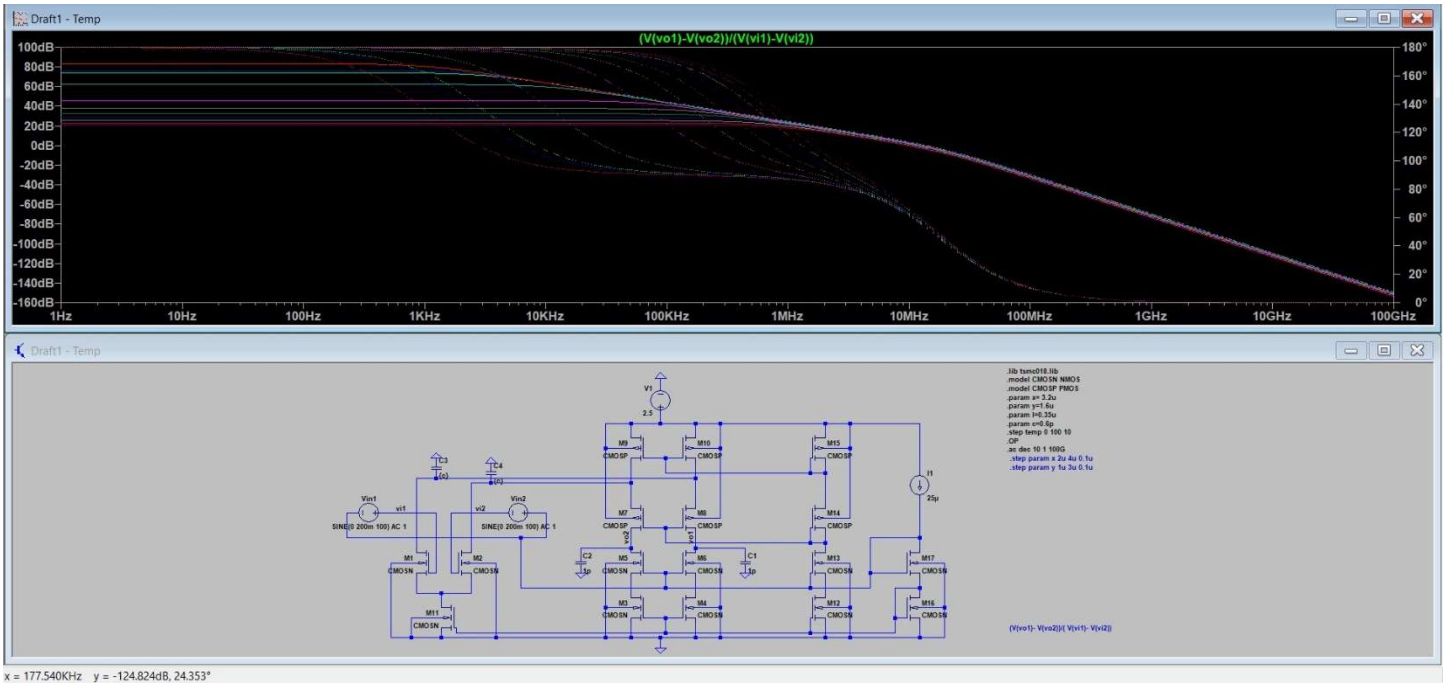
9. Temperature Sweep

As analysis for process corners cannot be done in LTspice, we performed a temperature sweep from 0 degree celcius to 100 degrees celcius.

Gain at 0 degrees celcius - 20 dB

Gain at 27 degrees celcius - 80.54 dB

Gain at 100 degrees celcius - 75 dB



PTO

10. DC Operating Point

All MOSFETs are in saturation region.

--- Operating Point ---

V(n004):	1.76049	voltage
V(vi2):	1.04583	voltage
V(n008):	0.522913	voltage
V(n003):	1.76049	voltage
V(vi1):	1.04583	voltage
V(n009):	0.522053	voltage
V(n007):	0.522913	voltage
V(n010):	0.522053	voltage
V(vo2):	1.01583	voltage
V(n005):	1.04583	voltage
V(vo1):	1.01583	voltage
V(n006):	1.02098	voltage
V(n001):	2.5	voltage
V(n002):	1.76049	voltage
V(n011):	0.522323	voltage
Id(M15):	2.5e-05	device_current
Ig(M15):	-0	device_current
Ib(M15):	7.49509e-13	device_current
Is(M15):	-2.5e-05	device_current
Id(M14):	2.5e-05	device_current
Ig(M14):	-0	device_current
Ib(M14):	2.23853e-12	device_current
Is(M14):	-2.5e-05	device_current
Id(M9):	4.99999e-05	device_current
Ig(M9):	-0	device_current
Ib(M9):	7.4951e-13	device_current
Is(M9):	-4.99999e-05	device_current
Id(M10):	4.99999e-05	device_current
Ig(M10):	-0	device_current
Ib(M10):	7.4951e-13	device_current
Is(M10):	-4.99999e-05	device_current
Id(M8):	2.49999e-05	device_current
Ig(M8):	-0	device_current
Ib(M8):	2.24368e-12	device_current
Is(M8):	-2.49999e-05	device_current
Id(M7):	2.49999e-05	device_current
Ig(M7):	-0	device_current
Ib(M7):	2.24368e-12	device_current
Is(M7):	-2.49999e-05	device_current
Id(M17):	2.5e-05	device_current
Ig(M17):	0	device_current
Ib(M17):	-1.58874e-12	device_current
Is(M17):	-2.5e-05	device_current
Id(M16):	2.5e-05	device_current
Ig(M16):	0	device_current
Ib(M16):	-5.32912e-13	device_current
Is(M16):	-2.5e-05	device_current
Id(M13):	2.5e-05	device_current
Ig(M13):	0	device_current
Ib(M13):	-1.5633e-12	device_current
Is(M13):	-2.5e-05	device_current
Id(M12):	2.5e-05	device_current
Ig(M12):	0	device_current
Ib(M12):	-5.32323e-13	device_current
Is(M12):	-2.5e-05	device_current
Id(M11):	5e-05	device_current
Ig(M11):	0	device_current
Ib(M11):	-5.32913e-13	device_current
Is(M11):	-5e-05	device_current
Id(M6):	2.49999e-05	device_current
Ig(M6):	0	device_current
Ib(M6):	-1.55788e-12	device_current
Is(M6):	-2.49999e-05	device_current
Id(M5):	2.49999e-05	device_current
Ig(M5):	0	device_current
Ib(M5):	-1.55788e-12	device_current
Is(M5):	-2.49999e-05	device_current
Id(M4):	2.49999e-05	device_current
Ig(M4):	0	device_current
Ib(M4):	-5.32053e-13	device_current
Is(M4):	-2.49999e-05	device_current
Id(M3):	2.49999e-05	device_current
Ig(M3):	0	device_current
Ib(M3):	-5.32053e-13	device_current
Is(M3):	-2.49999e-05	device_current
Id(M1):	2.5e-05	device_current
Ig(M1):	0	device_current
Ib(M1):	-2.3034e-12	device_current
Is(M1):	-2.5e-05	device_current
Id(M2):	2.5e-05	device_current
Ig(M2):	0	device_current
Ib(M2):	-2.3034e-12	device_current
Is(M2):	-2.5e-05	device_current
I(C4):	-1.05629e-24	device_current
I(C3):	-1.05629e-24	device_current
I(C2):	1.01583e-24	device_current
I(C1):	1.01583e-24	device_current
I(I1):	2.5e-05	device_current
I(Vin2):	-6.77626e-21	device_current
I(Vin1):	0	device_current
I(V1):	-0.00015	device_current

SPECIFICATIONS AND CONCLUSIONS

S.NO.	METRIC	REQUIRED SPECS	CIRCUIT SPECS
1	DC Gain	≥ 80 dB	80.54 dB
2	Power Dissipation	≤ 0.4 mW	0.375 mW
3	Phase Margin	50 – 60 degrees	55 degrees
4	Channel Length	≥ 350 nm	350 nm
5	No. of current sources	1	1
6	Vdd	2.5 V	2.5
7	Load Capacitance	≤ 1 pF	1 pF
8	Current mirror ratios	≤ 20	≤ 20
9	Technology	TSMC 180 nm	TSMC 180 nm
10	ICMR		0.557V – 1.74V
11	Slew Rate		0.003 V/μs
12	Output voltage Swing (Diff.)		2V
13	Input Offset voltage		0V
14	Output Offset Voltage		0V

PROBLEMS FACED DURING THE DESIGN

The major problem faced was to keep all the MOSFETS in saturations region, for which a suitable biasing circuitry was needed. Initially we had only 1 MOS along with the current source in the biasing circuitry, but then the widths needed were very large and it was getting hard to keep all MOSFETS in saturation.

INNOVATION IN DESIGN

To tackle the above-mentioned problem with biasing, we tried to modify the current mirror biasing. Hence, in the biasing circuitry used eventually, a total of 6 MOSFETS are used along with a single current source.

We could have further increased the gain by increasing the current of the current source as the current power dissipation is still 0.025mW less than the specified upper limit, but we settled doing a trade off so that the differential output voltage swing can be increased (which is currently 2V).

The dimension sweeping in LTSpice is done in such a way that the widths of all the MOSFETS are comparable and integer multiples of the smallest width. This is advantageous while making the layout of the circuit.

To improve the phase margin of the circuit, we attached two capacitors having capacitance of 0.6pF at the drain of the input MOSFETS. This gave a phase margin of 55 degrees.