Round 3: CMOS Amplifier design.

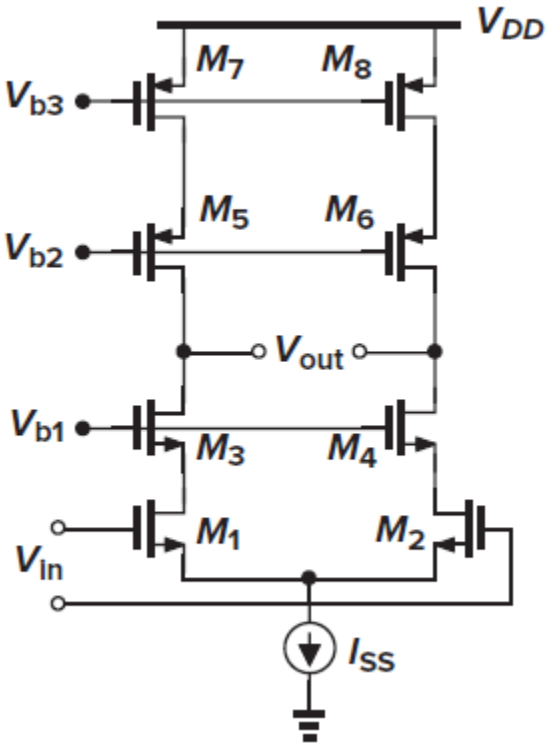
Instructions:

1. Participants are **not** allowed to use Resistors (**except Rload**) as part of their design. Biasing circuitry should be designed using MOSFETs (exception: the input terminals). The model will be provided to you before the start of this round.
2. Voltage sources should be used for Power supply and input transistors of the stages. Avoid additional voltage sources.
3. **Mention the trade-offs made as comments in your LTSpice schematic**. If a given specification is not met, do not worry, as the evaluation/ marking scheme is not binary.
4. Label the nodes with appropriate names wherever necessary.
5. Duration of 3hrs
6. Submit the Schematic (.asc file) (naming the file: 20VVWWXXYYYYZ.asc, where the ID number corresponds to the person who filled the google form during registration)
7. A google form will be provided at the end of that round for submitting your schematic.

You are working in a design team where you are to design a sound system. The microphone input and speaker output has been handled by your teammates, and you have to design an amplifier to meet the specs they provided to you.

Your design partner set up the topology for an operational amplifier before he was transferred to a different project. You are to add to his design and meet the specifications.

Add to the template of a telescopic OpAmp provided to you, and optimise to meet the following specifications :



Notes:

1. **The model names of the PMOS devices must be CMOSP, and NMOS devices must be CMOSN**
2. Iss has to be modelled using a MOSFET**.**
3. Output has to be **single ended.**
4. You can request for the inputs to ride over a DC voltage of your choice.
5. Comments in the schematic provided by us can be removed.

Specifications:

Technology(L)	0.35um
Supply Rails	2.5V, 0V
Open loop gain	≥ 60 dB
Rload	50 Ω
3db frequency	≥ 50kHz
Power dissipation	≤ 5mW
Power Supplied to load	≥ 0.5mW
Ibias	-
Current Mirror Ratios (W2/W1)	≤ 20
Capacitance(s)	≤ 1pF