ECE270: ELD: Quiz 3A (20 Minutes)

Date: October 24, 2024

1. Explain at least four signals in AXI Read Address and Control Channel. Mention the source and destination of each signal.

(4 marks)

2. Explain the constraints on ready and valid signals in AXI transaction.

(2 marks)

3. Draw the timing diagram explaining the AXI Lite write transaction to write 32 bits of data. Mention the source and destination of each signal.

(4 marks)

Ans. 1.

Signal	Description	Source	Destination
ARADDR	To indicate the address or memory location from where the data needs to be read.	Master	Slave
ARVALID	The information source uses the VALID signal to show when valid address, data or control information is available on the channel.	Master	Slave
ARREADY	The destination uses the READY signal to show when it can accept the information.	Slave	Master
RDATA	To indicate the data that is being read from a particular address or memory location.	Slave	Master
RLAST	To indicate the transfer of the final data item in a transaction.	Slave	Master
RVALID	The information source uses the VALID signal to show when valid address, data or control information is available on the channel.	Slave	Master
RREADY	The destination uses the READY signal to show when it can accept the information.	Master	Slave

Ans. 2

1. Source and VALID Signal:

- The source generates the `VALID` signal to indicate that the address, data, or control information is available on the bus and ready to be read by the destination.

- A thumbrule for the source is that it cannot wait for the `READY` signal from the destination before asserting `VALID`. This means the source must assert `VALID` as soon as the data or address is ready, regardless of the state of `READY`.

- Once `VALID` is asserted, it must stay high until the transfer handshake completes. This handshake occurs on a rising clock edge when both `VALID` and `READY` are high simultaneously.

2. Destination and READY Signal :

- The destination generates the `READY` signal to indicate it is ready to accept the information from the source.

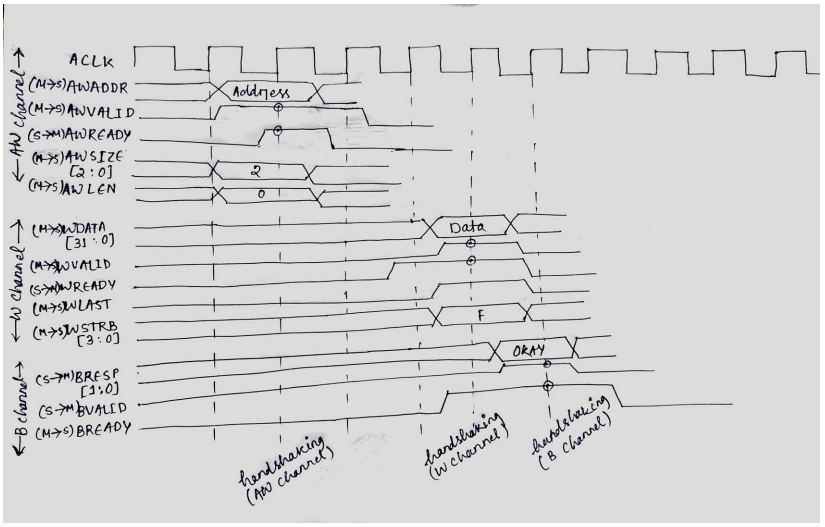
- The destination is allowed to wait until `VALID` is asserted before it asserts `READY`, allowing it to control when it is prepared to receive data.

- Additionally, the destination can assert `READY` when it's ready but is also allowed to deassert `READY` before the source asserts `VALID`. This means the destination can indicate readiness but may change its state before `VALID` is high if its circumstances change.

3. Data Transfer Condition :

- The actual transfer of information occurs only when both `VALID` and `READY` are high in the same clock cycle. This simultaneous assertion of both signals creates a handshake , indicating that the data on the bus has been successfully transferred.

Ans. 3



AW Channel - 2M

W Channel - 1M

B Channel - 1M