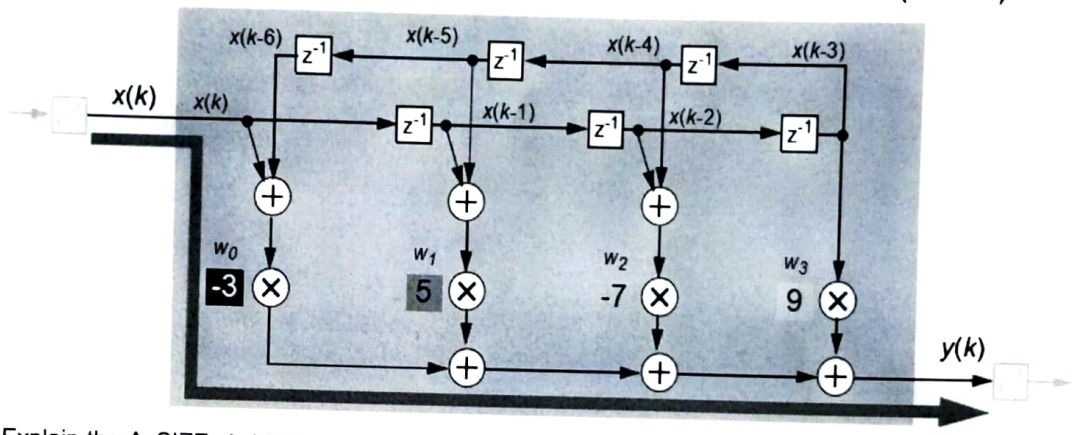
ECE270: ELD: End-Sem Exam (10 Marks) and Quiz 4 (10 Marks)

Date: December 7, 2024

End-Sem Exam

1. For the circuit shown below, the delay of the multiplier and adder is identical and equal to 1 ms. Fully pipeline the below circuit to achieve the clock period of 1ms without compromising on the functionality. Explain each stage of cut-set retiming. Find out the latency and throughput of the fully pipelined and non-pipelined circuit

(7 marks)



2. Explain the AxSIZE, AxLEN and STRB signals with suitable example of AXI Memory mapped read transaction.

(3 marks)

Quiz 4

1. With suitable examples, explain the differences between pipelining and parallel processing.

(4 marks)

3. Find out whether the given starting address is valid. If it is not valid, identify the nearest valid address. Also, find out the total wastage of memory between given and valid starting address.

IP1	32 MB	0x4002_0000
IP2	2 GB	0x0020_8000_0000

(6 marks)

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End-Sem Exam

1. Draw the timing diagrams of AXI LITE read transactions. Show two scenarios: 1) Master is ready before slave asserts valid signal and master becomes ready after slave asserts valid signal.

(3 marks)

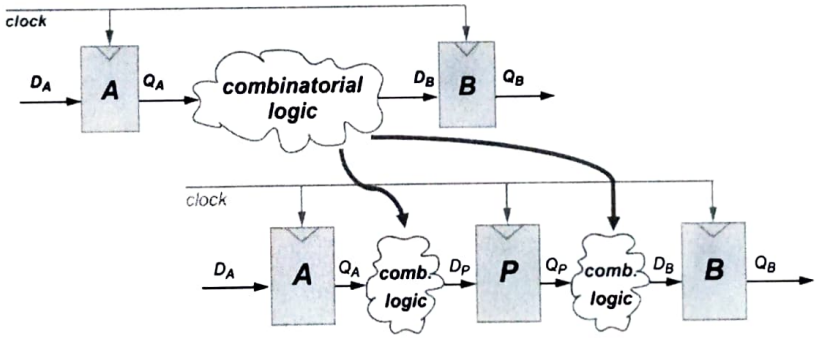
2. Consider Zynq SoC with memory mapped IO where the start or base address for any accelerator in PL must be equal to or higher than 0x0000_07FF. The example design consists of few accelerators and their memory requirements in Bytes are given in the table below. Assign appropriate starting or base address to each accelerator. Care must be taken to avoid memory wastage. Support your answer with appropriate explanation. **Short answers will not be evaluated.**

Accelerator Name	Memory Requirement
AXI GPIO1	4K
AXI BRAM	256K
AXI CDMA	2K
AXI Timer	128K

(7 marks)

Quiz 4

1. Using suitable example, explain why the clock period is not reduced by factor 2 when combinational circuit is pipelined by inserting one stage of FFs as shown below.



(6 marks)

2. Find out the maximum size of the hardware IP for which both the addresses 0x2300_0008 and 0x2300_0010 are valid. Explain your answer.

(3 marks)

3. Mention any two differences between AXI DMA and PS DMA in the Zynq SoC.

(1 marks)

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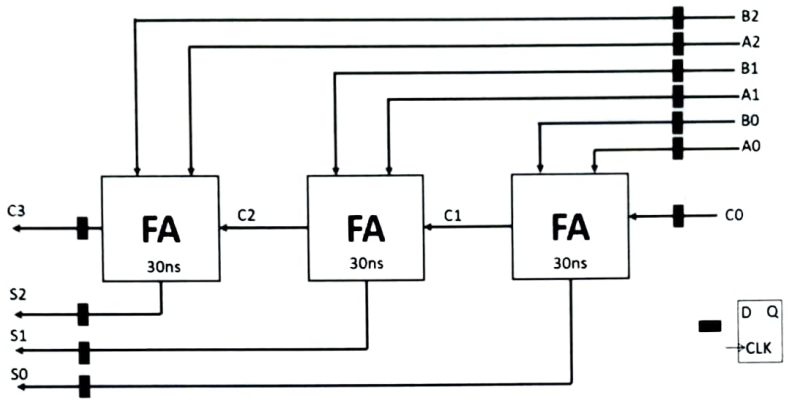
End-Sem Exam

1. Fully pipeline the below circuit via cut-set retiming without compromising on the functionality. Find out the latency and throughput of the fully pipelined and non-pipelined circuit given below.

(4 marks)



2. Consider Zynq SoC with memory mapped IO where the start or base address for any accelerator in PL must be equal to or higher than 0x0001_FFFF. The example design consists of few accelerators and their memory requirements in Bytes are given in the table below. Assign appropriate starting or base address to each accelerator. Care must be taken to avoid memory wastage. Support your answer with appropriate explanation. **Short answers will not be evaluated.**

Accelerator Name	Memory Requirement
AXI BRAM	256K
AXI Timer	128K

(6 marks)

Quiz 4

1. Using suitable example, explain why the clock period should be higher than the maximum latency of the combination circuit.

(4 marks)

2. What is the meaning EMIO interface? Why is it useful? Explain with suitable example.

(3 marks)

3. Explain the tasks of first stage boot loader in the Zynq boot process.

(3 marks)