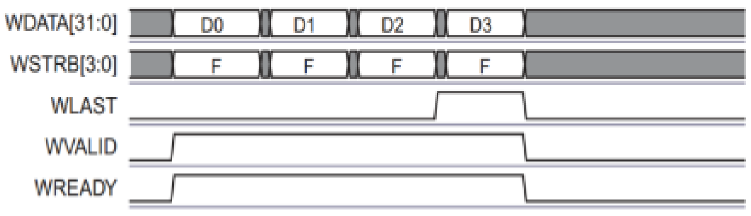
# ECE270: ELD: Quiz 3B (20 Minutes)

**Date**: October 24, 2024

1. Explain at least four signals in AXI Write Data Channel. Mention the source and destination of each signal.

**Write Data Channel Signals**



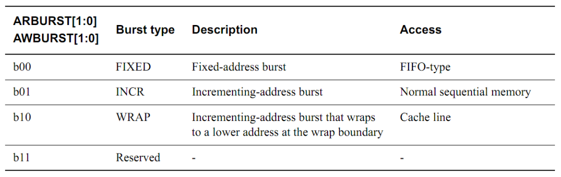
1. **WDATA[31:0] (Write Data)**
    ○ The actual data being transferred from the master to the slave. In this example, the data values D0, D1, D2, and D3 are written in four separate transfers. Source: Master, Destination: Slave.
2. **WSTRB[3:0] (Write Strobe)**
    ○ Indicates which bytes within WDATA are valid for each transfer. Here, WSTRB = F for all transfers, which means all 4 bytes (32 bits) of data are valid. Source: Master, Destination: Slave.
3. **WLAST**
    ○ Signals the last data transfer in the burst. It goes high during the final data transfer (D3) to indicate the end of the burst. Source: Master, Destination: Slave.
4. **WVALID and WREADY**
    ○ **WVALID**: Sent by the master to indicate that the data on WDATA is valid.
    ○ **WREADY**: Sent by the slave to indicate it's ready to receive data.
    ○ Data is transferred when both WVALID and WREADY are high.

**(4 marks)**

2. Explain various BURST modes of AXI memory mapped protocol.

**(3 marks)**

Table 4-3 Burst type encoding



| ARBURST[1:0] AWBURST[1:0] | Burst type | Description | Access |
|---|---|---|---|
| b00 | FIXED | Fixed-address burst | FIFO-type |
| b01 | INCR | Incrementing-address burst | Normal sequential memory |
| b10 | WRAP | Incrementing-address burst that wraps to a lower address at the wrap boundary | Cache line |
| b11 | Reserved | - | - |

**Fixed burst**

- Address remains the same for every transfer in the burst
- Repeat access to the same location

**Incrementing burst**

- Address for the each tranfer in the burst is an increment of the previous address
- The increment value depends on the size of the tranfer

**Wrapping burst**

- The start address must be aligned to the size of the tranfer
- The length of the burst must be 2, 4, 8 or 16.

3. Draw the timing diagram explaining the AXI stream transaction to send 20 bytes of data. Each transaction can transfer at most 4 bytes of data. Mention the source and destination of each signal.

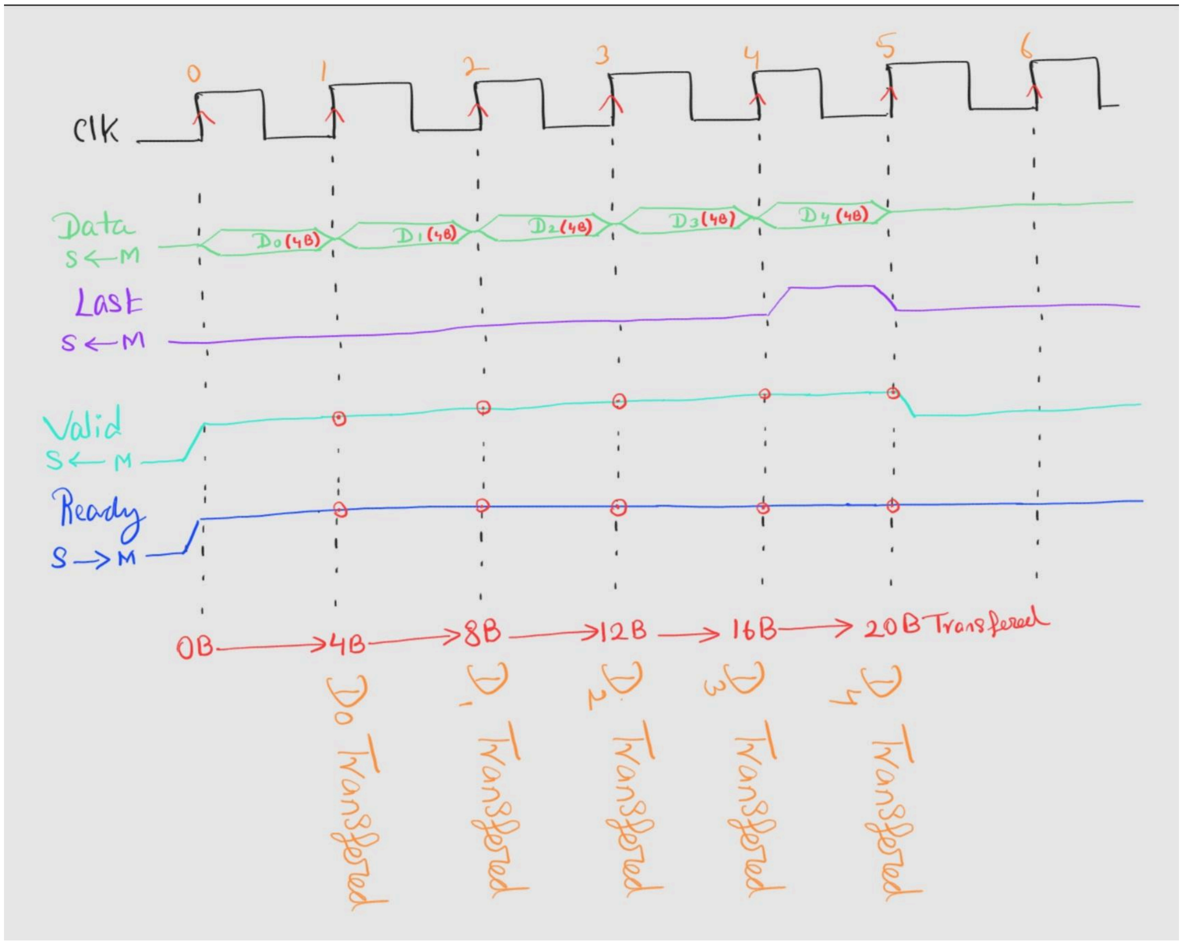
**(3 marks)**

**Diagram: 4*0.25= 1m (no mark for clock signal) and**

**Explaining any 4 signals of stream 4*0.25= 1m**

**Source and destination : 4*0.25= 1m**

**If you have written for Axi memory mapped then -> 0marks**



In an AXI stream transaction, several key signals coordinate the data transfer between the source and destination. Here's an overview of the 4 main signals:

Core AXI Stream Signals

1. TVALID [31:0] (Transmit Valid - Master as Source):

   Indicates that valid data is available on the data line (TDATA).

   The source asserts this signal when data is ready for transfer.

2. TREADY (Transmit Ready - by Destination):

   Indicates that the destination is ready to receive data.

   The destination asserts this signal when it can accept data in the current cycle.

3. TDATA (Transmit Data - by Mater as Source):

Carries the actual data to be transmitted.

The width of TDATA is configurable and can vary based on the implementation.

4. TLAST (Transmit Last -by Master as  Source):

Indicates the end of a packet or transaction.

The source asserts this signal to mark the last data transfer in a series.

In a typical AXI stream transfer:

- The source asserts **TVALID** when it has data ready.
- The destination asserts **TREADY** when it is ready to accept data.
- Data is transferred on **TDATA**, and **TLAST** signals the end of the packet.
- **TSTRB, TKEEP, TID, TDEST, and TUSER** are optional and used based on specific flexibility and data handling requirements.

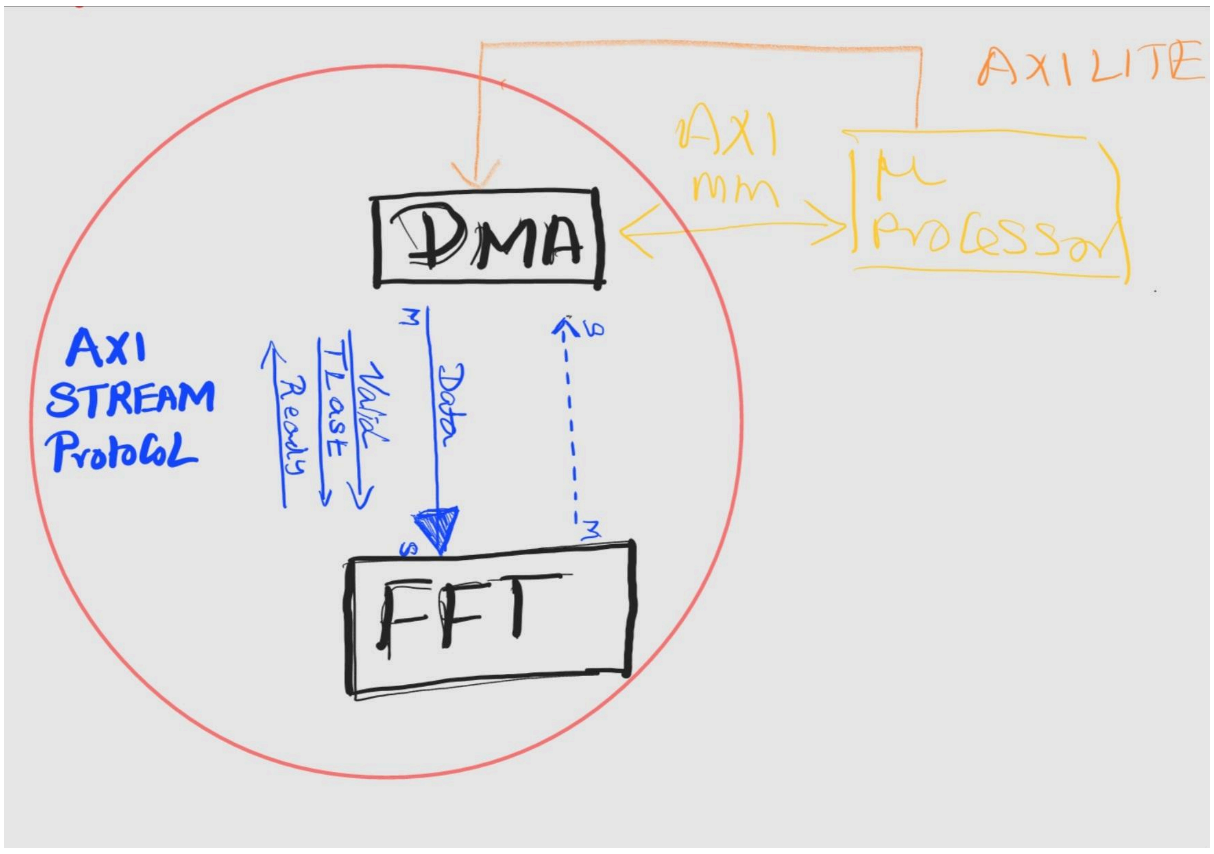
These signals provide flexibility and ensure smooth, controlled data transfers across the AXI Stream interface.

Reference for stream protocol:

https://www.intel.com/content/www/us/en/docs/programmable/683397/current/axi4-stream-protocol-signals.html#:~:text=The%20protocol%20transmits%20each%20line,last%20pixel%20of%20the%20line

https://docs.amd.com/r/en-US/ug1399-vitis-hls/How-AXI4-Stream-Works

Example stream transaction between 2 ips:


AXI LITE
AXI mm
μ Processor
DMA
FFT
AXI STREAM Protocol
Ready
TLast
Valid
Data
M
S
S
M