ECE270: ELD: Quiz 1A (20 Minutes)

Date: September 3, 2024

1. Write a Verilog code for a D-FF with asynchronous active low reset signal. (5 Marks)
2. Explain three differences between FPGA and micro-controllers. (3 marks)
3. Explain two differences between SRAM and DRAM memories. (2 marks)

ECE270: ELD: Quiz 2A (20 Minutes)

Date: September 24, 2024

1. Consider the design of 5-input LUT using two 4-input LUTs. Based on LUT architecture in FPGAs, draw and explain the architecture of 5-input LUT.

(4 marks)

2. Explain various types of combinational circuits and corresponding limitations in the use of 5-input LUTs for combinational circuit.

(3 marks)

3. Using suitable Verilog code, explain multi-driver error in digital hardware design.

(3 marks)

ECE270: ELD: Quiz 3A (20 Minutes)

Date: October 24, 2024

1. Explain at least four signals in AXI Read Address and Control Channel. Mention the source and destination of each signal.

(4 marks)

2. Explain the constraints on ready and valid signals in AXI transaction.

(2 marks)

3. Draw the timing diagram explaining the AXI Lite write transaction to write 32 bits of data. Mention the source and destination of each signal.

(4 marks)

ECE270: ELD: Mid-Sem Exam

Date: October 6, 2024

1. Consider the design of 10-input LUT using two 9-input LUTs. Based on LUT architecture in FPGAs, draw and explain the architecture of 10-input LUT. Explain any two distinct limitations of 10-input LUT for implementation of combinational circuits.

(5 marks)

2. Explain the difference between WRITE_FIRST and NO_CHANGE mode in BRAM of FPGA.

(4 marks)

3. Write a Verilog code for 4:1 MUX using behavioural and data flow modelling without using any instantiation approach.

(6 marks)

ECE270: ELD: End-Sem Lab Exam (10 Marks)

Date: December 7, 2024

1. Design an accelerator which performs multiplication by 2 ~~followed by addition by 2~~ before FFT operation on input data comprising of 8 complex samples of float data type.
   A. Implementation on processor and display the execution time (**1 Mark**)
   B. Implementation on PL, compare PS and PL outputs and display the execution time **(7 marks: 1 Mark for FFT)**
   C. Demonstrate the outputs of FFT on ILA **(2 marks)**

Hint: Use Floating point IP with multiplication operation and second input to addition operation may be given using the constant IP. Ensure that data inside the constant IP is in floating point format with appropriate radix. To input decimal 10, find out its floating-point representation in hexadecimal and enter in constant IP as 0xVALUE. Other option is to use fixed-to-float IP with constant IP.