

Q1. (a) For the circuit given in Figure 1, R_L is a potentiometer. Case a: R_L is removed and the overall voltage gain of the circuit is measured, it is found to be 0.98. Case b: Again R_L is connected and varied, it was observed that the overall gain of the circuit becomes half of as absorbed in case a, at $R_L = 500$ ohm. Assume that the amplifier remained linear throughout the measurement done in both cases. Find out the value of g_m and r_o . [12.5 marks]

(b) In the circuit given in Figure 2, the voltage source is an ideal voltage source providing both DC and AC superimposed. I_D is provided by an ideal current source. D is a real diode that follows the Exponential Current-Voltage relation of a diode. Assume that at the frequencies of interest(High), the capacitor becomes a closed circuit, that is, Zero-Impedance. Using the small-signal model for diode, determine the AC gain of circuit (V_o/V_i) where V_i is the input AC component and V_o is the output AC Component. By controlling which factors, can we control the AC component of V_o ? (Hint: In real circuits, the capacitances and resistances are usually fixed) [12.5 marks]

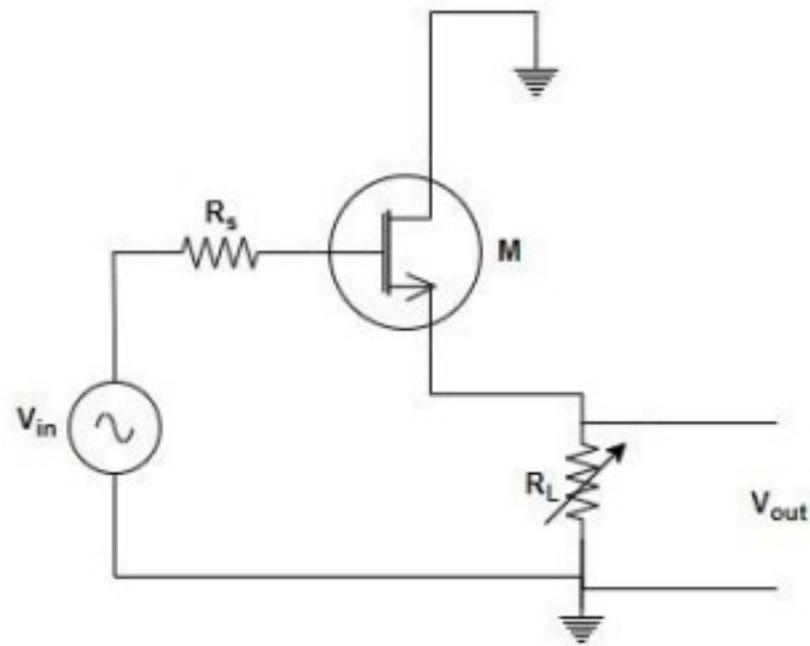


Figure 1

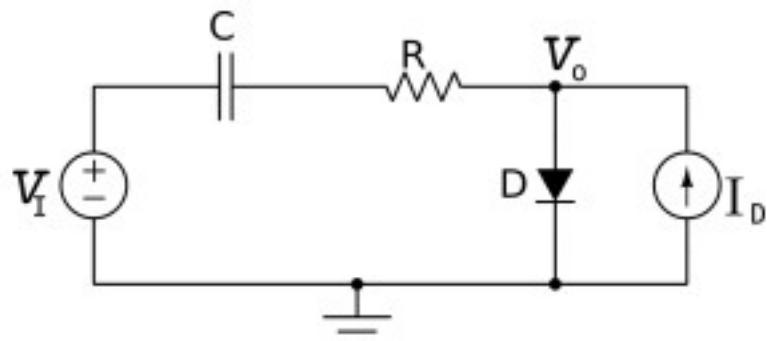
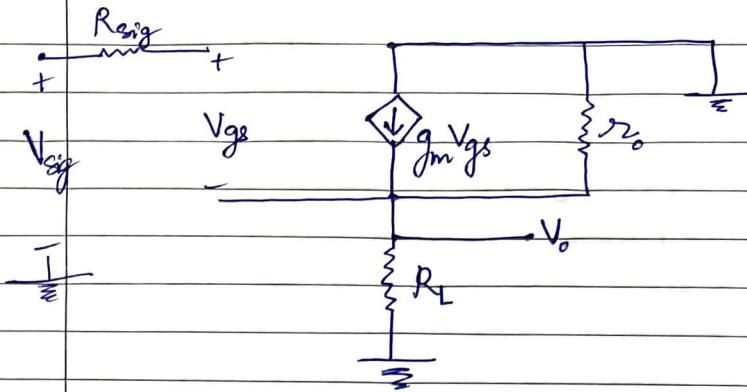


Figure 2



$$V_o = g_m V_{gs} (r_o \parallel R_L)$$

$$\frac{V_o}{V_{gs}} = g_m (r_o \parallel R_L) - \textcircled{1}$$

Now,

$$V_{sig} = V_{gs} + g_m V_{gs} (r_o \parallel R_L)$$

$$V_{sig} = V_{gs} [1 + g_m (r_o \parallel R_L)]$$

$$\frac{V_{gs}}{V_{sig}} = \frac{1}{1 + g_m (r_o \parallel R_L)} - \textcircled{2}$$

from $\textcircled{1}$ & $\textcircled{2}$,

$$\frac{V_o}{V_{sig}} = \frac{r_o \parallel R_L}{(r_o \parallel R_L) + 1/g_m}$$

if R_L is removed,

$$\frac{V_o}{V_{sig}} = \frac{r_o}{r_o + 1/g_m} = 0.98$$

$$\Rightarrow g_m r_o = 49 - \textcircled{3}$$

If $R_L = 500\Omega$ or $0.5k\Omega$,

$$\frac{V_o}{V_{sig}} = \frac{r_o || 0.5}{(r_o || 0.5) + \frac{1}{g_m}} = 0.49$$

$$\Rightarrow \frac{\frac{0.5 r_o}{(r_o + 0.5)}}{\left(\frac{0.5 r_o}{r_o + 0.5}\right) + \frac{1}{g_m}} = 0.49$$

$$\Rightarrow \frac{0.5 r_o}{0.5 r_o + \left(\frac{r_o + 0.5}{g_m}\right)} = 0.49$$

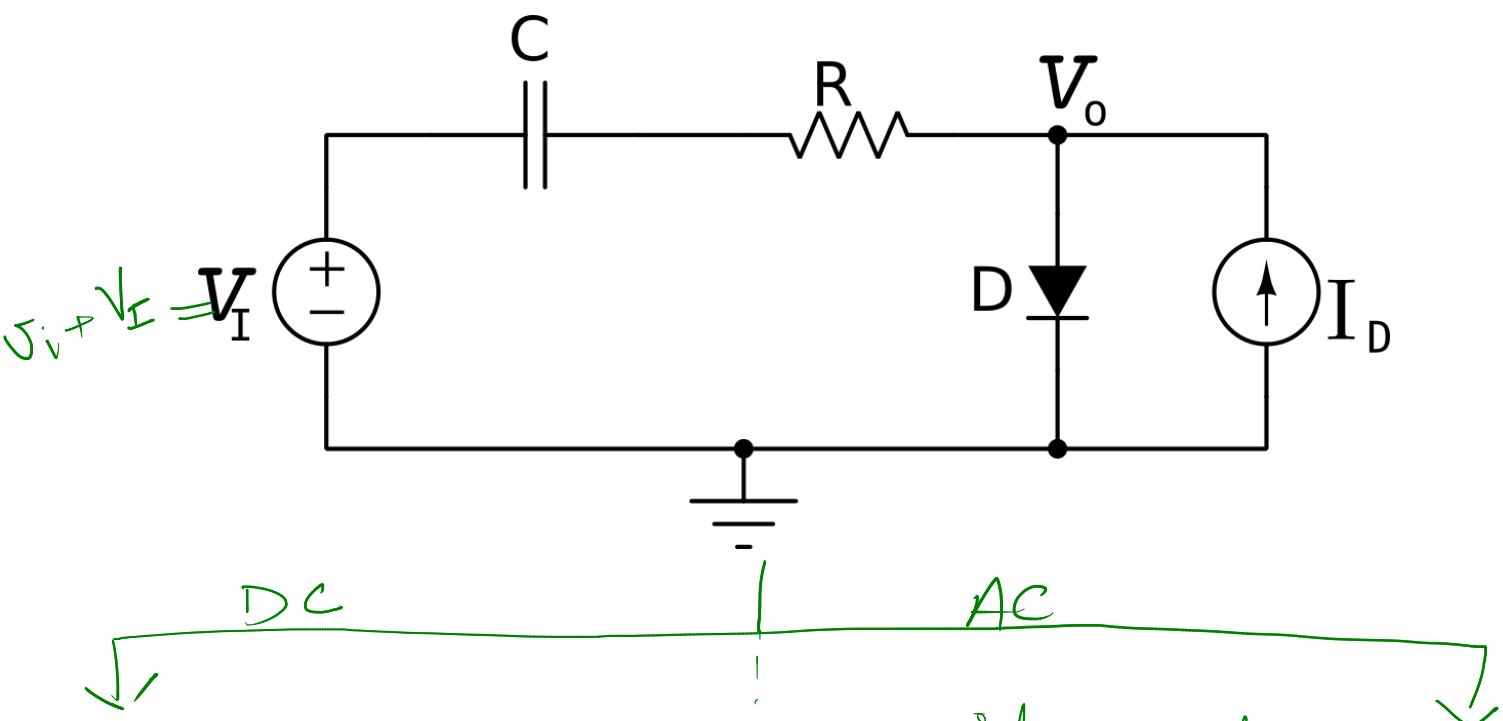
$$\Rightarrow \frac{0.5 r_o g_m}{0.5 r_o g_m + r_o + 0.5} = 0.49$$

from eqⁿ (3), $g_m r_o = 49$

$$\therefore \frac{0.5 \times 49}{(0.5 \times 49) + 0.5 + r_o} = 0.49$$

$$\Rightarrow r_o = \frac{0.5 \times 49}{0.49} - 0.5 - (0.5 \times 49)$$
$$\Rightarrow \boxed{r_o = 25 k\Omega}$$

$$\boxed{g_m = \frac{49}{25} \frac{mA}{V} = 1.96 \frac{mA}{V}}$$

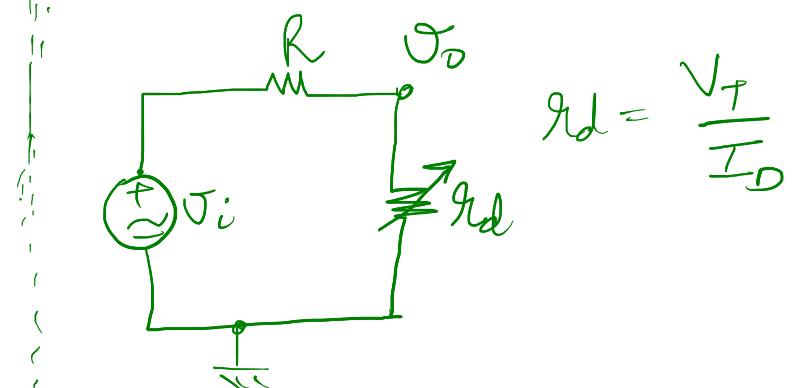
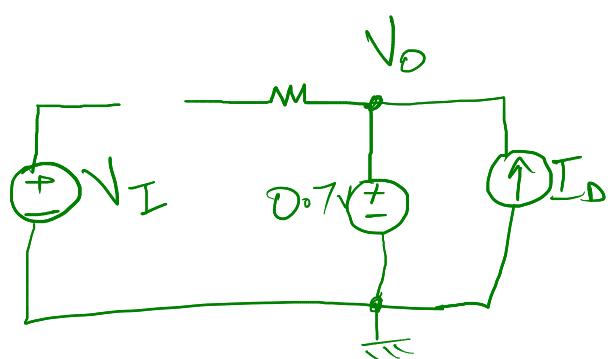


Capacitor \rightarrow open

Diode \rightarrow Voltage Source

Capacitor \rightarrow Closed

Diode \rightarrow Resistance



$$V_0 = \frac{R_d}{R_d + R} V_i \Rightarrow \frac{V_0}{V_i} = \frac{R_d}{R_d + R} = \text{AC Gain}$$

$$= \frac{1}{1 + \frac{R I_D}{\sqrt{I_F}}}$$

We can usually not change R in a circuit
But we can control I_D in a circuit
using BJT or a MOSFET.

thus, we can control the AC Gain
of the circuit by controlling I_D

Q2. For the circuit given in Figure 3. The base to emitter drop when the respective junction is operating in forward bias is, V_{BE} (forward) = 0.7V.

(a) Draw the DC load line and mark the Q-point of the transistor. Assume base current to be negligible wrt the current going into R_1 and R_2 . [10 marks]

(b) Determine the percentage change in collector current, if the transistor with $\beta = 60$ is replaced by another transistor with $\beta = 140$. [15 marks]

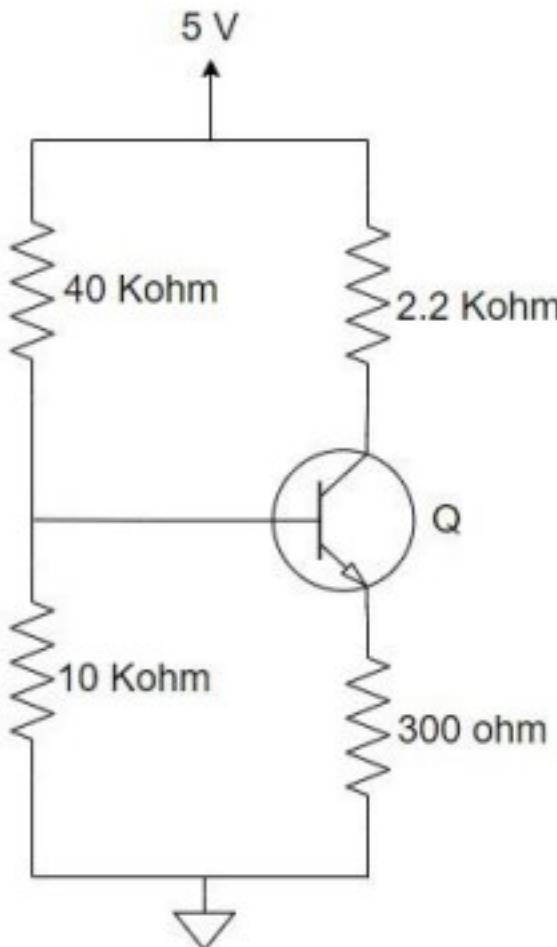


Figure 3

Answer (a)

$$V_{CC} = 5V, R_C = 2.2K\Omega, R_E = 300\Omega$$
$$R_2 = 40K\Omega, R_1 = 10K\Omega, V_{BE} = 0.7V$$

Now, for the given ckt -

$$V_B = \frac{R_1}{R_1 + R_2} \times V_{CC}$$
$$= \frac{10}{10+40} \times 5$$
$$= \frac{10}{50} \times 8 = 1V$$

$$V_E = V_B - V_{BE} = 1 - 0.7 = 0.3V$$

Now,

$$I_E = \frac{V_E}{R_E} = \frac{0.3}{3000} = 1mA$$

Also,

$$I_C \approx I_E = 1mA$$

We know that the voltage across collector resistor

$$V_{RC} = I_C \times R_C$$
$$= 1 \times 10^{-3} \times 2.2 \times 10^3$$
$$= 2.2V$$

Now,

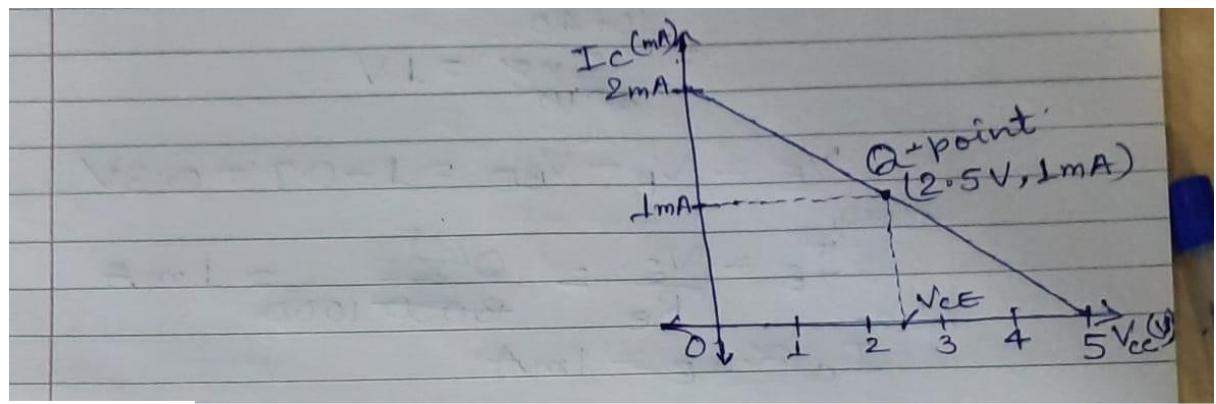
Voltage at collector w.r.t ground

$$V_C = V_{CC} - V_{RC}$$
$$= 5 - 2.2 = 2.8V$$

$$V_{CE} = V_C - V_E$$
$$= 2.8 - 0.3 = 2.5V$$

$$I_{Cmax} = \frac{V_{CC}}{(R_C + R_E)} = \frac{5}{(2.2 + 0.3)K} = \frac{5}{2.5K}$$

$$= 2mA$$



$$Q2.b. \quad I_E = \frac{V_{Th} - V_{BE}}{R_E + \frac{R_{Th}}{\beta}}$$

$$V_{BE} = 0.7V$$

$$R_E = 300\Omega$$

$$V_{Th} = \frac{R_1}{R_1 + R_2} \cdot V_{CC} = \frac{10}{10+40} \times 5 = 1V$$

$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{400k\Omega}{50} = 8k\Omega$$

$$\therefore I_E = \frac{1 - 0.7}{300 + \frac{8000}{\beta}} = \boxed{\frac{0.3\beta}{300\beta + 8000}}$$

$$I_C = \left(\frac{\beta}{\beta+1}\right) \cdot I_E = \left(\frac{\beta}{\beta+1}\right) \left(\frac{0.3\beta}{300\beta + 8000}\right)$$

$$= \frac{0.3\beta^2}{(\beta+1)(300\beta + 8000)}$$

$$\frac{\beta_1 = 60}{I_{C1} = \frac{(0.3)(60)^2}{(61)(300 \times 60) + 8000}} = 0.68095 \text{ mA}$$

$$I_{C2} = \frac{(0.3)(140)^2}{(141)(300 \times 140) + 8000} = 0.83404 \text{ mA} \quad \left. \begin{array}{l} \\ \end{array} \right\} \beta_2 = 140$$

$$\therefore \text{change} = \frac{(0.83404 - 0.68095)}{0.68095} \times 100 = \boxed{22.48\%}$$

Q3. Consider the circuit proposed by a student given in Figure 4 as an alternate for the differential amplifier circuit given in Figure 5. Where V_{in1} and V_{in2} is applied to ensure $(V_{in1}-V_{in2}) > 0.7V$, and the BJT remains in piecewise linear region. $I_c \approx I_E$.

- (a) For the circuit in Figure 4 find out the relation between V_{out} and $(V_{in1}-V_{in2})$. [10 marks]
- (b) Qualitatively compare differences between the circuits (Figures 4&5) on the basis of I_D and $(V_{in1} - V_{in2})$ (Proper graphical explanation, without driving the exact equation will suffice) and establish which one is a best choice for a differential amplifier. [10 marks]
- (c) It is required to design a class B output stage as shown in Figure 6 to deliver an average power of 20 W to an 8 ohm load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. Determine the maximum power that each transistor must be able to dissipate safely. [5 marks]

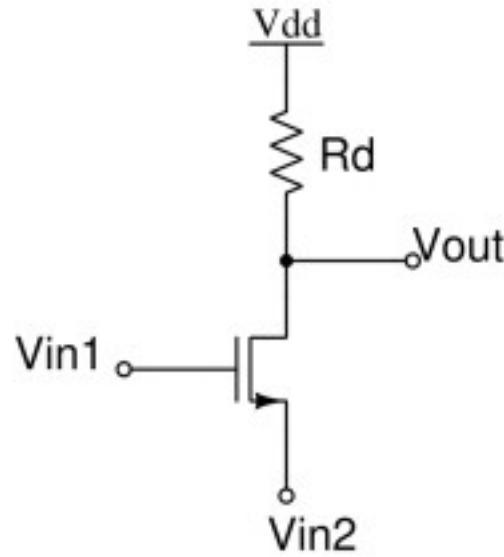


Figure 4

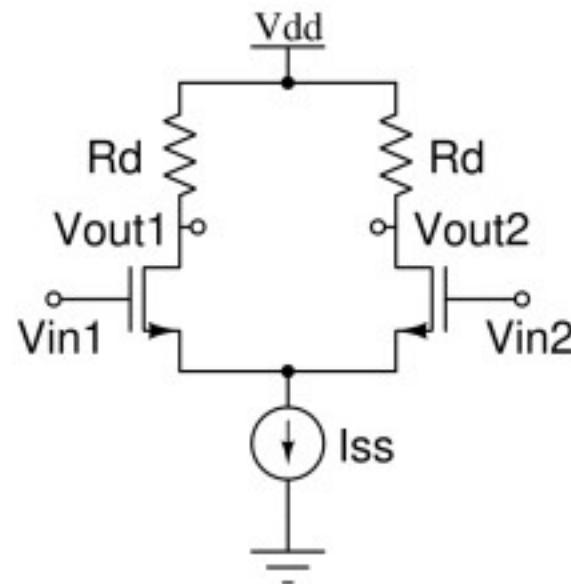


Figure 5

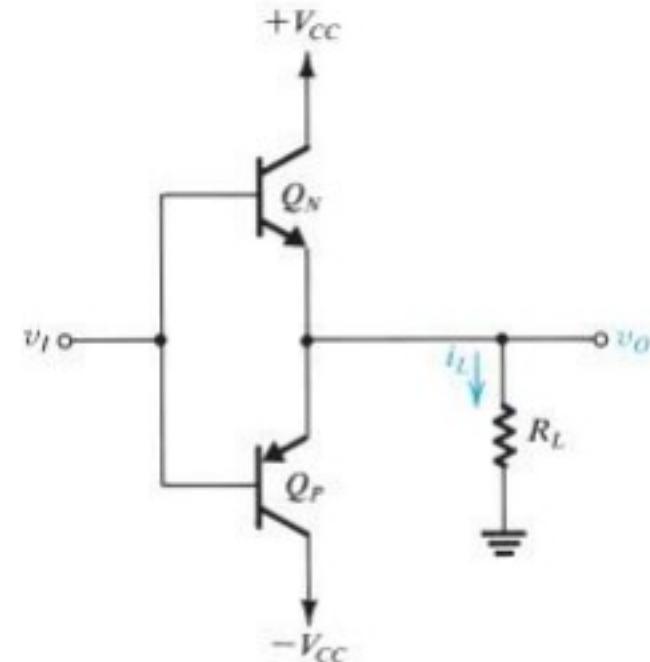
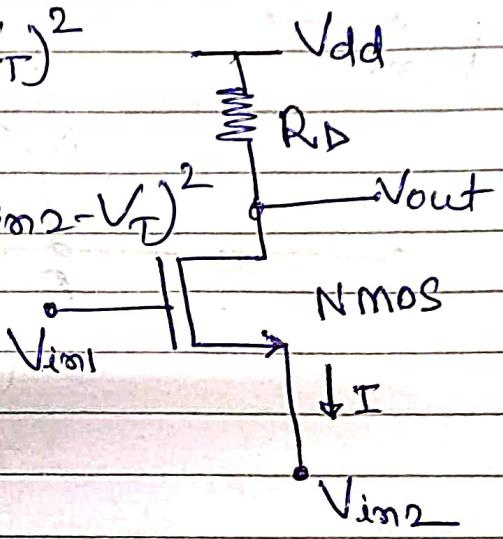


Figure 6

Q: 3(a) For the circuit to act as an amplifier NMOS should operate in saturation region and hence the biasing will be given in such a way that NMOS will operate in saturation.

$$j_D = \frac{1}{2} K_m \left(\frac{w}{L} \right) (V_{DS} - V_T)^2$$

$$j_D = \frac{1}{2} K_m \left(\frac{w}{L} \right) (V_{in1} - V_{in2} - V_T)^2$$



$$\therefore V_{DS} = V_{in1} - V_{in2}$$

$$\text{Now, } V_D = V_{DD} - j_D R_D$$

$$\therefore V_D = V_{out}$$

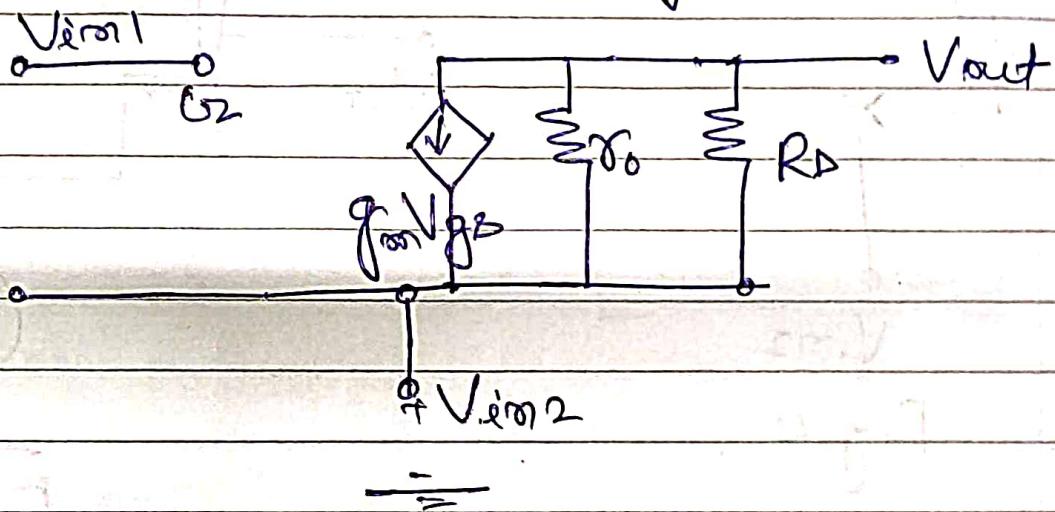
$$V_{out} = V_{DD} - K_m (V_{in1} - V_{in2} - V_T)^2 R_D$$

→ ①

Here, we can see that unlike the differential amplifier circuit given in Fig 5, we can not make V_{out} equal to zero even when common mode input is applied.

that is $V_{in1} = V_{in2}$. In fact if we apply common mode signal then NMOS will be off. For the NMOS to operate properly $V_{in1} - V_{in2} > V_T$.

Now, comparing the relations for V_{out} vs $V_{in1} - V_{in2}$ for small signal ACs,



$$V_{out} = -g_m V_{gs} (R_D || \tau_o)$$

$$V_{gs} = V_{in1} - V_{in2}$$

$$\therefore V_{out} = -g_m (R_D || \tau_o) (V_{in1} - V_{in2})$$

Hence, differential gain = $-g_m (R_D || \tau_o)$.

provided $V_{in1} - V_{in2} > V_T$
and MOSFET is operating
in saturation.

Q. 3.(b) We have to compare the circuit on the basis of I_D , V_S ($V_{in1} - V_{in2}$).

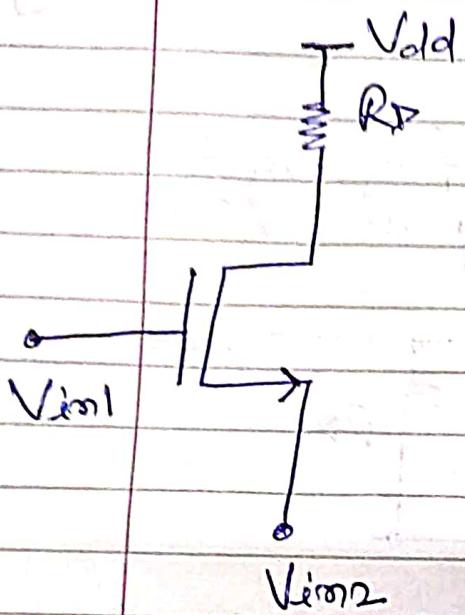


Fig 4

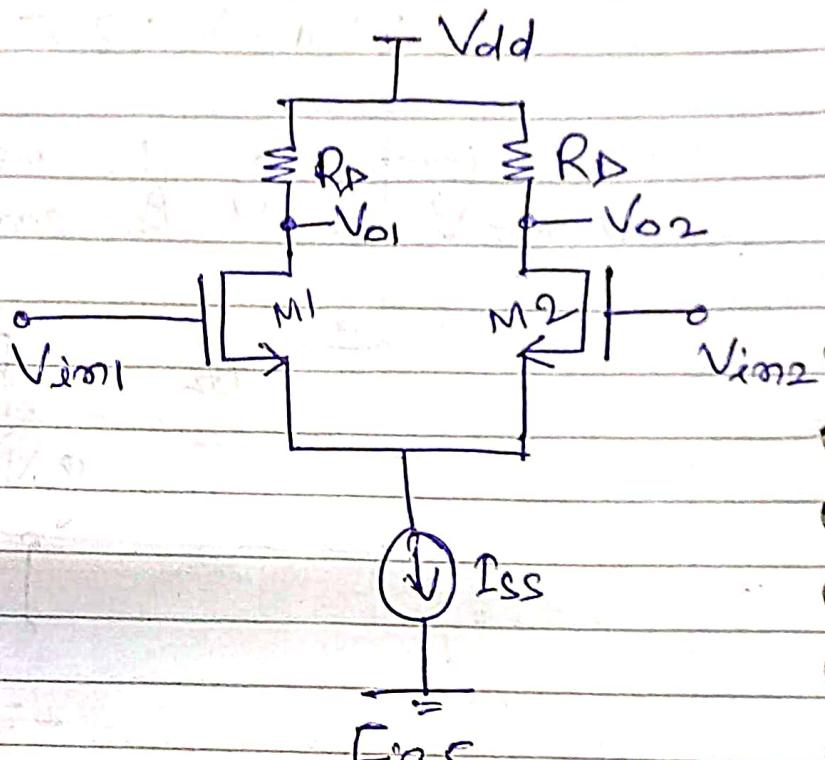


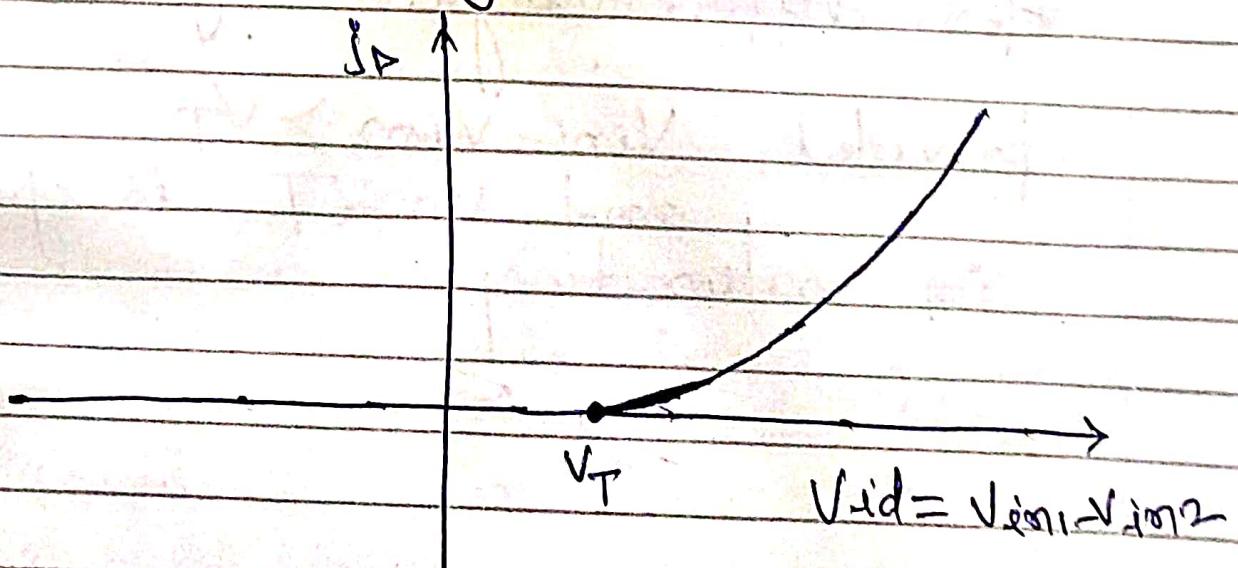
Fig 5

For Fig 4

~~$I_D = \frac{V_{DD}}{R_D}$~~

$$I_D = K_m (V_{in1} - V_{in2} - V_T)^2$$

Here, plotting I_D w.r.t $V_{in1} - V_{in2}$



Now for Figs.

$$\begin{aligned} j_{D1} &= K_m (V_{ns1} - V_T)^2 \\ j_{D2} &= K_m (V_{ns2} - V_T)^2 \end{aligned} \quad \left\{ \begin{array}{l} V_{T1} = V_{T2} = V_T \\ K_{m1} = K_{m2} = K_m \end{array} \right. \quad \text{Since } M_1 \text{ & } M_2 \text{ are matched.}$$

$$j_{D1} + j_{D2} = I_{SS} \quad \text{--- (1)}$$

$$\sqrt{j_{D1}} = \sqrt{K_m (V_{ns1} - V_T)}$$

$$\sqrt{j_{D2}} = \sqrt{K_m (V_{ns2} - V_T)} \quad \text{--- (2)}$$

$$\sqrt{j_{D1}} - \sqrt{j_{D2}} = \sqrt{K_m [V_{ns1} - V_{ns2}]}$$

$$\therefore V_{ns1} - V_{ns2} = V_{im1} - V_{im2} = V_{id}$$

$$\sqrt{j_{D1}} - \sqrt{j_{D2}} = \sqrt{K_m V_{id}} \quad \text{--- (2)}$$

Squaring both sides

$$\underbrace{j_{D1} + j_{D2} - 2\sqrt{j_{D1} j_{D2}}}_{I_{SS}} = K_m V_{id}^2$$

$$\therefore 2\sqrt{j_{D1} j_{D2}} = I_{SS} - K_m V_{id}^2$$

$$j_{D2} = I_{SS} - j_{D1}$$

$$\therefore 2\sqrt{(j_{D1})(I_{SS} - j_{D1})} = I_{SS} - K_m V_{id}^2$$

By solving,

$$j_{D1} = \frac{I_{SS}}{2} \pm \sqrt{\frac{I_{SS}}{2} \left(\frac{V_{id}}{2} \right)^2} \cdot \sqrt{1 - \frac{(V_{id}/2)^2}{I_{SS}/2}}$$

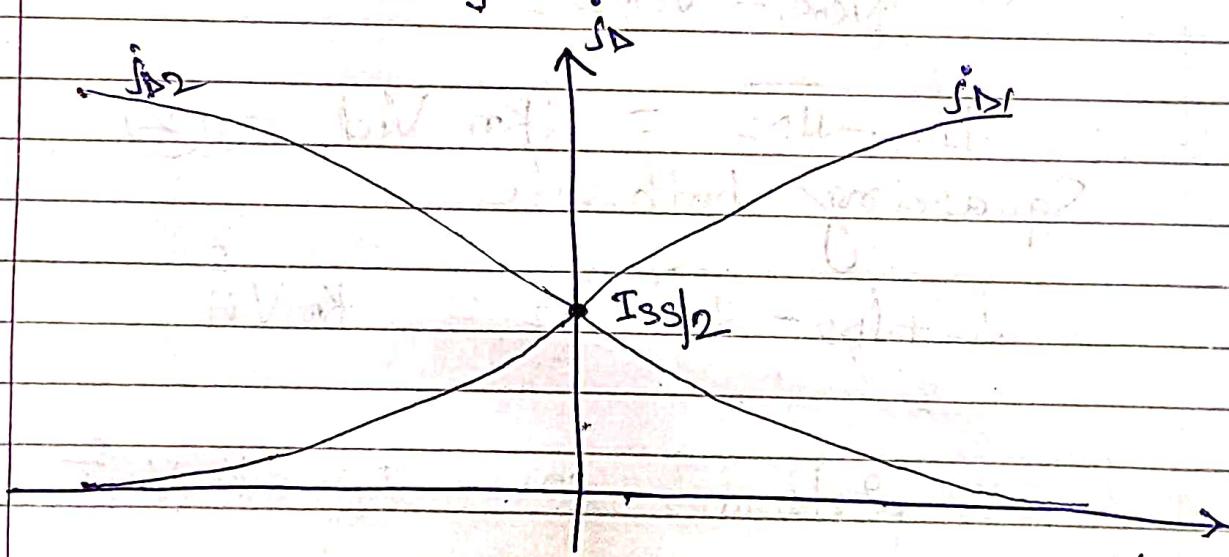
Since, only one root is valid.

$$\therefore j_{D1} = \frac{I_{SS}}{2} + \sqrt{2KmI_{SS}} \left(\frac{V_{id}}{2} \right) \sqrt{1 - \frac{(V_{id}/2)^2}{(I/2Km)^2}}$$

We have taken only positive root which is valid, since the current j_{D1} above bias point ($I_{SS}/2$) must have the same polarity as V_{id} .

$$j_{D2} = \frac{I_{SS}}{2} - \sqrt{2KmI_{SS}} \left(\frac{V_{id}}{2} \right) \sqrt{1 - \frac{(V_{id}/2)^2}{(I/2Km)^2}}$$

The plot of j_{D1} vs V_{id} & j_{D2} vs V_{id} will be as follows



1 → Here, we see that, for $V_{id} = 0$, that is for common mode input

$$j_{D1} = j_{D2} = I_{SS}/2$$

& hence differential output = $V_{o1} - V_{o2} = 0$

However, that can not be achieved.

~~For Fig 4.~~

→ The circuit of Fig 5 can operate in both the conditions when $V_{id} > 0$ or $V_{id} < 0$. There will be the respective modifications in the J_{A1} and J_{A2} however for fig 4 the circuit will only work when $V_{id} > V_T$. This is not a proper differential behaviour.

Hence based on these basic conclusions we can say that circuit in Fig 5 is more superior than fig 4.

Q (3) (c)

Since,

$$P_L = \frac{1}{2} \frac{V_o^2}{R_L}$$

$$\left\{ \begin{array}{l} V_o = (V_b)_{RMS} \end{array} \right\}$$

$$(V_b)_{RMS} = \sqrt{2 P_L \cdot R_L}$$

$$= \sqrt{2 \times 80 \times 8}$$

$$\therefore V_o = 17.9V$$

According to question

$$\therefore V_{cc} = V_o + 5$$

$$\boxed{V_{cc} \approx 23V}$$

Now, max^{“on”} power that the BJTs can tolerate is

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$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L}$$

$$= \frac{(23)^2}{\pi^2 \times 8} = \underline{\underline{6.7 \text{ W}}}$$

Q4. For the circuit given in Figure 5, MOSFET (NMOS) has, $\mu_nC_{ox} = 100 \mu\text{A/V}$, where μ_n is the electron mobility in the channel and C_{ox} is the oxide capacitance per unit area, the threshold voltage $V_t = 1 \text{ V}$, and aspect ratio (W/L) = 10. Channel length modulation effects are negligible ($\lambda = 0$).

- (a) Find the range of R_1 (approximate values up to one decimal place), such that Branch 1 (as indicated in the circuit) will act as a potential divider. The MOSFET-related error should be kept approximately within the 10% range. **[15 Marks]**
- (b) Given $R_1 = 1\text{K}$, find the value of R_2 such that $V_a = V_b$. **[10 Marks]**

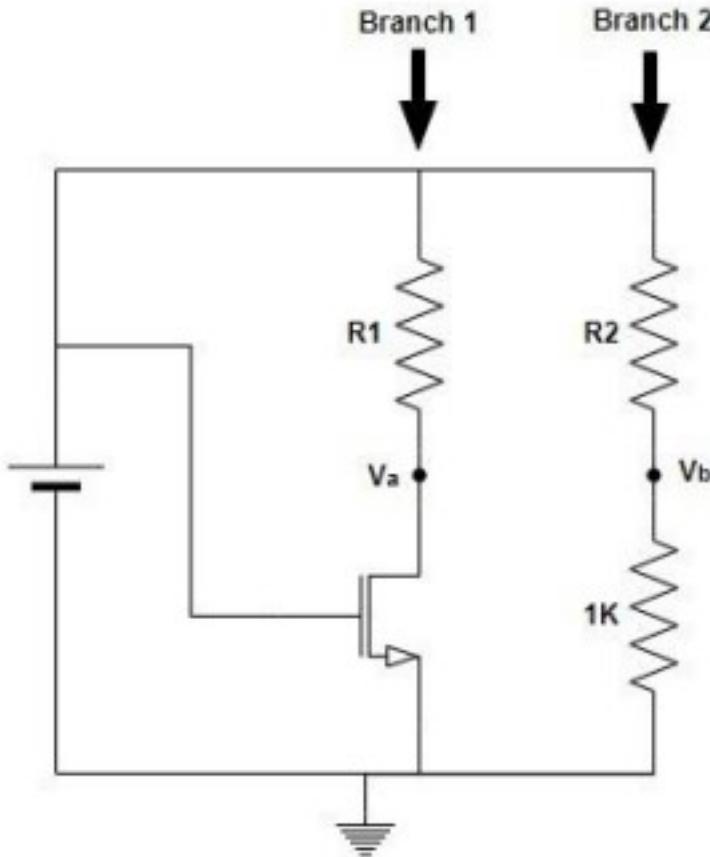
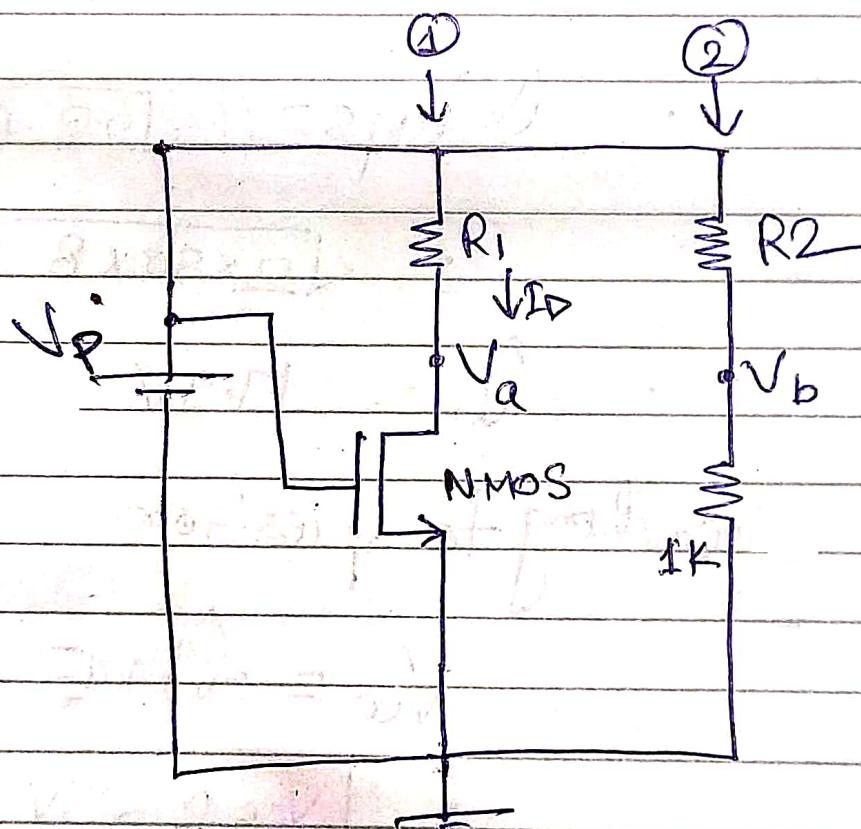


Figure 7

Q. (4)



(a) Here in the question supply voltage is not given we will assume it to V_p .

Now branch 1 will act as a potential divider when NMOS will operate in triode and for smaller V_{DS} I_D vs V_{DS} relation can be approximated to,

$$I_D = n_m \mu_0 C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T) V_{DS}$$

$$\therefore V_S = 0$$

$$\therefore I_D = 10^{-3} (V_p - 1) V_D = 10^{-3} (V_p - 1) V_D$$

$$\text{Also, } \therefore I_D = \frac{V_p - V_D}{R_1}$$

$$\therefore \frac{V_p - V_D}{R_1} = 10^{-3} (V_p - 1) V_D$$

$$V_p - V_D = 10^{-3} V_p R_1 V_D - 10^{-3} V_D R_1$$

$$\therefore V_D \left(1 + 10^{-3} V_p R_I - 10^{-3} R_I \right) = V_p$$

$$\therefore V_D = \frac{V_p}{1 + 10^{-3} V_p R_I - 10^{-3} R_I} \quad \text{(1)}$$

Now ~~need~~ to maintain error within 10%.

$$V_D < \frac{V_{p-1}}{5} < \cancel{\frac{V_p}{10}} \quad \frac{V_{p-1}}{5}$$

$$\frac{V_p}{1 + 10^{-3} V_p R_I - 10^{-3} R_I} < \frac{V_{p-1}}{5} \quad \{ \text{by (1)} \}$$

$$\therefore 5V_p < (V_{p-1}) (1 + 10^{-3} V_p R_I - 10^{-3} R_I)$$

$$\therefore 5V_p < (V_{p-1}) + R_I [V_p^2 \cdot 10^{-3} - 2 \times 10^{-3} V_p + 10^{-3}]$$

$$R_I \times 10^{-3} [V_p^2 - 2V_p + 1] > (4V_p + 1)$$

$$\text{or, } R_1 > \frac{4V_p + 1}{(V_p - 1)^2} \times 10^3 \text{ Ohm}$$

Hence for the branch to act as PP
 V_p should be chosen such that $V_p > V_T$
and R_1 should satisfy the above
condition for a given V_p .

Q.(4)(b) Since both the branches
are acting as potential dividers

$$\text{for } V_a = V_b$$

$$\frac{R_1}{R_{DS}} = \frac{R_2}{1K} \quad \left. \begin{array}{l} \text{Balance bridge} \\ \text{or } R_1 = R_2 \end{array} \right\}$$

$$\therefore R_{DS} \approx \frac{1}{10^3 \cot \frac{\omega}{L} (V_{BS} - V_T)} \quad \left. \begin{array}{l} \text{within} \\ 10\% \text{ error} \end{array} \right\}$$

$$\therefore R_{DS} = \frac{1}{10^3 (V_p - 1)}$$

$$\therefore \frac{R_1}{10^3 (V_p - 1)} = \frac{R_2}{1K}$$

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$$\therefore R_2 = \frac{1K \times 1K}{10^3(V_p - 1)}$$

∴ $R_2 = \frac{10^9}{V_p - 1} = \left(\frac{1000}{V_p - 1} \right) \text{ MN}$

Here, we see that since ~~R_{D2}~~ R_D is small hence for the circuit to act as a balance bridge R_2 will be very large.