DVD Monsoon 2025: Review Quiz-2

Total points 8/10

Quiz Instruction

1. The test will be live from 4:00 PM to 7:00 PM.
2. You must submit your response before 7:00 PM; no responses will be accepted afterward.
3. Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
4. Only one attempt is allowed per student.
5. You must attempt the quiz using your college email ID.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

✓ How BIST is helpful in designing more testable designs? 1/1

- [x] It offers at-speed testing. ✓
- [x] It enables on-site testing. ✓
- [ ] It helps reduce the die's area, further increasing testability.
- [x] It helps to reduce chip cost by reducing test cost. ✓

Feedback

Testing at Speed: Memories, in particular, can operate at very high speeds (gigahertz), while traditional testing methods are much slower (around 100 megahertz). BIST allows testing at the memory's operational speed, ensuring performance is verified under realistic conditions. Slower testing methods would be insufficient and time-consuming for large memories.

Reduced Test Time and Cost: The combination of speed and parallel testing leads to a significant reduction in the time required for testing. This translates directly into lower costs associated with testing.

BIST enables on-site testing by embedding test generation and analysis logic directly into the chip, so the IC can test itself without external equipment and allowing self-checks in the field.

Roll Number *

2023024

✗ Why is self-aligned polysilicon important in MOSFET fabrication 0/1

- [x] It allows a much better yield than earlier processes. ✓
- [x] It improves the switching speed of the devices. ✗
- [x] The process minimizes variability and allows for smaller transistor geometries, which is crucial for scaling. ✓
- [ ] It helps in increasing the parasitic capacitances.

Correct answer

- [x] It allows a much better yield than earlier processes.
- [x] The process minimizes variability and allows for smaller transistor geometries, which is crucial for scaling.

Feedback

The self-aligned polysilicon gate process in VLSI offers several key advantages.

It enables the creation of source and drain regions with high precision by using the polysilicon gate itself as a mask during ion implantation, ensuring that the source and drain are perfectly aligned with the gate edges.

This self-alignment significantly reduces parasitic capacitance, particularly the gate-to-drain capacitance (Cgd), which is a major factor in limiting switching speed due to the Miller effect.

Full Name *

Abhinav Maurya

✓ **As MOSFETs are scaled down, short channel effects become dominant. FDSOI technology is used to mitigate these effects and improve performance. How does FDSOI help in reducing short channel effects?** 1/1

- [x] FDSOI reduces short channel effects due to its ultra-thin body and buried oxide. ✓
- [x] FDSOI allows dynamic tuning of threshold voltage using body biasing. ✓
- [ ] FDSOI increases junction leakage compared to bulk CMOS.
- [ ] FDSOI has weaker electrostatic control of the channel compared to bulk CMOS.

Feedback

1. In an FDSOI device, the silicon region deep beneath the gate, which is typically difficult for the gate to control, is replaced with a buried oxide layer. Consequently, this poorly controlled region is effectively removed, making that part of the FD-SOI FET inactive.

Effects:
** Better short-channel characteristics*
** Sharper subthreshold swing*
** Lower OFF-state current*

2. The presence of the buried oxide allows for the application of biasing voltages to the substrate, which acts as a back gate. Dynamic control of the transistor's threshold voltage can be achieved using this substrate bias.

✓ Why do we rotate the substrate by 45 degrees during the fabrication of devices

1/1

- [ ] It improves current through PMOS and NMOS devices.
- [x] It improves current through only PMOS devices, and current through NMOS devices remains unchanged. ✓
- [ ] There are two types of holes in Si: light holes and heavy holes. The mobility of light holes depends on crystal orientation.
- [x] There are two types of holes in Si: light holes and heavy holes. The mobility of heavy holes depends on crystal orientation. ✓

Feedback

NMOS devices rely on electrons, whose mobility is nearly isotropic, so rotation does not affect NMOS current.

In PMOS devices, holes exist as light holes and heavy holes. The light-hole mobility strongly depends on crystal orientation.

By rotating the substrate by 45°, the PMOS channel is aligned with the direction of higher light-hole mobility, which improves the drive current of PMOS devices while NMOS current remains unchanged.

✓ In a MOSFET fabricated at a 100 nm technology node, due to a process that causes the increase of length of the gate by **x** nm(not percentage-based), the drive current is measured as 80μA. When the same absolute error x occurs at a reduced channel length of 30 nm, the drive current increases to 240 μA. What is the error x? 2/2

[Assume only the length of the change in other parameters remains unchanged]

Note: Answer should be in "**nm**". Please don't write unit in the answer.

5 ✓

Feedback

We use the model
Leff =L+x
ID ∝ 1/Leff

For L = 100nm For L = 30nm

I1 = 80μA = k/(100 + x)
I2 = 240μA = k/(30 + x)

Taking ratio:
I2/I1 = (100 + x)/(30 + x) 3 = (100 + x)/(30 + x) 240/80 = (100 + x)/(30 + x)
x = 5 nm

✓ **A wafer can have 100 dies with area A and yield Y, and if you reduce the die area to A/2, what is the new yield? (with same defectivity)** 1/1

- [ ] 1.5Y
- [ ] 20Y
- [ ] 50Y
- [x] 2Y ✓

Feedback

Yield is inversely proportional to area; yield increases as the die's area reduces.

✓ **The different nodes of the *"virtuous cycle"* that benefit the VLSI industry include** 1/1

- [x] Integration ✓
- [x] Performance ✓
- [x] Cost ✓
- [ ] Time to Market

Feedback

Moore's law ensures the benefit of integration and price/cost
Pollack's rule establishes the relationship between integration and performance
Dennard's scaling enables improvement in both performance and cost

✓ How does a cleanroom help in improving the yield of devices? 1/1

- [x] A dust particle can result in an open circuit of wire. ✓
- [x] A dust particle can result in a short circuit of a wire. ✓
- [ ] A particle in the air can affect the machines used for fabrication.
- [ ] A cleanroom increases the oxidation rate of silicon during thermal processing.

Feedback

If a dust particle settles on a wafer during lithography or deposition, it can block the formation of a metal line, leading to an open circuit.

If a dust particle causes unintended bridging between two adjacent metal lines, it can create a short circuit, making the device non-functional.

Cleanrooms are primarily designed to protect wafers from defects, not to protect the machines. While contamination can indirectly affect equipment performance, the yield improvement mainly comes from preventing defects on wafers, not machine failure. (Partially correct but not the main reason)

Cleanrooms control dust, humidity, and particle count, but they do not affect the oxidation rate of silicon. Oxidation depends on furnace conditions (temperature, oxygen flow, pressure), not the cleanliness of the air.

✗ You are tasked with designing a memory chip of 16 GB capacity. 0/1

Scenario A: A single large die of 16 GB is fabricated.

Scenario B: Instead of one large die, multiple smaller dies are fabricated. Assuming 1 GB is the optimal die size for best yield, you can fabricate 16 dies of 1 GB each and integrate them.

Now for better yield we will go with **Scenario B:**

Part A: *The 16 dies are combined into a single package using multi-die packaging.*

Part B: *The 16 dies are packaged separately as individual 1 GB chips.*

Question:
Why is multi-die packaging (Part A) preferred over packaging all dies separately (Part B)?

- [x] Form factor is optimized. ✓
- [x] Inter-die delays are minimized ✓
- [ ] Better Thermal Distribution
- [ ] Decreased Packaging Complexity and cost

Correct answer

- [x] Form factor is optimized.
- [x] Inter-die delays are minimized
- [x] Better Thermal Distribution

Feedback

Multi-die packaging allows stacking or side-by-side placement, keeping the package compact even with multiple dies.
Heat is spread across multiple smaller dies, avoiding concentration in one very large die, making thermal management easier.
Multi-die packaging actually increases packaging complexity (bonding, stacking, interposer connections).

If you package all 16 dies separately (Part B), they must be connected externally on a PCB or system board. This means signals have to travel through longer interconnects, resulting

in higher delay and power consumption. Also, cost of a larger PCB and more work during assembly makes the option undesireable.

In multi-die packaging (Part A), the dies are integrated inside a single package, connected through short, high-bandwidth interconnects (wire-bonds, TSVs, interposers). This minimizes inter-die delays compared to packaging them separately.