DVD END-SEM 2021 RUBRICS

Q1. Give reasons for the following questions briefly: (1*3 = 3 Marks)

a). Use of strap cells for making layouts?

b). Leaving ½ DRC spacing while designing layouts in standard cell topology?

c). Width of the standard cell is a multiple of 0.2 in the 12T library?

Ans:

a). Strap cells are used for connecting the VDD and GND at regular intervals (substrate connection). This will avoid the positive feedback where the low impedance path forms (Rwell, Rsub) known as latchup. If latchup is not avoided it can lead to internal junction breakdown.

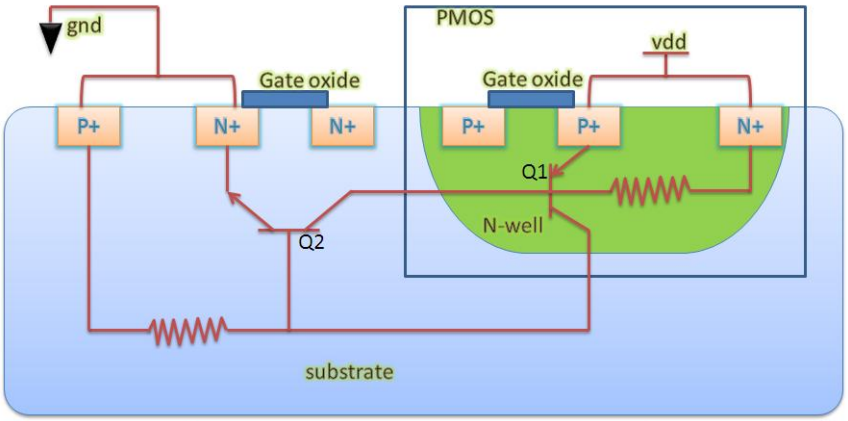


Figure 1 : Latchup formation in a CMOS device

Source: Wikipedia

b). In standard cell topology, one cell is abutted with another cell. Now if one leaves ½ the minimum DRC requirement across cell sharing, then after abutment, 1 full DRC is met. This will enable abutting cells at minimum possible spacings saving the area and time/effort to make DRC clean layouts.

c). When the Metal-3 (M3) layer is used in standard cells, it is typically drawn vertically over the cell, and hence the width of the cell is governed by the pitch of the M3 layer. The pitch of the M3 layer is equal to the **metal track width + 2*(1/2DRC)**. Hence the pitch is **0.2um**. Therefore the width of standard cells is in multiples of M3 pitch.

Each part carried 1 mark. If the answer was partially correct then 0.5 marks were awarded.

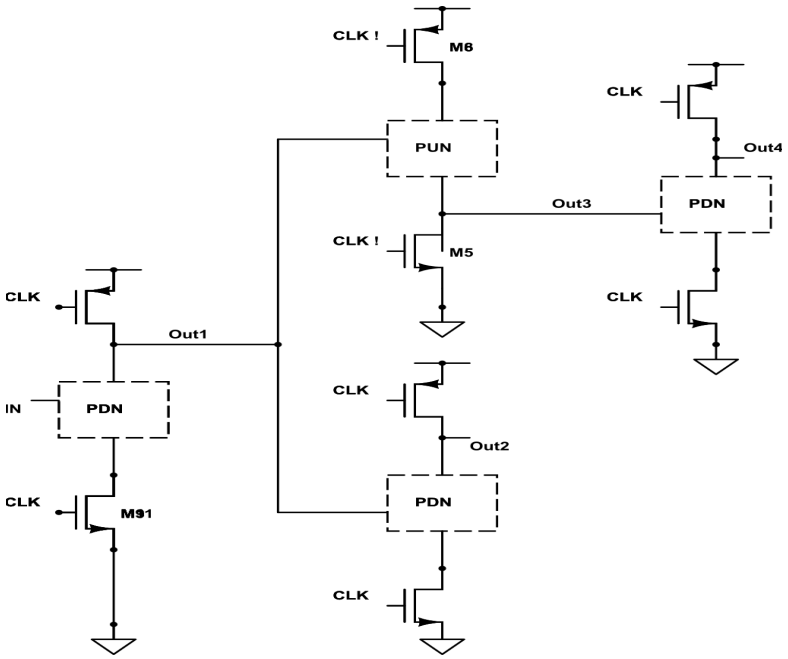
Q2. Fill in the Table: Explain the impact of the following manufacturing events on drain current for a given gate-source voltage of an N-MOSFET? (1*4 = 4 Marks)

Ans: This question can be solved by considering the current equation for an n-MOSFET and analysing the impact of different parameters on the drain current of the device.

Events	Impact on I_{DS}	Explanation
Growth of thicker gate oxide	Decrease	Tox is inversely proportional to current as Cox reduces / Vth Increases.
Extra poly etching	Increase	Gate length has been reduced due to extra removal of poly. The channel length is inversely proportional to the drain current.
Extra etching of oxide when creating windows for source/drain implants	Increase	The extra etch on S/ D windows will lead to a bigger source and drain. This will increase the width and hence the current.
HfO_2 is used as dielectric rather than SiO_2	Increase	The dielectric constant of HfO_2 is ~16.6 compared to 3.9 for SiO_2. Hence Cox is larger when HfO_2 is used. Current is directly proportional to Cox.

Each part carries 1 mark. 0.5 for mentioning the impact and 0.5 for the explanation.

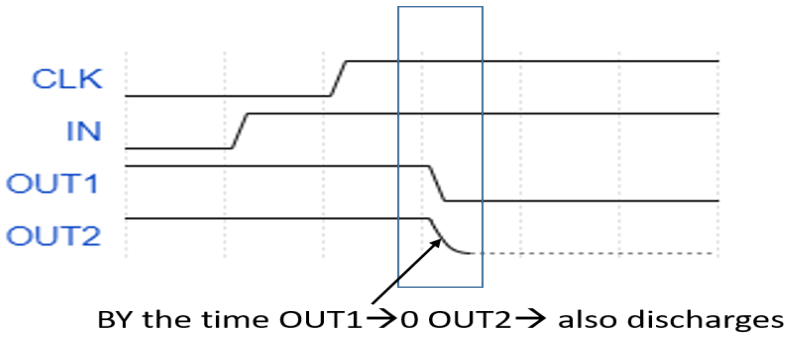
Q3. Consider the circuit given below. Pull-down/Pull Up network can be considered as a single NMOS/PMOS device. Assume that evaluation time, precharge time & propagation delay all are T/2.(CLK! is the inverse of CLK) (6 Marks)



a) **Detect the problems in the circuit during 1->0 & 0->1 transition (if any).If any problem exists how do you resolve it by inserting one inverter somewhere in the circuit.** **[2 Marks]**

Solution:

There is no problem if the input makes a 1->0 transition, as long as the input is stable when the evaluation phase begins. However, if the input makes a 0->1 transition, Out1 will initially be precharged to 1 and then go to 0 at some time after the evaluation phase begins. In our case this time is T/2. This could allow the next PDN to pull Out2 low before Out1 goes low and cause



an error in Out2. as shown below. Insert the inverter before the PDN generating Out2 to solve the problem.

b) **For the corrected circuit draw the timing diagram for Out1, Out2, Out3, Out4. Assume a clock period of 10T and the IN signal goes high before the rising edge of CLK.**

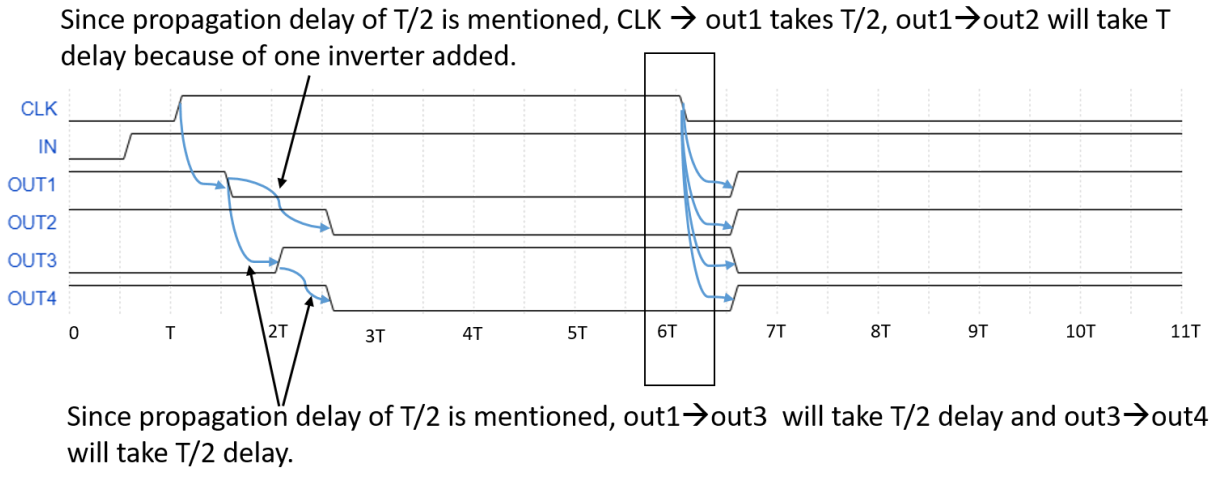
[4 Marks]

Solution:

when the IN signal goes high before the rising edge of the clock CLK. Assume that the clock period is 10 T time units.

(Marks distribution)

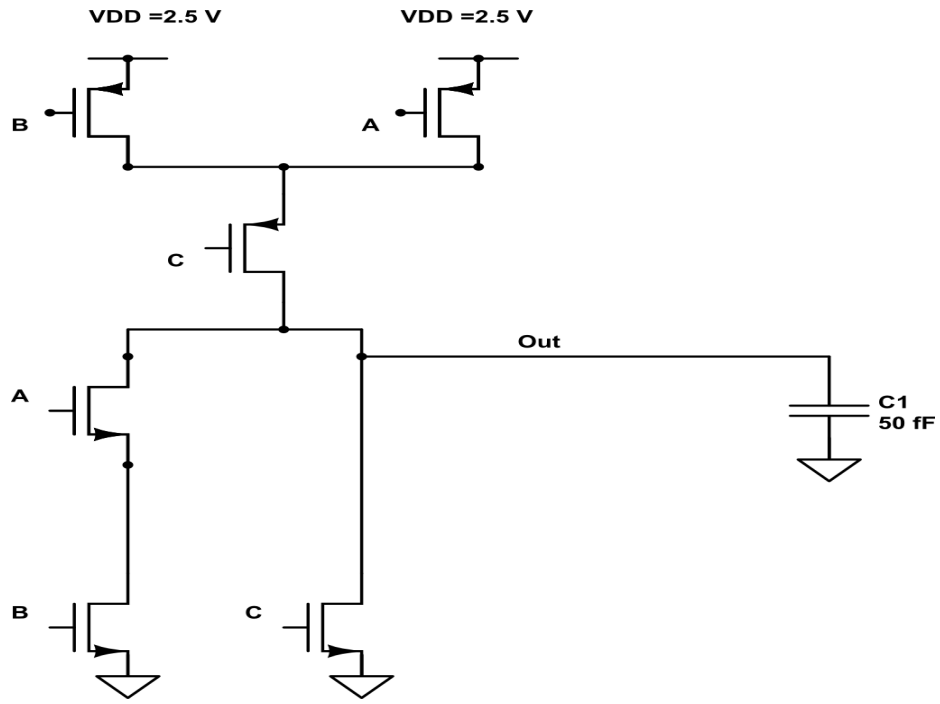
Each output waveform is 1 mark, (0.5 mark for delay + 0.5 mark for correct waveform)



At t=6T, every output is either at the pre-charged or discharged stage with a delay of T/2

Q4: Consider the circuit shown below

a) **What is the logic function implemented by the circuit? (1)**
b) **What input vectors will cause the worst leakage power for both HIGH & LOW output values? (1)**
c) **Consider the Probability of each input = 0.5 and every input is independent. What will be the activity factor of the circuit? (2)**
d) **Calculate the dynamic power of the circuit if the input frequency is 100MHz? (1)**

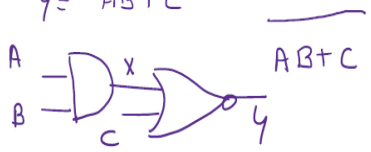


Ans:

a) ((AB)+C)'
b) When the output is high, the worst-case leakage occurs when two transistors leak in parallel: ABC = 100 or 010. When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: ABC =110. At these combinations, Vds is highest.

c)

c) ① $Y = \overline{AB + C}$



$P(A) = 1/2 \quad P(B) = 1/2 \quad P(C) = 1/2$

$P(X) = P(A) \times P(B) = 1/4$

$P(Y) = \overline{P(X)}\,\overline{P(C)} = 3/4 \times 1/2 = 3/8$

$\alpha_Y = (1 - P(Y)) \times P(Y)$

$= \frac{5}{8} \times \frac{3}{8} = \frac{15}{64}$

②

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$P(Y) = 3/8$

This method to calculate P(Y) at output is more accurate as well as easy to follow.

d)

d) Dynamic Power $= \alpha C V_{DD}^2 f$

$= \left(\frac{15}{64}\right) \times (50 \times 10^{-15}) \times (2.5)^2 \times 100 \times 10^6$

$= 7.03\ \mu W$

Q5: Which circuit (between fig1 and fig2) will you prefer for designing the latch? Why? If you use a tristate buffer, which input (CLK or out) will you apply as the inner input and why? (0.5+1.5+2)

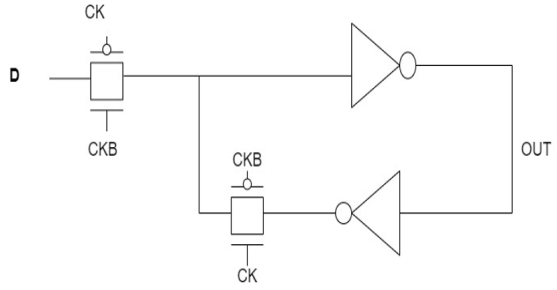


Fig-1

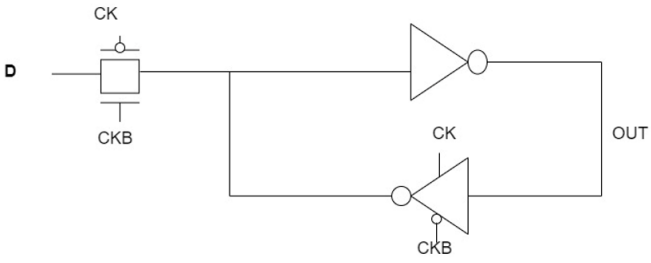


Fig-2

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Solution: We will prefer the design used in fig-2.

Reason:

- Tristate buffer is preferred over the inverter+ transmission gate design because, if the input at D is toggling continuously , then that will be propagated to OUT and eventually the inverter will unnecessarily waste power due to continuous charge and discharge. This can be avoided by using a tristate buffer.

- By using a tristate buffer, we will use the devices in stacking which will reduce the leakage.
- Also, using tristate logic, we can make the design more compact.

Part 3: We have shown 2 figures below which are electrically equivalent. But fig 4 is inferior design compared to fig 3 because, if the OUT is toggling when the latch is in opaque, it can cause charge sharing noise on the output node (here ‘X’).

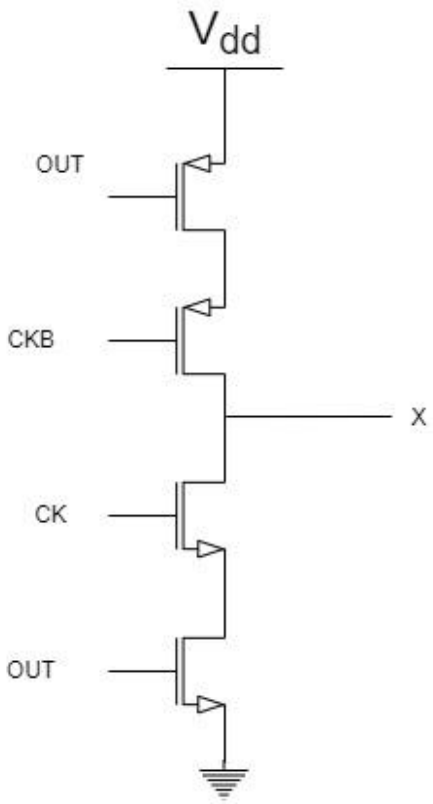


FIG-3

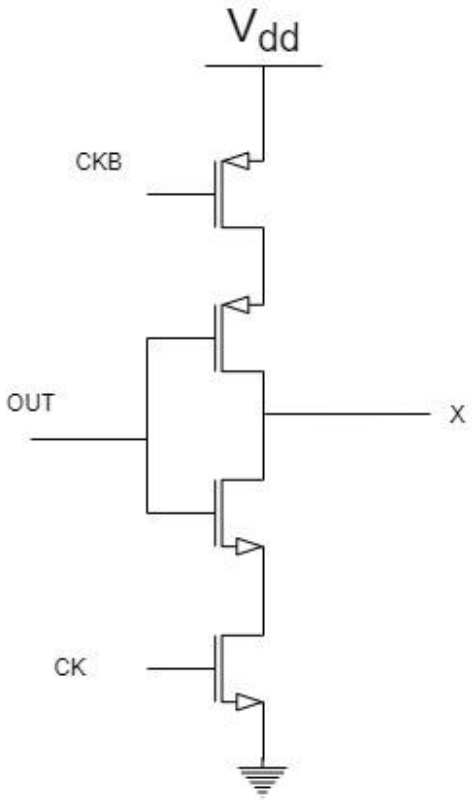
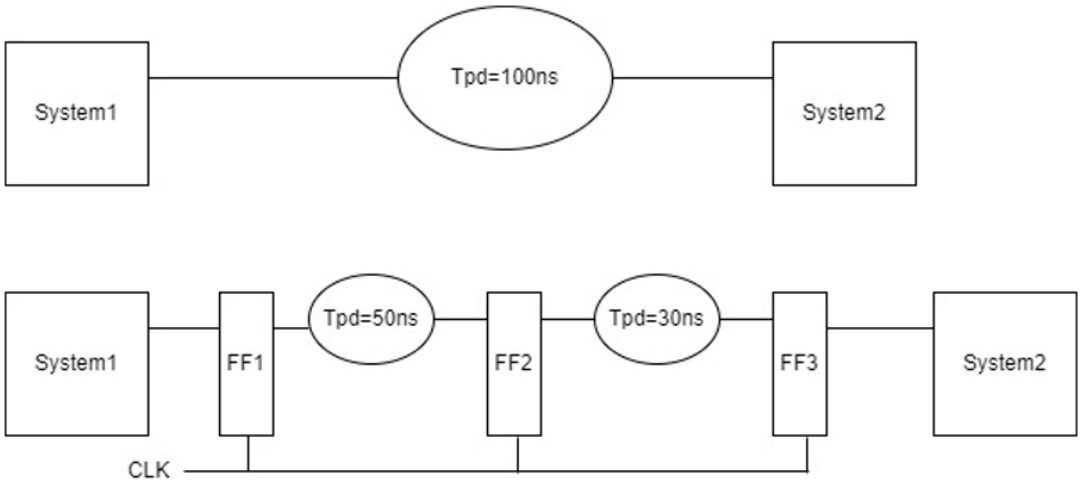


FIG-4

Q6: What do you mean by sequencing overhead? Why does FF need to satisfy setup time and hold time constraints? (1+2)

Solution:

Part1: In order to improve the throughput of a system and ensure sequencing, we use pipelining by breaking complex logic into smaller circuits. In a pipeline, we expect that the overall clock time period is utilized to evaluate the combinational logic block. Whereas in order to send the data properly to the next stage, the effective clock time period needs to satisfy the following condition: $T_{clk} >= T_{pcq}+T_{pd}+T_{setup}$ This ($T_{pcq}+T_{setup}$) delay is known as sequencing overhead since it adds extra delay to a slow token where Tpcq is the propagation clock to Q delay and Tpd is the combinational logic delay in the datapath.



If Tpcq= 3ns

Tsetup=2ns

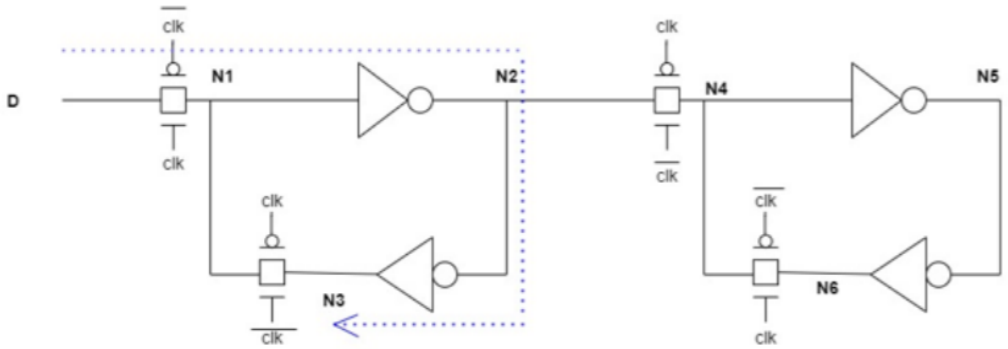
On that case the Tclk has to be >= 55ns

Therefore the delay from system1 to system 2 will become 110ns

This increase in 10ns is due to sequencing and is known as the sequential overhead

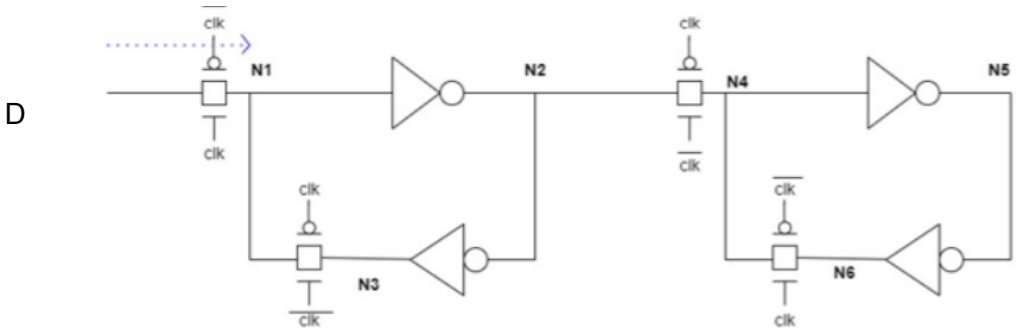
Part2: Why setup time?

When the clock (CLK) is low, input D follows the path D->N1->N2->N3 and reaches the input of TG2. This time is known as the setup time of a flop. If data changes within this time, the data won't be able to reach the input of TG2 and when TG2 turns on, it might be two different data reaching node N1, which can cause metastability, glitch at the output and therefore dissipate extra power.



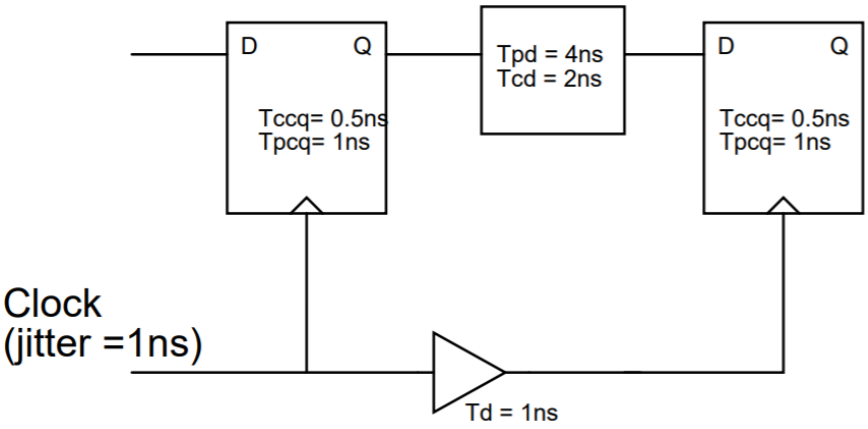
Why hold time?

Hold time arises because of the finite delay between the clock and clock_bar signals which control the switching of transmission gates. The transmission gate takes some time to switch on or off, which is known as the hold time of a flop. So it is necessary to maintain a stable value at D pin to ensure a stable value at node N1 (from the first transmission gate) which is translated to output.



Note: Defining setup time and hold time was not the question. 0.5 marks have been awarded for that.

Q7. For the circuit shown below calculate the setup and hold slack for a clock period of 10ns. Both the flops have setup and hold time of 2ns and 1 ns respectively. (2 Marks)



Note: Slack is the extra time/margin available after meeting the setup or hold requirement.

Soln:

Arrival Time (AT) is the time at which **data arrives** the D pin of the capture flop measuring from the clock edge.

Required Time (RT) is the time at which **data should be present** at the D pin of capture flop measuring from the clock edge, to prevent any setup or hold violation.

For Setup check

AT = 1 (for jitter) +1 + 4 = 6ns

RT = 10 + 1 (for buffer) - 1 (for jitter) - 2 (for setup) = 8ns

Setup slack = RT-AT=8 - 6 = 2 ns

For hold check

Jitter not to be considered for hold because the same clock edge is taken for launch and capture flop .However, for setup subsequent edges are taken.

AT = 0.5 +2 =2.5 ns

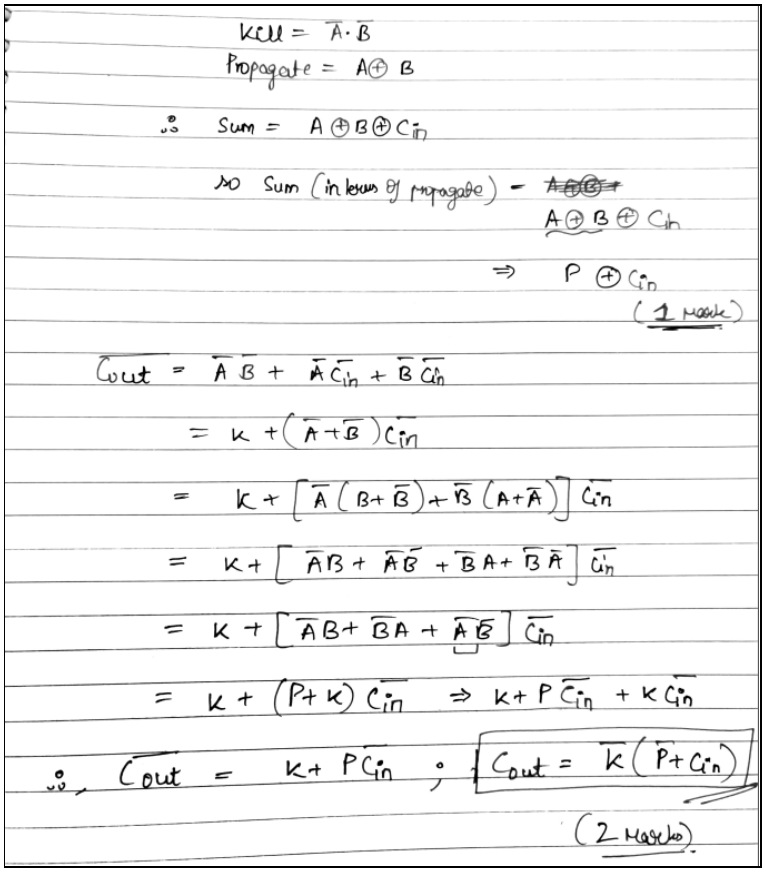
RT = 1 + 1 (for hold) = 2ns

hold slack = AT-RT = 0.5 ns

[Both Setup and Hold check 1 marks for correct expression and 1 marks for final answer]

Q8. It is given that the Kill signal = A'.B' and the Propagate signal = A xor B for a full adder. Represent Sum and Carry-out in terms of Kill & Propagate (instead of Generate & Propagate)? (3 Marks)

Ans:



1 mark for writing the sum & 2 marks for finding the Carry_out. NOTE: There can be other techniques also to arrive at the answer of Carry_out.

Q9. (bonus) (3 Marks)

Electromigration (EM) is a failure mode in which high current density could lead to defects, voids in metal interconnects. Since the thickness of wires is already fixed for a given technology, a designer can only change the width of the wire to reduce current density and prevent EM. Assume that the EM limit is J_{AL} = 1.0 mA/um (J_{AL} should not be higher than this, o/w failure would occur) and VDD = 1.8 V.

1. Find the required widths of power and ground wires connected to a 500 MHz clock buffer that drives 5pF on-chip capacitance. (2 Marks)

2. Suppose that the clock buffer is 400um away from both the power and ground pads. The rise and fall times of the clock are the same and equal to 200 ps. What is the ground bounce with the chosen size of wire? Assume wire resistance to be 57 mOhm/square. (1 Marks)

Ans:

1. We have the power dissipation of the clock buffer

$P = C_L V_{DD}^2 f$
$= 5*10^{-12} *1.8^2* 500 *10^6$
$= 8.1$ mW {0.5}

The current from the power supply pad is found to be
$I = 8.1$ mW/1.8 V = 4.5 mA {0.5}

Width of the wire = $(I / J_{AL}) = 4.5$um {1}

Hence, the width of power-supply wires for the clock buffer should be at least 4.5um.

2.
The resistance of wire would be
$R = (400/4.5)*57*10^{-3}$
$= 5.06$ ohm {0.5}

The IR drop on the power supply-wire is
$V = IR = C_L(dV/dt)*R = 5 *10^{-12} *(1.8/0.2*10^{-9})*5.06 = 227.7$ mV {0.5}

which may be intolerable in some applications. To reduce the ground bounce, the power-supply wire should be widened so as to reduce its resistance.