VLSI Design Flow (ECE313/ECE513)

End Semester Exam (8th December 2025)

Time allowed: 2 hours *Maximum Marks: 80*

Note:

I. ***There are five printed pages in this question paper. Check if you have all of them.***
II. ***Marks are indicated in bold at the end of each question.***
III. ***There are 5 questions of 14, 14, 17, 17, and 18 marks. All questions are compulsory.***
IV. ***Be crisp and precise in your answer so that you can complete the answers in 2 hours.***
V. ***Calculator and other electronic gadgets are NOT allowed in the exam.***
VI. ***Cheating or using unfair means will be dealt with as per institute policy.***

1.

a. With respect to photolithography, answer the following questions:
- i. What is the role of a photomask?
- ii. How is developer used in photolithography?
- iii. What is optical proximity correction (OPC)?
- iv. What is a pellicle used for?

[1+1+1+1=4 Marks]

b. With respect to design styles and methodologies, answer the following questions:
- i. Name the design style that employs a library of standard logic cells, and that are placed and routed automatically.
- ii. What is a full-custom design?
- iii. What is a synchronous design?
- iv. What do you understand by IP assembly?

[1+1+1+1=4 Marks]

c. With respect to manufacturing and test of integrated circuit, answer the following questions:
- i. What is a test vector from the perspective of manufacturing test?
- ii. Name the process that classifies the manufactured chips based on measured performance.
- iii. Name the packaging method in which an IC is mounted *face-down* onto the substrate using tiny solder bumps instead of wire bonds.
- iv. Name the process that performs stress testing on chips under high temperature and voltage to detect infant mortality (early failures).

[1+1+1+1=4 Marks]

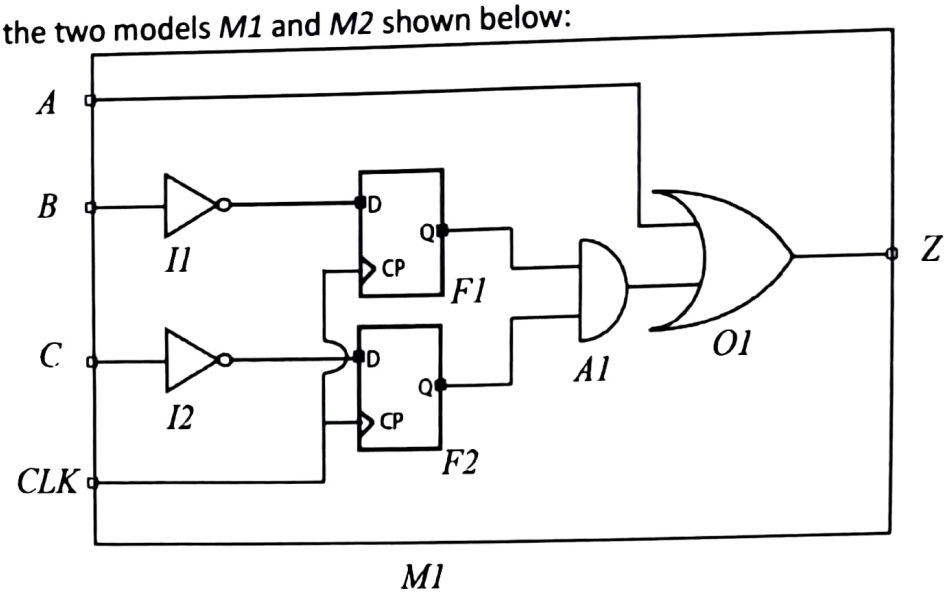
d. A polysilicon layer has a resistivity of 2×10^{-4} Ω·cm and is deposited with a thickness of 0.25 µm.
- i. Compute the sheet resistance of the layer.
- ii. If a rectangular polysilicon resistor is designed with a length-to-width ratio (L/W) of 12, find the total resistance.

[1+1 Marks]

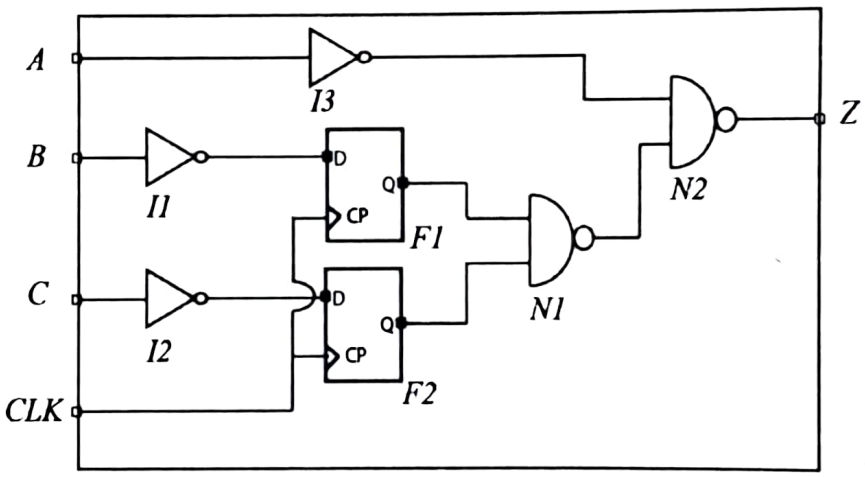
2.

a. Draw the Reduced Ordered Binary Decision Diagram (ROBDD) of the function $y = a'b'c'$ with the variable order a, b, and c. Label the ROBDD appropriately. **[4 Marks]**

b. Consider the two models *M1* and *M2* shown below:



M1



M2

These two models are subjected to combinational equivalence checking (CEC). The ports and registers are matched by names.

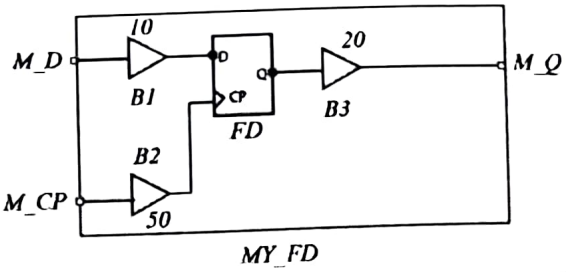
i. Draw the schematic of the miter circuit for the compare point output port Z that the CEC tool will internally create. Label the ports and instances (no other label needed). Mark the elements that are created due to model *M1* as *M1.A1*, *M1.O1* etc. and that created due to *M2* as *M2.N1*, *M2.N2* etc.

ii. Draw the truth-table for the miter circuit you have drawn above. Is the miter function satisfiable or unsatisfiable? Give reasons. No marks will be awarded without correct explanation.

iii. Deduce from the above result, whether the ports Z in the two models represent equivalent Boolean function? Give reasons. No marks will be awarded without correct explanation. **[5+3+2 Marks]**

3.

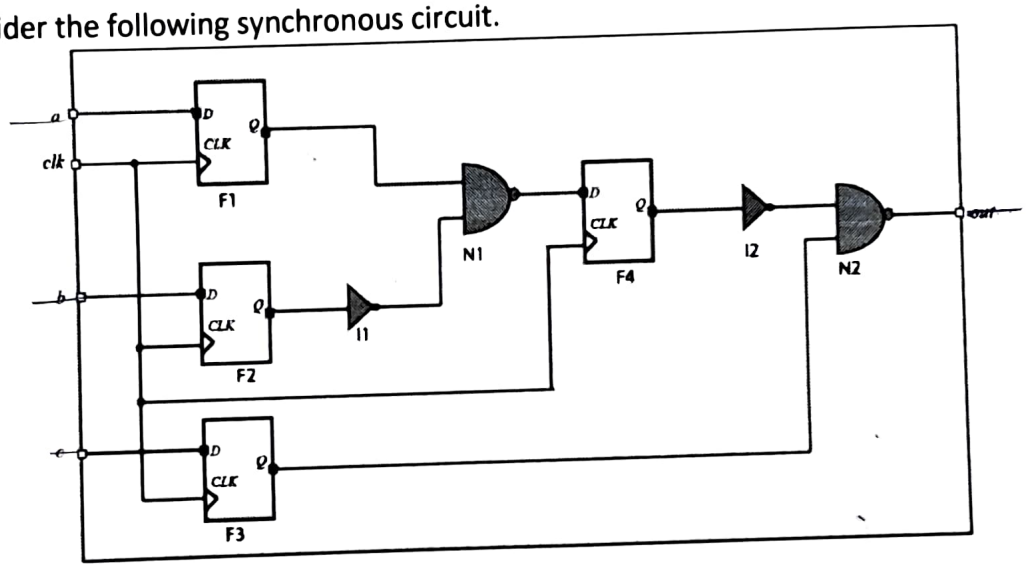
a. A flip-flop named FD has the following attributes: setup time = 30 ps, hold time = 10 ps, and clock to Q delay = 50 ps. An engineer made the following circuit named *MY_FD* by using buffers and the flip-flop *FD*. The delay of the buffers *B1*, *B2*, and *B3* are 10 ps, 50, ps, and 20 ps, respectively.



MY_FD

The engineer proposes to use *MY_FD* as a flip-flop, with *M_D* acting as the D-pin, *M_CP* acting as the clock pin and *M_Q* acting as the Q-pin. Compute the setup time, hold time, and the clock to Q delay of *MY_FD* such that constraints of FD are met. **[2+2+2 Marks]**

b. Consider the following synchronous circuit.



The following attributes are valid for all the flip-flops: setup time=40 ps, hold time=10 ps, and CLK-to-Q delay=50 ps. The delay of each inverter is 100 ps. The delay of each NAND gate is 120ps. Ignore the wire delay.

Assume that we have defined the following constraints in the SDC file (all time units are in picoseconds):

```
create_clock -name CLK -period 800 [get_ports clk]
set_input_delay -clock [get_clocks CLK] 200 [get_ports a]
set_input_delay -clock [get_clocks CLK] 100 [get_ports b]
set_input_delay -clock [get_clocks CLK] 150 [get_ports c]
set_output_delay -clock [get_clocks CLK] 200 [get_ports out]
```

i. What is the **setup slack** at the timing end-point *F1/D*?

ii. What is the **hold slack** at the timing end-point *F1/D*?

iii. What is the **worst slack** for setup at the timing end-point port *out* [Show the computation of all the relevant paths for this port, because each path has separate marks allotted]? **[2.5+2.5+6]**

4.

a. With respect to DFT, answer the following questions:

i. What is a scan chain?

ii. Name the fault model that assumes that a signal is permanently tied to logic 0 or 1.

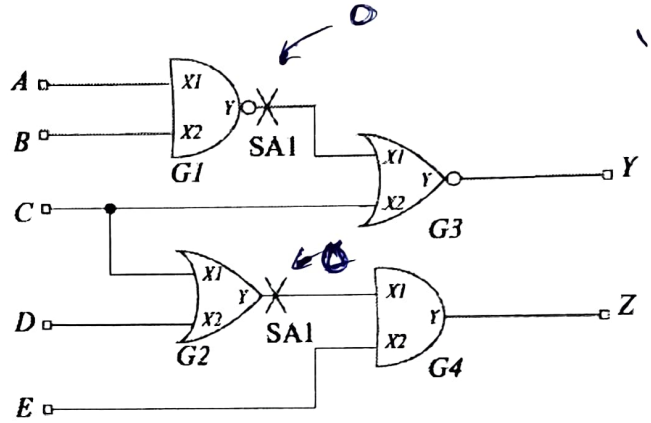
iii. What is the typical circuit that we use for random test vector generation in BIST?

iv. How is combinational ATPG different from sequential ATPG? Which is computationally more difficult problem and why? **[1+0.5+0.5+2=4 Marks]**

b. Consider the circuit shown below.

I. Derive the test pattern for the faults: a) SA1 at G1/Y and b) SA1 at G2/Y.

II. Using the above result compute a single test pattern that can test both the above faults. **[3+3+2=8 Marks]**



c. With respect to IC fabrication, answer the following questions:

i. Explain the problem of channelling encountered during Ion Implantation. How is this problem tackled?

ii. What is dopant activation? Which process is carried out for dopant activation after they are injected?

iii. Why is the barrier layer needed before copper is incorporated into the substrate or wafer?

iv. What is the role of STI in integrated circuit? **[2+1+1+1=5 Marks]**

5.

a. Assume that there are three nets in a design: N1, N2, and N3. The net N1 has 7 pins P1, P2, P3, P4, P5, P6, and P7. The net N2 has 3 pins P8, P9 and P10. The net N3 has 6 pins P11, P12, P13, P14, P15, and P16. A placement engine has identified the following locations of the pins (X and Y coordinates are shown within parentheses):

P1: (0,0)
P2: (10,4)
P3: (2,6)
P4: (4,10)
P5: (5,20)
P6: (7,30)
P7: (18, 35)

P8: (20, 35)
P9: (35, 35)
P10: (70,75)
} N_2

P11: (28, 9)
P12: (64, 6)
P13: (22, 11)
P14: (15, 77)
P15: (12, 9)
P16: (11, 22)
} N_3

Compute the total wirelength of the design, based on the semi-perimeter wirelength estimate (same as the half-perimeter wirelength approximation). Units of length are micron. **[7 Marks]**

b. With respect to power planning, answer the following questions:

i. Name the special circuit element inside a chip through which the chip receives power.

ii. What do we call the metal ring around the core that distributes VDD and VSS around the chip?

iii. What is electromigration? Why are power lines more prone to electromigration than signal lines?

iv. What are decap cells? **[0.5+0.5+2+1=4 Marks]**

c. With respect to clock-tree synthesis, answer the following questions:

i. What is the intentional skew introduced in the clock tree to enhance the maximum operable frequency of a circuit called?

ii. Name the SDC constraint that needs to be applied after clock tree synthesis so that the STA tools can account for real insertion delay in the clock path?

iii. Why does a clock mesh architecture exhibit smaller skews than symmetric tree architecture? **[0.5+0.5+1=2 Marks]**

d. With respect to routing, answer the following questions:

i. Why is crosstalk expected to increase with the increase in the aspect ratio of wires observed at advanced process nodes?

ii. When do we get congestion during routing?

iii. What is a jog in routing?

iv. Why do we add dummy metals over layout after routing?

v. What is parasitic extraction? **[1+1+1+1+1=5 Marks]**