VLSI Design Flow

Solution of Mid Semester Exam (13th March 2022)

Time allowed: 1 hour   *Maximum Marks: 30*

1. Area of wafer = pi*r2=pi*15*15=706.85 cm2

   Area of die = 0.25 cm2

   Number of dies fabricated = 706.85/0.25=2827   1 mark

   (a) Ad=0.25*0.5=0.125

   Yield=(1+0.125/0.5)^(-0.5)*100=89.44%   1 mark

   Number of good dies = 2827*0.8944=2528   1 mark

   Cost per die = $200/2528=7.92 cents   1 mark

   (b) New Ad=0.25*0.1=0.025

   New Yield=(1+0.025/0.5)^(-0.5)*100=97.6%   1 mark

   Number of good dies=2827*0.976=2758   1 mark

   Cost per die =7.24 cents   1 mark

   The yield improves because the defect density decreases and less percentage of dies get impacted by the defect.   1 mark

   (c) Area of die=1 cm^2

   Number of dies fabricated = 706.85/1=706   0.5 mark

   Ad=1*0.1=0.1

   New Yield=(1+0.1/0.5)^(-0.5)*100=91.3%   1 mark

   Number of good dies =706*0.913=644   0.5 mark

   Cost per die=20000/644 cents=31.06 cents   1 mark

   The yield decreases because with the increased die area, the probability of getting a defect on a die increase.   1 mark

2.
   a. create_clock -name VCLK -period 1
      set_input_delay 0.1 -clock [get_clocks VCLK] [get_ports IN]   0.5+0.5 mark

   b. set_case_analysis 0 [get_ports TM]
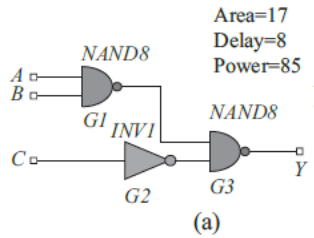
set_case_analysis 1 [get_ports NORMAL]   **0.5+0.5 mark**

c.

set_multicycle_path 8 -setup -from [get_pins FF1/CP] -to [get_pins FF2/CP]   **1 mark for setup**
set_multicycle_path 5 -hold -from [get_pins FF1/CP] -to [get_pins FF2/CP]   **3 marks for hold**
[0 marks if multiplier is wrong in hold]

3.
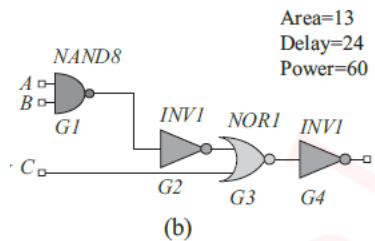
(a)

Area=17
Delay=8   **0.5+0.5+0.5 marks for area, delay power calculations**
Power=85

1.5 marks for circuit mapping

(a)

(b)

Area=13
Delay=24   **0.5+0.5+0.5 marks**
Power=60

1.5 marks

(b)

(c)

Area=8
Delay=32   **0.5+0.5+0.5 marks**
Power=65

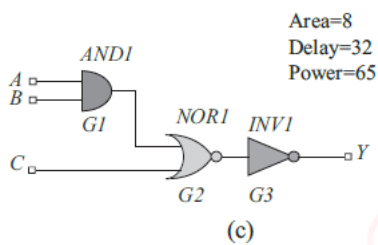**1.5 marks**

(c)

(d) (i) (c) has minimum area
(ii) (a) has minimum delay of worst path   **1+1+1 marks**
(iii) (b) has minimum power