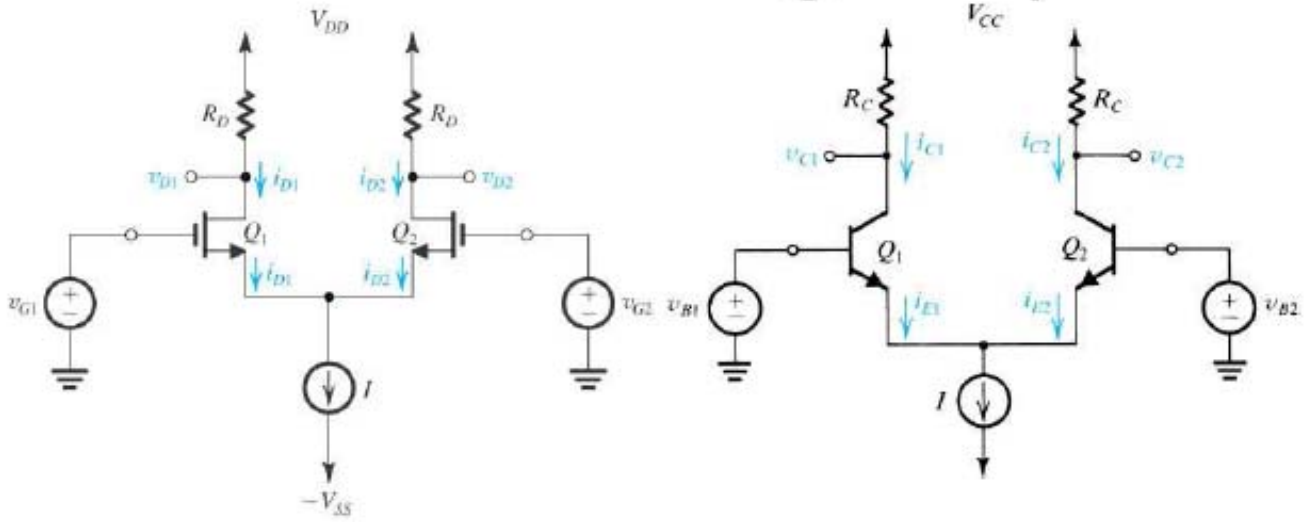
# Differential and Multistage Amplifier

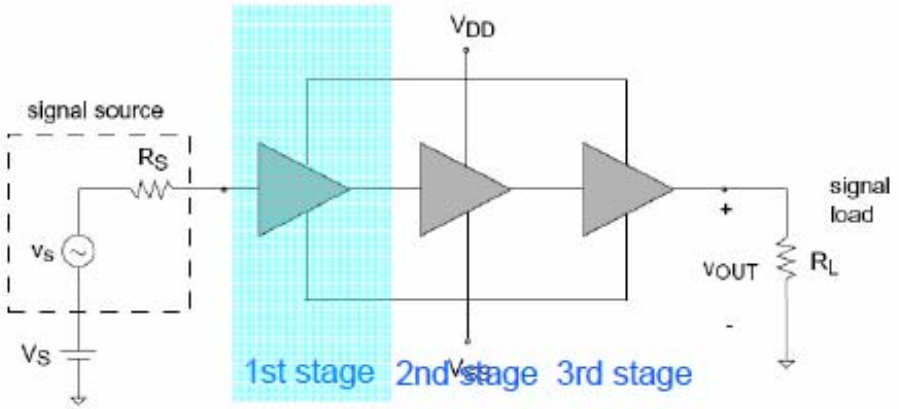
CHAPTER 7

# Differential and Multistage Amplifiers



# Chapter 7 Differential and Multistage Amplifiers

# Introduction to multistage amplifiers




Configuration of multistage voltage op amp

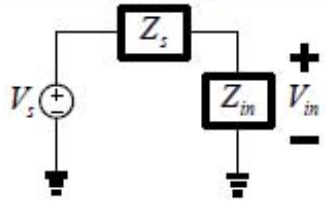
Input (or first) stage

① Provide gain

② Provide a high input resistance to avoid signal loss

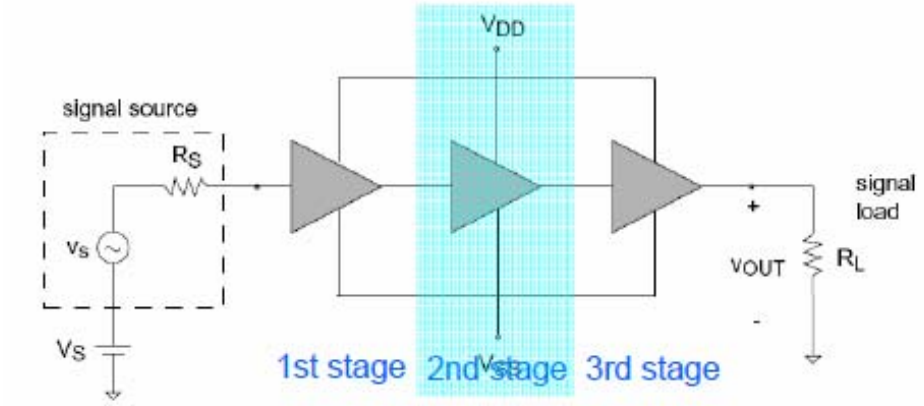
③ Use differential pair to increase CMRR

Infinite input impedance




$$V_{in} = V_s \frac{Z_{in}}{Z_s + Z_{in}} = V_{in} \; (Z_s \ll Z_{in} \rightarrow Z_{in} = \infty)$$

# Introduction to multistage amplifiers



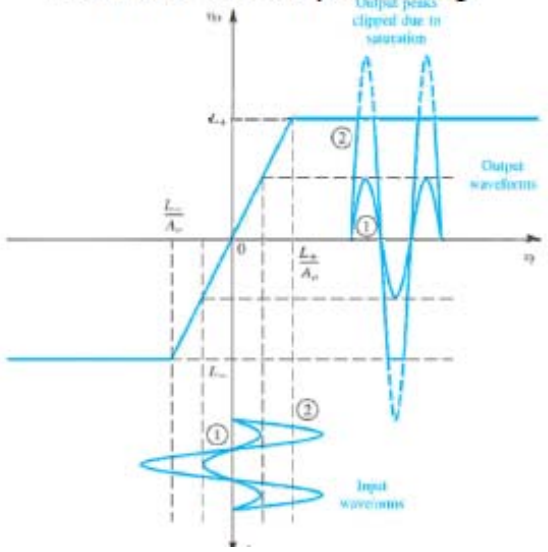

Configuration of multistage voltage op amp

Middle stage

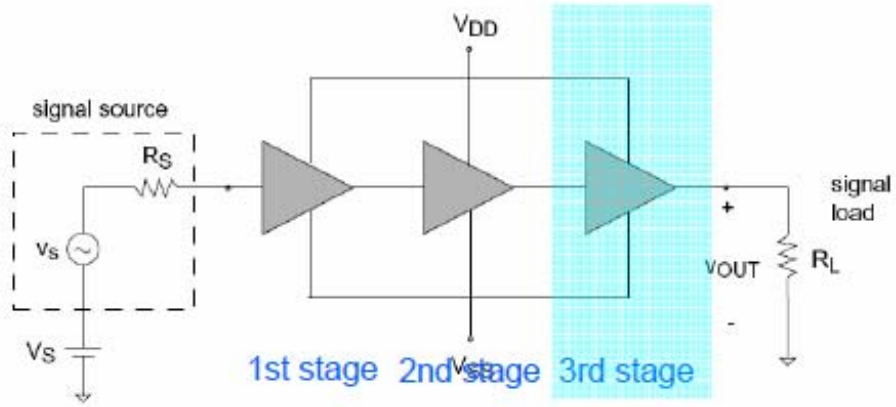
① Provide large gain

② Convert the differential to single signal

③ Shift the dc level of the signal to increase the output swing



# Introduction to multistage amplifiers



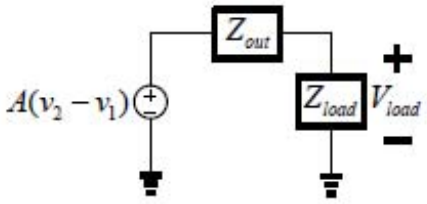

Configuration of multistage voltage op amp

**Output stage**

① Provide low output resistance to avoid gain loss

② Supply the required current to the load

**Zero output impedance**




$$V_{load} = A(v_2 - v_1)\frac{Z_{load}}{Z_{out} + Z_{load}} = A(v_2 - v_1)\ (Z_{out} \ll Z_{load} \rightarrow Z_{out} = 0)$$

# 7.7.1 A Two-Stage CMOS Op Amp

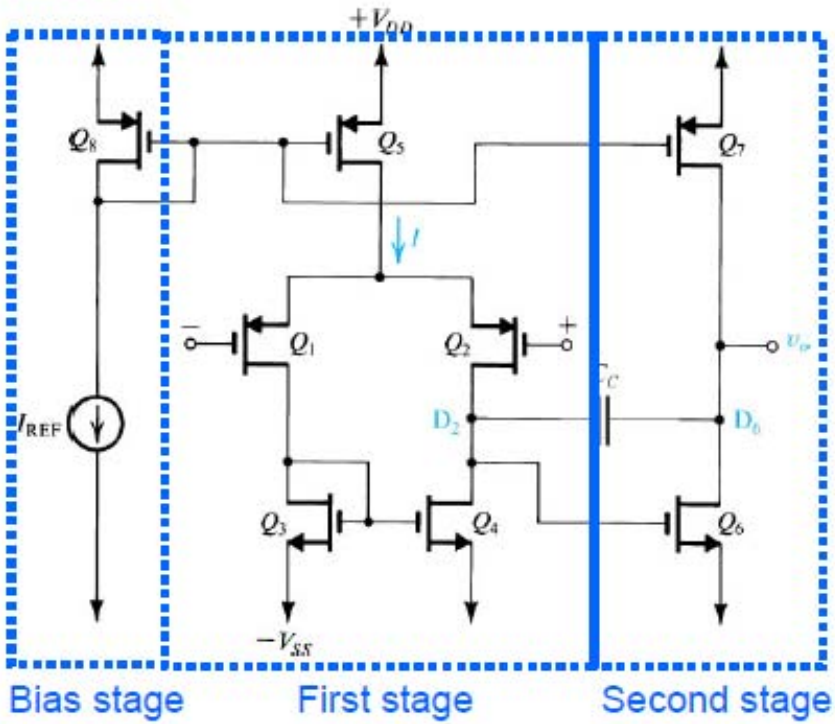



Figure 7.40 Two-stage CMOS op-amp configuration

common source Amp.

Configuration of two stage amplifier

Bias stage

① Reference bias current: $I_{REF}$

② Q8 and Q5: current mirror

First stage

① Q1 and Q2: input differential pair

② Q3 and Q4: active load

Second stage

① Q6: input

② Q7: current source load

③ Cc: frequency compensation capacitor (Ch. 8 & 9)

## 7.7.1 A Two-Stage CMOS Op Amp

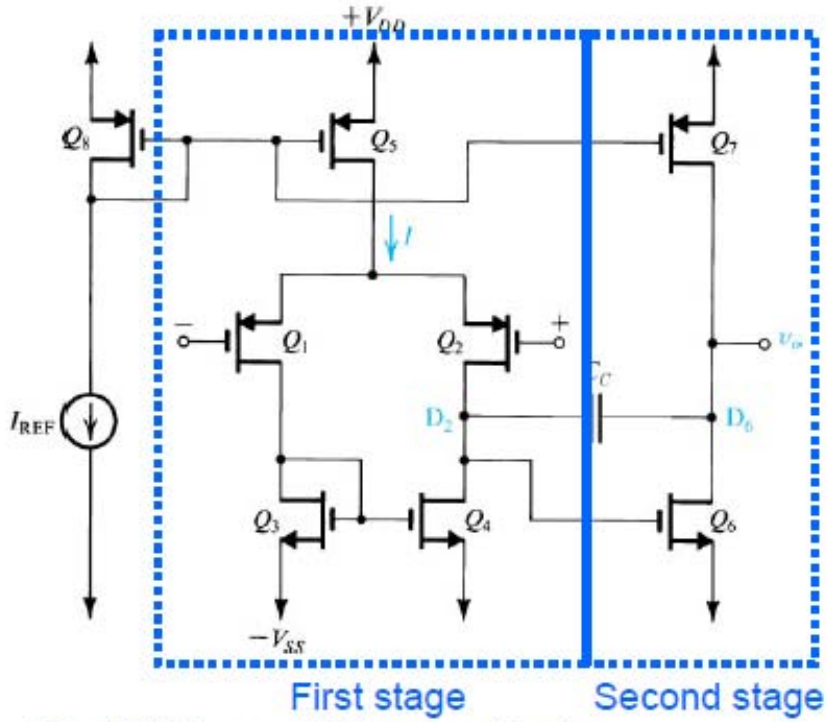



**Figure 7.40** Two-stage CMOS op-amp configuration.

Find the voltage gain of two stage amplifier

The voltage gain of the first stage

① $A_1 = -g_{m1}(r_{o2} \| r_{o4})$ (7.197)

The voltage gain of the second stage

① $A_2 = -g_{m6}(r_{o6} \| r_{o7})$ (7.198)

The voltage gain of two stage amplifier

① $A_{dc} = A_1 A_2 = g_{m1} g_{m6}(r_{o2} \| r_{o4})(r_{o6} \| r_{o7})$ (7.199)

- This circuit does not have a low-output resistance stage ($r_{o6}||r_{o7}$), nevertheless, the circuit is very popular in implementing op-amps in VLSI circuit, where the op-amp needs to drive only a small capacitive load.

# Example 7.3

| | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 |
|---|---|---|---|---|---|---|---|---|
| *W/L* | 20/0.8 | 20/0.8 | 5/0.8 | 5/0.8 | 40/0.8 | 10/0.8 | 40/0.8 | 40/0.8 |

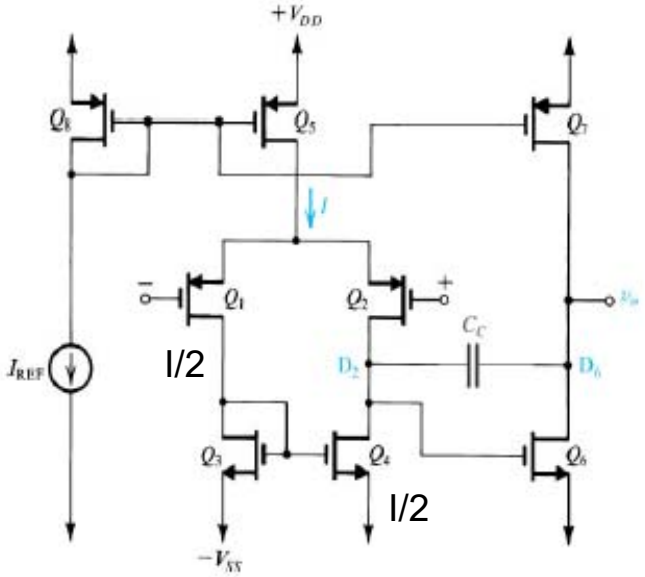



**Figure 7.40** Two-stage CMOS op-amp configuration.

**Conditions**

$I_{REF}=90\mu A$, $V_{tn}=0.7V$, $V_{tp}=-0.8V$, $\mu_n C_{ox}=160\mu A/V$

$\mu_p C_{ox}=40\mu A/V^2$, $|V_A|=10V$, $V_{DD}=V_{SS}=2.5V$

**Solution**

① Since $(W/L)_5=(W/L)_7=(W/L)_8$, $I=I_{REF}$

② Drain current of each device

$$I_D=\frac{1}{2}(\mu C_{ox})(W/L)V_{OV}^{\ 2}$$

③ Thus, the overdrive voltage, the transconductance, and the output resistance of each device

$$V_{ov}=\sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}},\quad |V_{GS}|=|V_t|+|V_{OV}|,\quad g_m=\frac{2I_D}{|V_{OV}|},\quad r_o=|V_A|/I_D$$

## Example 7.3

| Table 7.1 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 |
|---|---|---|---|---|---|---|---|---|
| $I_D$(uA) | 45 | 45 | 45 | 45 | 90 | 90 | 90 | 90 |
| $V_{OV}$(V) | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| $V_{GS}$(V) | 1.1 | 1.1 | 1 | 1 | 1.1 | 1 | 1.1 | 1.1 |
| $g_m$ | 0.3 | 0.3 | 0.3 | 0.3 | 0.6 | 0.6 | 0.6 | 0.6 |
| $r_o$ | 222 | 222 | 222 | 222 | 111 | 111 | 111 | 111 |

① Voltage gain of 1st stage & 2nd stage

$$A_1 = -g_{m1}(r_{o2} \| r_{o4}) = -33.3\text{V/V}$$

$$A_2 = -g_{m6}(r_{o6} \| r_{o7}) = -33.3\text{V/V}$$

② Overall open-loop dc gain

$$A_0 = A_1 A_2 = (\text{-}33.3) \times (\text{-}33.3) = 1109\text{V/V}$$

$$A_0(\text{dB}) = 20\log 1109 = 61\text{dB}$$

## Example 7.3

③ Lower limit of the input common-mode range;

$$V_{ICM,\min} = -V_{SS} + V_{GS3} - \left|V_{tp}\right| = -2.5 + 1 - 0.8 = -2.3\text{V}$$

④ Upper limit of the input common-mode range;

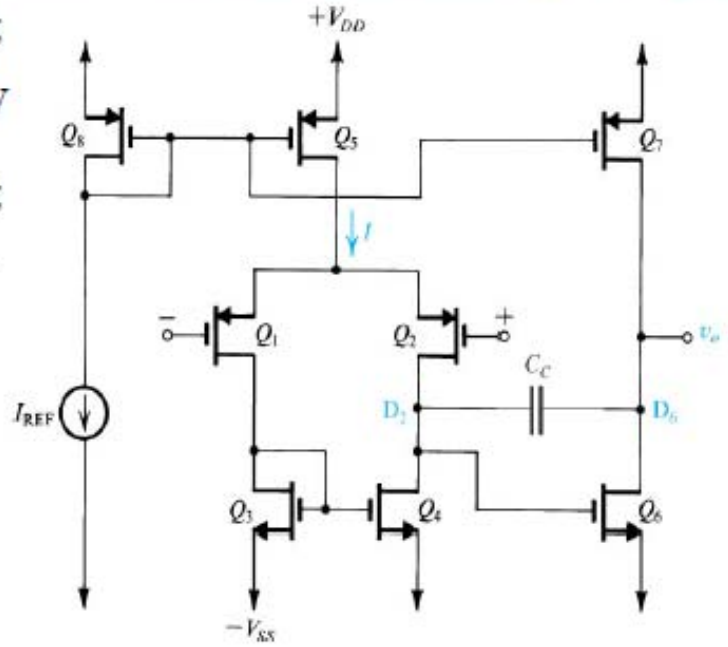
$$V_{ICM,\max} = V_{DD} - V_{OV5} - V_{SG1} = 2.5 - 0.3 - 1.1 = 1.1\text{V}$$

⑤ Highest allowable output voltage;

$$V_{O,\max} = V_{DD} - \left|V_{OV7}\right| = 2.5 - 0.3 = 2.2\text{V}$$

⑥ Lowest allowable output voltage;

$$V_{O,\min} = -V_{SS} + V_{OV6} = -2.5 + 0.3 = -2.2\text{V}$$



# 7.7.1 A Two-Stage CMOS Op Amp

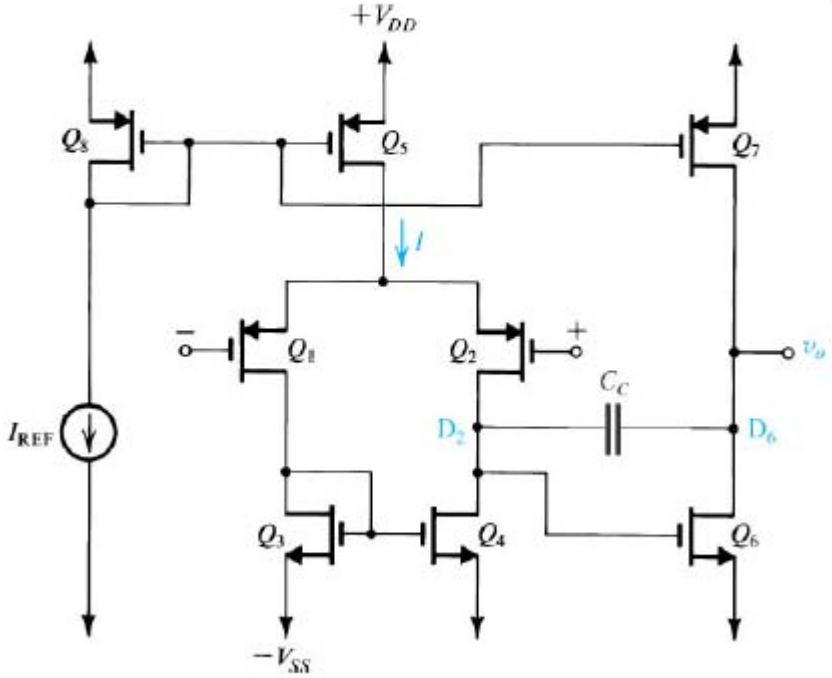



**Figure 7.40** Two-stage CMOS op-amp configuration.

Systematic offset (not random offset)

① Two input terminals: grounded

② If the input stage is perfectly matched

$$V_{D3} = V_{D4} = -V_{SS} + V_{GS4}$$

$$V_{GS4} = V_{GS6}$$

③ Thus, drain current through Q6

$$I_6 = \frac{(W/L)_6}{(W/L)_4}(I/2)$$

④ And drain current through Q7

$$I_7 = \frac{(W/L)_7}{(W/L)_5} I$$

⑤ For no offset, $I_6 = I_7$

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

$(W/L)_4 = 5/0.8, (W/L)_6 = 10/0.8$

$(W/L)_5 = 40/0.8, (W/L)_7 = 40/0.8$

## 7.7.1 A Two-Stage CMOS Op Amp

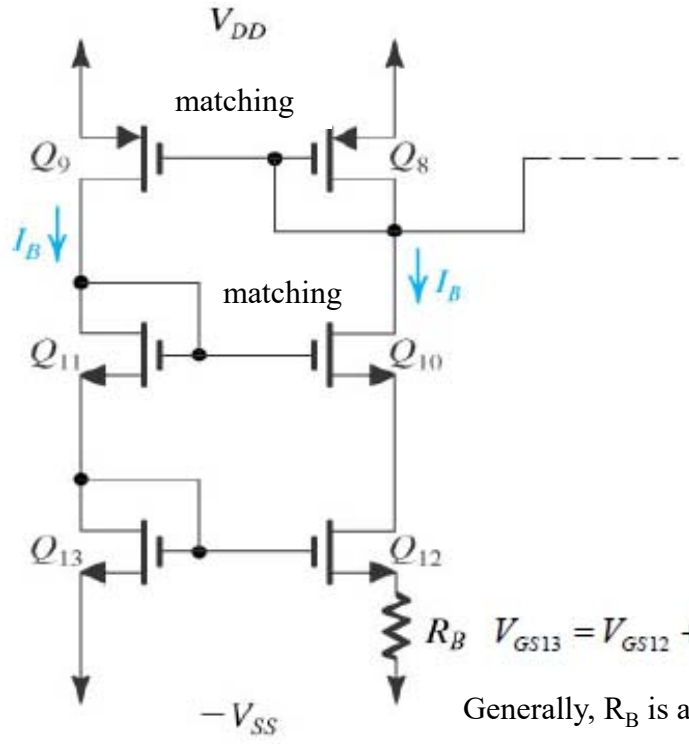



**Figure 7.42** Bias circuit for the CMOS op amp.

A bias circuit that stabilizes $g_m$

① Independent of supply voltage
② Independent of MOSFET threshold voltage
③ Determined only by a single resistor and the device dimensions

Generally, $R_B$ is an off-chip resistor.

## 7.7.1 A Two-Stage CMOS Op Amp

How to remain constant $g_m$

Currents through Q12 & Q13 due to current mirror

$$I_B = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{12}(V_{GS12} - V_t)^2 \qquad (7.212)$$

$$I_B = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{13}(V_{GS13} - V_t)^2 \qquad (7.213)$$

Gate-source voltages at Q12 & Q13

$$V_{GS13} = V_{GS12} + I_B R_B$$

$$V_{GS13} - V_t = V_{GS12} - V_t + I_B R_B$$

$$\sqrt{\frac{2I_B}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_B}{\mu_n C_{ox}(W/L)_{12}}} + I_B R_B \qquad (7.214)$$

$$I_B = \frac{2}{\mu_n C_{ox}(W/L)_{12} R_B^{\,2}}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)^2 \qquad (7.215)$$

$$I_B \propto \frac{1}{(W/L)_{12} R_B^{\,2}}$$

$$R_B = \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{12} I_B}}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)$$

$$g_{m12} = \sqrt{2\mu_n C_{ox}(W/L)_{12} I_B}$$

$$g_{m12} = \frac{2}{R_B}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right) \qquad (7.216)$$

$g_{m12}$ can be constant.
(determined only by $R_B$, ration of $(W/L)_{12}$ and $(W/L)_{13}$)

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \qquad g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$