

VLSI Design Flow

Mid Semester Exam (27th February 2023)

Time allowed: 1 hour

Maximum Marks: 30

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Cheating or use of unfair means will be dealt with as per institute policy.

1.
 - a. Briefly explain Optical Proximity Correction (OPC). **[2 Marks]**
 - b. Explain why does a designer (or verification engineer) needs to make more effort in determining the functional coverage than determining the code coverage for an RTL design written in Verilog? **[2 Marks]**
 - c. Explain how does SoC design methodology help in reducing design effort. **[2 Marks]**
 - d. A designer wants to capture within-cycle glitches for combinational circuit elements/logic in RTL simulation. Which type of simulator can be used for this purpose: event-based or cycle-based. Give reason in support of your answer. **[0.5+1.5 Marks]**
 - e. What is the effect of uniquification in RTL synthesis? When do we want to perform uniquification? **[1+1 Marks]**
 - f. When can you get a warning of a module being treated as black-box during elaboration? How can the problem be solved? **[1+1 Marks]**
2. Draw the schematic of the circuit that will be generated by the synthesis of the following Verilog codes (No need of any explanation). Label all the design entities (including pins and ports) appropriately (marks will be deducted for wrong/missing labeling).

a.

```
module top(a, b, s, out1);
    input a, b, s;
    output out1;
    reg out1;
    always @(*) begin
        if (s==1'b1)
            out1 = a;
        else
            out1 = b;
    end
endmodule
```

b.

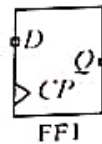
```

module top(c, en, out2);
    input c, en;
    output out2;
    reg out2;
    always @(*) begin
        if (en==1'b0)
            out2 = c;
    end
endmodule

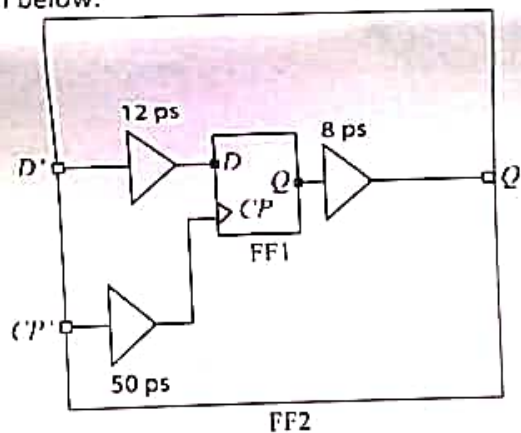
```

[2+2 Marks]

3. A library contains a flip-flop named FF1 (shown below) with a setup time of 20 ps, hold time of 10 ps, clock-to-Q delay of 10 ps.

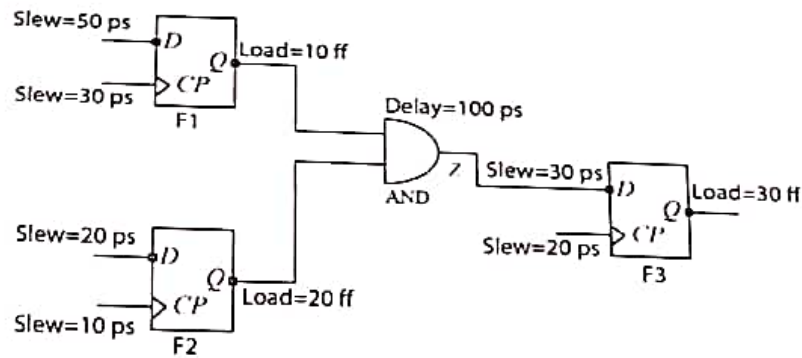


A designer made another flip-flop FF2 by reusing FF1 and adding three buffers having delays 12 ps, 8 ps, and 50 ps, as shown below.



Compute the setup time, hold time and clock-to-Q delay of FF2 (the data, clock, and Q pins of FF2 are D', CP', and Q', respectively). [2+2+2 Marks]

4. Consider the portion of a synchronous circuit shown below.



Assume that the clock period is 1000 ps. Assume that the arrival time of the clock signal at the clock pin of all the flip-flops is 0 ps. The signals arriving at the input of the flip-flops have slews as shown in the figure. Also, the loads at the output of the flip-flops are shown in the figure. The delay of the AND gate is 100 ps.

The NLDM table for the clock-to-Q delay (in ps) are shown below [valid for all flip-flops].

	Load=10 ff	Load=20 ff	Load=30 ff	Load=40 ff
Clk Slew=10ps	10	20	30	40
Clk Slew=20ps	20	30	40	50
Clk Slew=30ps	25	35	45	55
Clk Slew=40ps	28	38	48	58

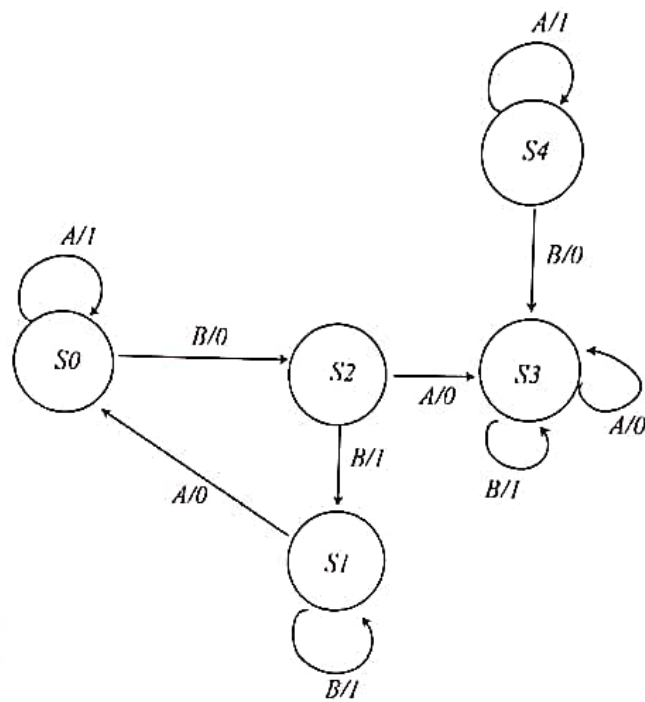
The NLDM table for the setup time (in ps) are shown below [valid for all flip-flops].

	Clk Slew=10ps	Clk Slew=20ps	Clk Slew=30ps	Clk Slew=40ps
Data Slew=20ps	10	12	14	16
Data Slew=30ps	12	16	18	20
Data Slew=40ps	14	18	22	26
Data Slew=50ps	18	25	30	40

For data not given for the problem (such as wire delay), assume that ideal conditions exist. The setup slack is defined as the difference between the required time and the arrival time.

- Compute the setup slack for the path between F1 and F3.
- Compute the setup slack for the path between F2 and F3. [2+2 Marks]

5. The state diagram for an FSM with five states S_0 , S_1 , S_2 , S_3 , and S_4 is shown below:



The state bits are a, b, c . The input set is $\{A, B\}$ and the output set is $\{0, 1\}$.

The state encoding is as shown in the following table.

	a	b	c
$S0$	0	0	0
$S1$	0	0	1
$S2$	0	1	0
$S3$	0	1	1
$S4$	1	0	0

- Write the characteristics function of the set of reachable states when the starting state is $S1$.
- Write the characteristics function of the set of reachable states when the starting state is $S4$.

[2+2 Marks]