VLSI Design Flow

Mid Semester Exam (2nd March 2024)

Time allowed: 1 hour *Maximum Marks: 30*

1.

a. Inputs:

i. Algorithm or Design in C/C++/SystemC/MATLAB, High-level Programming Language

ii. Constraints (Frequency, Latency, Area, Power etc.) and list of resources that can be used

Output: RTL in Verilog or VHDL **[0.5+0.5+1 Marks]**

b. ECO involves making small final fixes/changes in the design at the last stages of a design flow. **[2 Marks]**

c. Increasing the area of a die reduces the yield of manufacturing that die. With increased area the probability of introducing at least one fatal random defect on the given die increases, which will reduce the yield. **[0.5+1.5 Marks]**

d. Event-based simulator should be used. An event-based simulator can capture events or changes in the signal within a clock cycle for combinational circuit elements. Hence, it can capture within-cycle glitches. A cycle-based simulator only computes values at clock edges. Hence, it will miss within-cycle glitches. **[0.5+1.5 Marks]**

e.

A) Setup-time of the flip-flop will decrease

B) Clock-to-Q delay of the flop-flip is not impacted by the slew at the D-pin **[1+1 Marks]**

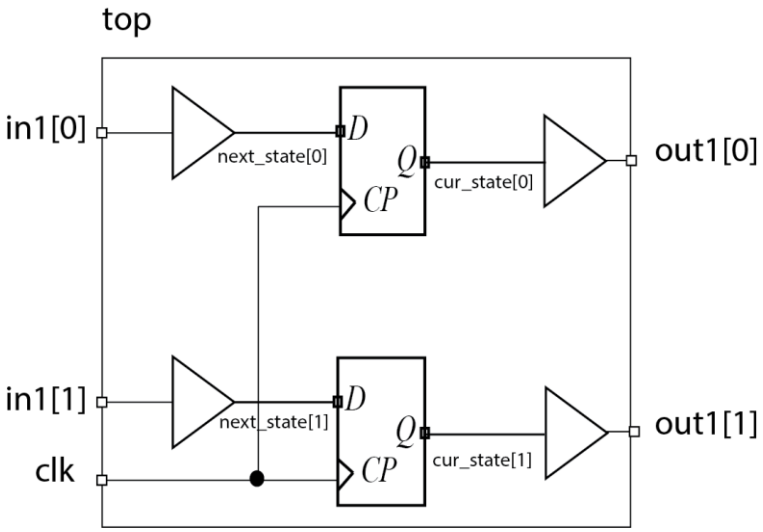
2. Output will be:

Display a=1 b=1
Monitor a=0 b=1

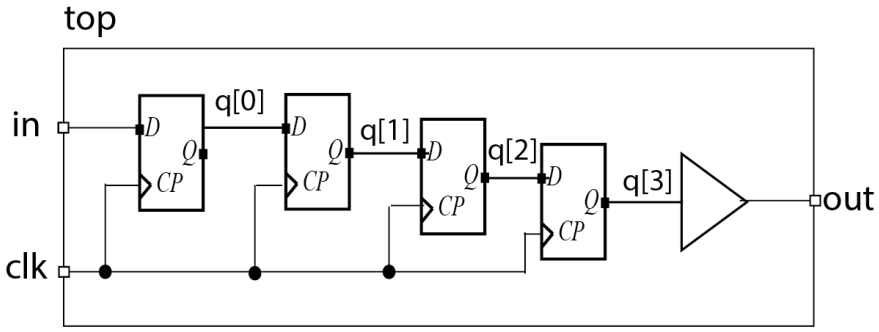
The two blocking assignments will be executed before the display statement.
The LHS of non-blocking assignment will be executed before the monitor statement. The values that are assigned by NBA was pre-determined while executing the RHS of NBA. Hence b gets the old value of a. **[1.5+0.5+1.5+0.5 Marks]**

3.

a.



b.



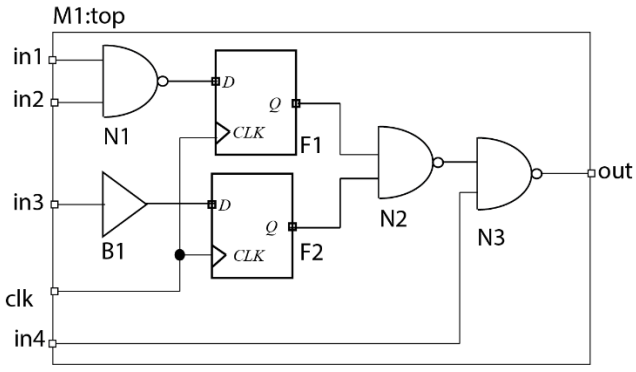
4.

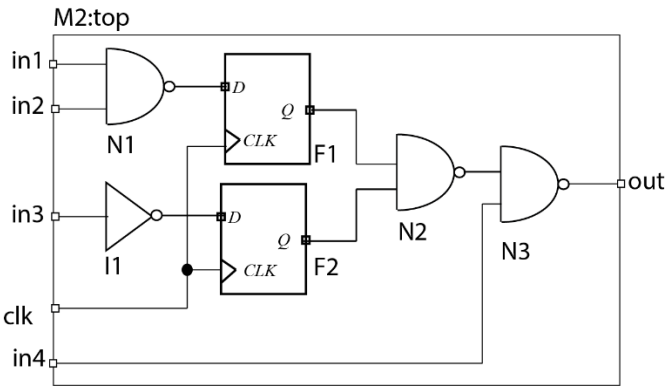
a) Taking maximum arrival time = 17 + 14 + 44 + 23 ps = 98 ps
Required Time = 1000 – 37 ps = 963 ps
Slack = RT-AT=963-98=865 ps

b) Taking minimum arrival time = 17 + 23 ps = 40 ps
Required Time = 15 ps
Slack = AT-RT=40-15=25 ps [**2+2 Marks]**

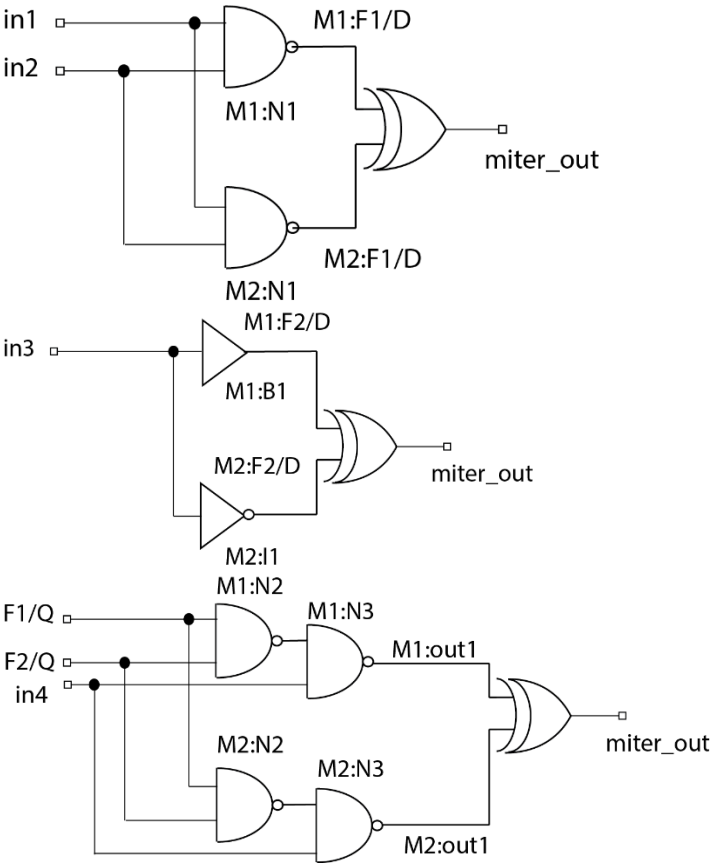
5.

a)





b)



c) Second miter will fail. The input pattern is in1=X, in2=X, in3=0, in4=X or in1=X, in2=X, in3=1, in4=X