VLSI Design Flow

End Semester Exam (6th May 2024)

Time allowed: 2 hours *Maximum Marks: 80*

Note:

*I. **Marks are indicated in bold at the end of each question.***
*II. **There are 5 questions of 15, 15, 10, 20 and 20 marks. All questions are compulsory.***
*III. **Be crisp and precise in your answer so that you can complete the answers in 2 hours.***
*IV. **Cheating or using unfair means will be dealt with as per institute policy.***

1.

a. Regarding the semiconductor business ecosystem, answer the following questions:
   i. What are fabless design companies?
   ii. How can merchant foundries, such as TSMC, become profitable despite having a huge capital cost?
   iii. What is the role of PDKs in ensuring that the layout produced (designed) by a fabless design company is profitably manufactured by a given merchant foundry? **[2+2+2 Marks]**

b. Regarding photolithography, answer the following questions:
   i. What is the role of mask in photolithography?
   ii. How does OPC help in improving the resolution of photolithography? **[2+2 Marks]**

c. How does SoC-based design methodology improve a designer's productivity? **[2 Marks]**

d. What is the package's role in managing a chip's thermal profile? **[2 Marks]**

e. What information does a GDS file contain? **[1 Mark]**

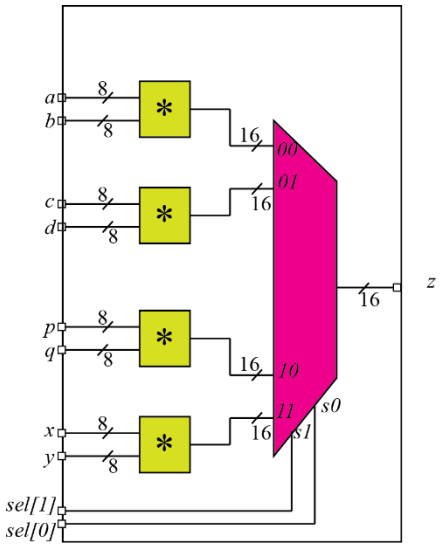
2.

a. Consider the following Verilog module.

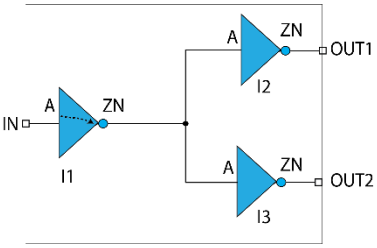
```
module top(in1, in2, clk, out);

        input in1, in2, clk; output out;
        reg q1, q2;

        always @ (posedge clk) q1 <= !(in1 & in2);
        always @ (posedge clk) q2 <= (in1 & in2);
        always @* out = !(q1 & q2);
endmodule
```

Draw the schematic of the synthesized netlist and mark the circuit elements. Assume that the library used in synthesis contains only the following circuit elements: inverter, two-input NAND gate, and D flip-flop. [**4 Marks]**

b. Consider the unoptimized netlist (circuit) generated by an RTL synthesis tool shown alongside. The numbers on the nets indicate the number of lines in a bus. The multiplexer selects one of the four buses based on the select lines $s0$ and $s1$. The elements marked * are multipliers.
Redraw the circuit with resource sharing that minimizes the circuit area (**mark the number of lines in each bus).** Assume that the area of a multiplier is significantly higher than the multiplexers. Hence, the number of multipliers needs to be minimized. Increasing the number of multiplexers is permitted. Further, assume that the timing constraints are relaxed. **[4 Marks]**



c. Consider the circuit shown alongside. It consists of instances of three **identical** inverters. The input capacitance of the pin A for each inverter is 10 ff. The NLDM table for the timing arc $A \rightarrow ZN$ for the inverter is also shown below the circuit.



The minimum and maximum transition time at the input port IN are 10 ps and 20 ps, respectively. Ignore net capacitances. Compute

i. Delay of the arc $A \rightarrow ZN$ for the instance $I1$ for the setup analysis
ii. Delay of the arc $A \rightarrow ZN$ for the instance $I1$ for the hold analysis

	$C=10ff$	$C=20ff$	$C=50ff$
$10\ ps$	20	30	60
$20\ ps$	30	45	75
$100\ ps$	60	75	90

[2+2 = 4 Marks]

d. The ROBDD for a Boolean function of 7 variables is a leaf vertex labeled 1. Is this function satisfiable? Explain your answer. **[0.5+0.5=1 Mark]**

e. Consider combinational equivalence checking (CEC) of two purely combinational circuit (i.e. a circuit that does not contain any flip-flops or latches).

i. Which types of design entities are treated as **matching points** for these circuits (i.e., the design entities whose matching will be done by the CEC tool)?
ii. Which types of design entities are treated as **compare points** for these circuits (i.e., design entities where equivalence will be established by the CEC tool by creating miters)? **[2 Marks]**

3.

a. Name the type of unate-ness for the following logic gates: i) NAND ii) NOT **[0.5+0.5=1 Mark]**

b. Name any one tool (can be open-source or commercial) that is used for i) combinational equivalence checking ii) automatic test pattern generation iii) clock tree synthesis iv) RTL simulation **[0.5+0.5+0.5+0.5=2 Marks]**

c. Why do we typically not focus on hold violation during logic synthesis? **[2 Marks]**

d. Write a UNIX command for doing the following i) going to a parent directory from any given directory ii) searching all the occurrences of the word "port" in a Verilog file "test.v" **[1+1=2 Marks]**

e. Write an SDC command to create a clock named "CLOCK" on a pin named "Gen/Clk" with a period of 1000 ps and 50% duty cycle. Assume that the unit for time in the SDC file is ps. **[1 Mark]**

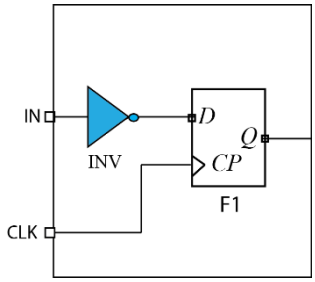
f. Answer the following questions based on the report shown alongside. It was generated by an open-source STA tool:

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max
```

(i) Name of the capture flip-flop (ii) Whether the timing analysis is for the setup constraint or the hold constraint? **[1+1=2 Marks]**

4.

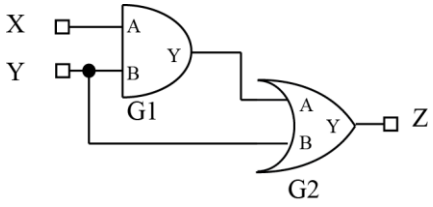
a. Consider the following portion of a circuit shown alongside. The delay of the inverter is 100 ps. The setup and hold time of the flip-flop F1 is 50 ps and 20 ps, respectively. The following constraints are given in the SDC file.




```
create_clock -name CLK -period 1000 [get_ports CLK]
set_input_delay 100 -min -clock [get_clocks CLK] [get_ports IN]
set_input_delay 500 -max -clock [get_clocks CLK] [get_ports IN]
```

Compute the setup and hold slack at the flip-flop F1. Ignore wire delays. **[2+2 Marks]**

b. Consider the circuit shown alongside.



- **i.** How many fault sites are there in the circuit for single stuck-at faults? (Just give the number)
- **ii.** Determine the test pattern for SA0 at G2/A.
- **iii.** Using the results of the above question, transform the given circuit to reduce area and draw its schematic representation.
- **iv.** Consider CEC for the given circuit and the circuit you have drawn in the above question. Draw the miter circuit employed for carrying out CEC.
- **v.** What is the output of the above miter circuit for various input values? Using this observation, comment on the functional equivalence of the given and the transformed circuits. **[1+2+2+2+1 Marks]**

c. What do you understand by the recovery time constraints for a flip-flop having an asynchronous reset pin? **[2 Marks]**

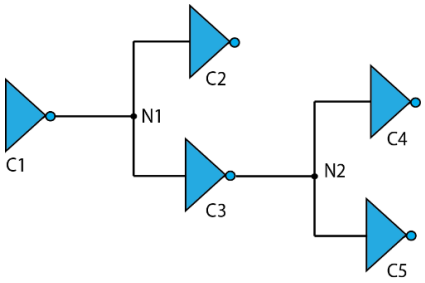
d. What is aliasing in signature analysis for a BIST? **[2 Marks]**

e. Why do we typically route power lines on the higher layer of the interconnect stack? **[2 Marks]**

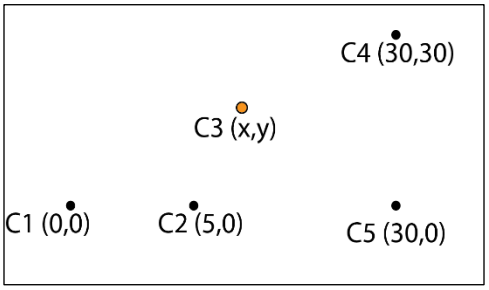
f. What is the motivation for adding spare cells in a design? **[2 Marks]**

5.

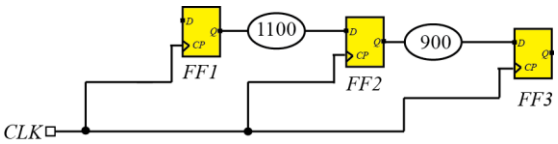
a. Consider the portion of a netlist shown alongside. The five cells $C1$, $C2$, $C3$, $C4$, and $C5$ are connected using two nets $N1$ and $N2$.



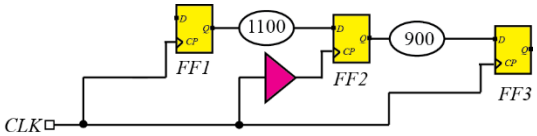
Each cell is treated as a point object during placement. The location of the cells on the layout (X and Y coordinates) is also shown alongside. The location of $C3$ is unknown and marked as (x,y). The half perimeter wirelength estimate of the net $N1$ is 20 units and of the net $N2$ is 45 units. Given that: $5 \leq x \leq 30$ and $0 \leq y \leq 30$, determine x and y. {**Hint:** For a net with multiple pins at (x_i, y_i), HPWL estimate is $[MAX(x_i) - MIN(x_i)] + [MAX(y_i) - MIN(y_i)]\}$ **[3+3 Marks]**



b. Consider the most critical portion of a synchronous sequential circuit shown alongside. The combinational circuit elements shown in the figure have a delay of 1100ps and 900ps. Assume that the setup time and clock-to-Q delay of all the flip-flops are zero. Ignore wire delays. What is the minimum clock period at which the circuit can operate? **[2 Marks]**



c. This is a continuation of the above question. A designer wishes to increase the maximum operable frequency of the circuit by adding a single buffer, as shown in the figure alongside. There are three buffers in the library of delay: 50 ps, 100 ps, and 150 ps. The designer tries these buffers one by one. Evaluate separately the minimum clock period the circuit can operate for each buffer. **[2+2+2 Marks]**



Using the above evaluations, determine which buffer should be inserted to obtain the maximum operable frequency and also compute the maximum operable frequency of the circuit? **[1+1=2 Marks]**

d. Explain how self-healing of the electromigration effect can occur in the clock lines or nets. **[2 Marks]**

e. Why do we insert redundant vias in a design? **[2 Marks]**