VLSI Design Flow

Mid Semester Exam (15th February 2020)

Time allowed: 1 hour *Maximum Marks: 40*

Note:

I. *All questions are compulsory.*
II. *Marks are indicated in bold at the end of each question.*
III. *Be crisp and precise in your answer so that you can complete the answers in 1 hour.*
IV. *Use the marks allotted to each question as an indicator of how elaborate you need to answer.*
V. *Use of any communication device is prohibited during examination.*
VI. *Cheating or use of unfair means will be dealt with as per institute policy.*

1. As per Verilog IEEE Std 1364-2001 (from Verilog LRM), the definitions of binary AND (&) and OR (|) operators are as follows.

Table 19—Bit-wise binary and operator

&	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

Table 20—Bit-wise binary or operator

|	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

A Verilog design is as follows:

```
module top(A, clk, R1, R2, W, Y, Z);
        input A, clk;
        output R1, R2, W, Y, Z;
        reg R1, R2;

        assign Y = ~A|A;
        assign Z = ~A&A;
        assign W = 1'bx;
        always @(clk or A)
                if (clk)
                        R1 <= A;
        always @(clk)
                if (clk)
                        R2 <= A;
endmodule
```

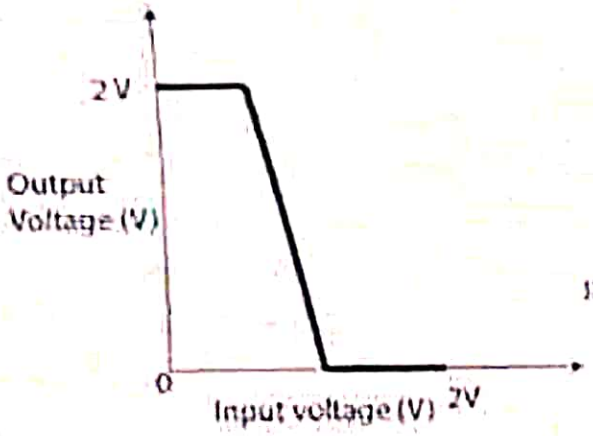
i) Assume that the value of A is 1'bx. What will be the value of Y, Z and W if the above code is simulated using four-valued logic?

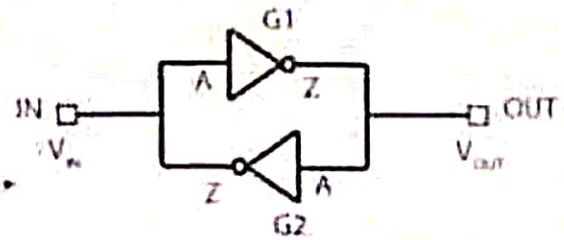
ii) Draw the schematic of the expected netlist for the above Verilog code when synthesized.

iii) Assume that the value of A is 1'bx. What will be the value of Y, Z and W if the above expected netlist is simulated using four-valued logic?

iv) If the underlined block of code is synthesized as a latch, then there can be a synthesis-simulation mismatch. Explain why. **(1.5+5+1.5+2 Marks)**

2.





a. An approximate transfer characteristic of a CMOS inverter is shown above. Assume that the supply voltage is 2V. Assume that in the transition region the output voltage (Y) is

$Y = 12 - 20X$, where X is the input voltage in volts. In other regions, the inverter characteristics are ideal.

Using the above inverter, a primitive memory element is built by cross-coupling as shown on the previous page.

i) Find the metastable voltage (V_{MS}) for the cross-coupled inverter.

ii) Assume that the cross-coupled inverter was initially in the metastable state. If due to thermal noise, V_{IN} decreases by 1 mV, then what will be the stable voltage V_{OUT}?

iii) Assume that the cross-coupled inverter was initially in the metastable state. If due to thermal noise, V_{IN} increases by 1 mV, then what will be the stable voltage V_{OUT}?

(3+1+1 Marks)

b. Assume that for the library cells INV1X, INV4X and FF1X, the NLDM tables specified in a technology library is as follows:

Output transition in ps for INV2X:

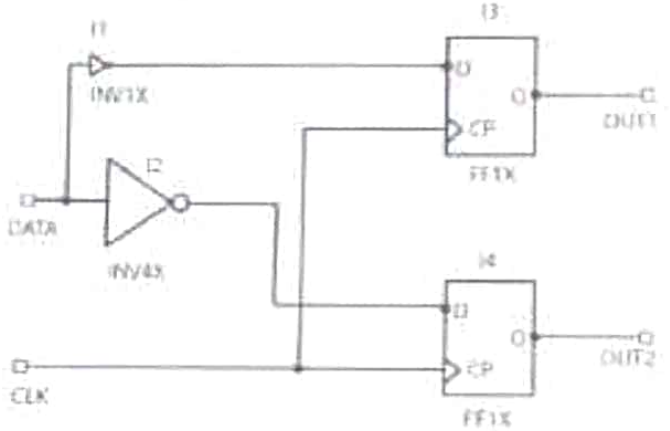
Load -> Input Transition V	2 pF	4 pF	8 pF	16 pF
10 ps	10	20	30	40
20 ps	20	30	40	50
40 ps	30	40	50	60
80 ps	40	50	60	70

Output transition in ps for INV4X:

Load -> Input Transition V	2 pF	4 pF	8 pF	16 pF
10 ps	5	7.5	8	10
20 ps	10	20	30	40
40 ps	20	30	40	50
80 ps	30	40	50	60

Hold Time in ps for FF1X:

Clock Pin Transition -> Data Pin Transition V	5 ps	10 ps	12 ps	15 ps
5 ps	5	6	7	8
10 ps	9	10	11	12
20 ps	13	14	15	16
40 ps	17	18	19	20



Consider the design as shown above. The instances I1, I2, I3 and I4 are of library cells INV1X, INV4X, FF1X and FFF1X, respectively.

Assume that all the wires are ideal (with negligible resistance and capacitance). The load capacitance of D pin is 4 pF. The input transition at the port DATA is 10 ps and the port CLK is 12 ps.

Find the hold time of flip-flops I3 and I4. Show all the steps. Just writing answer will not fetch any marks.

(2+3 Marks)

3.

a. The yield is given by the following equation.

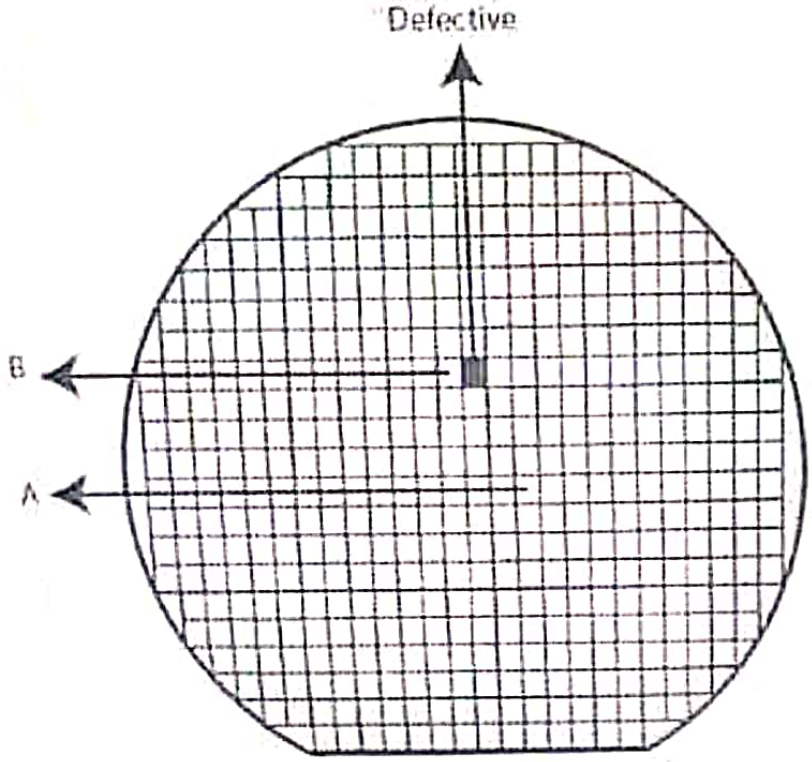
$$Yield = (1 + Ad/\alpha)^{-\alpha} \times 100\%$$

where A is the area of the die, d is the defect density and α is the clustering parameter. The diameter of the wafer is 300 mm and the die size is 25 mm^2. Assume that the cost of fabricating a wafer is $100 and there is no wastage of material in creating dies out of wafer. Assume defect density is 0.5 $defect/cm^2$ and clustering parameter is 0.5. Estimate the yield and the cost per die. **(3+3 Marks)**

b. What is the purpose of a pellicle on a mask? **(1 Mark)**

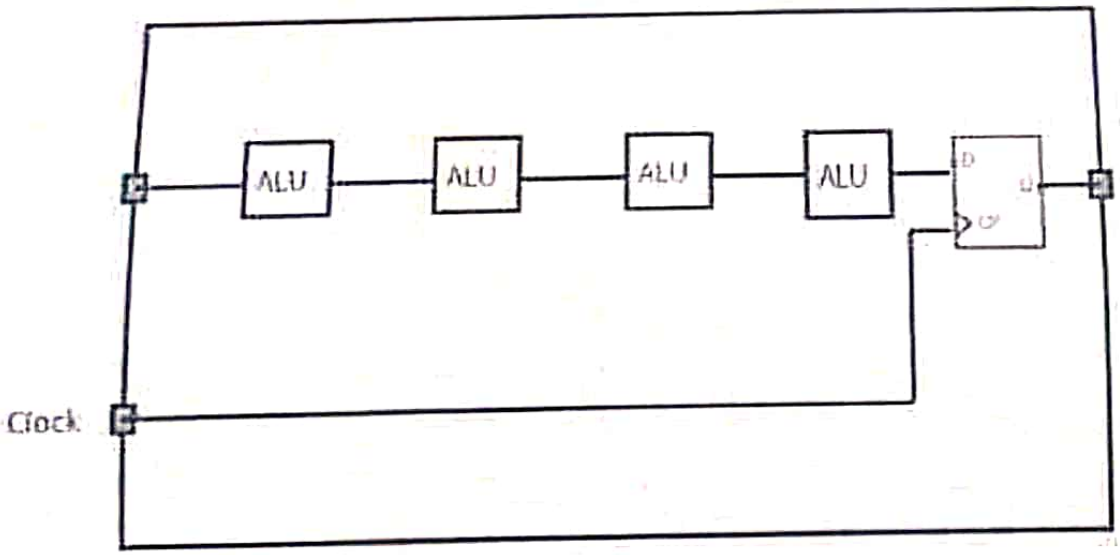
c. If the area of a die increases then how is the yield expected to change (i.e. yield will increase or decrease)? Give reason for your answer. **(2 Marks)**

d. Name any two resolution enhancement techniques. **(1 Mark)**



c. A defect is found on a die on a wafer, as shown above. Consider two dies A and B, as shown above. Which of the two dies is more likely to be defective. Give reasons for your answer. **(2 Marks)**

4. Consider the following synchronous circuit. It receives data from another circuit that uses the same clock.



a. Estimate the maximum operable frequency of the circuit. Make the following assumptions:

i. All ALUs have delay of 2 ns
ii. All nets are ideal and have delays of 0 ns
iii. All flip-flops are ideal, Setup Time of flip-flop is 0 ps
iv. All clocks are ideal

v. Input Delay of Data Path is 0 ns **(2 Marks)**

b. A designer decided to improve the maximum operable frequency of the circuit by introducing some flip-flops (as many as required) in the data-path of the circuit. Modify and redraw the circuit shown on the previous page such that the maximum operable frequency is two times that computed in (a).

Modify and redraw the circuit shown on the previous page such that the maximum operable frequency is four times that computed in (a). **(2+2 Marks)**

c. Name two disadvantages of modified circuits with respect to the original circuit shown on the previous page. **(2 Marks)**