TWO STAGE OTA DESIGN

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AIM :

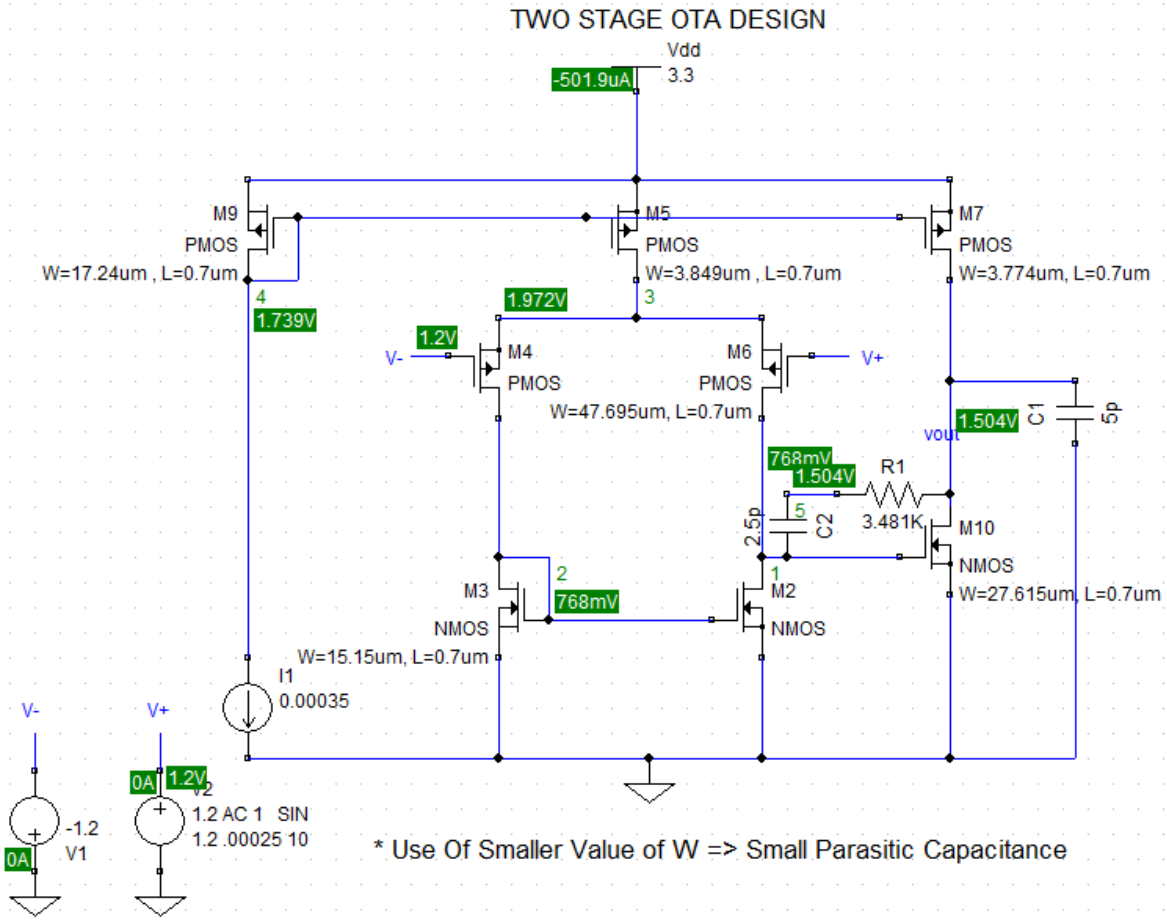
To design a 2-stage, single-ended op-amp with PMOS inputs with the following design specifications. The first stage is a differential pair with a current mirror load. The second stage is a common source amplifier. Use a simple current source with a diode-connected PMOS load as the bias circuit. Use Miller compensation and if necessary use zero cancelling resistor.

VDD = 3.3V
DC Gain ≥ 60 dB
GBW = as high as possible
Phase Margin ≥ 60 degrees
Slew Rate: as high as possible
Power Consumption ≤ 1.65 mW excluding bias circuit
CL = 5 pF
Input Voltage Swing: 0V to 1.4V
Output Voltage Swing: 0.3V to 2.7V
Input-referred Offset Voltage: as low as possible
Common Mode Rejection Ratio (CMRR): as high as possible
Power Supply Rejection Ratio (PSRR+/ PSRR-): as high as possible

Use the TSMC 0.35µm process. Simulate the design over typical, fast and slow process corners. The process corners are defined as:

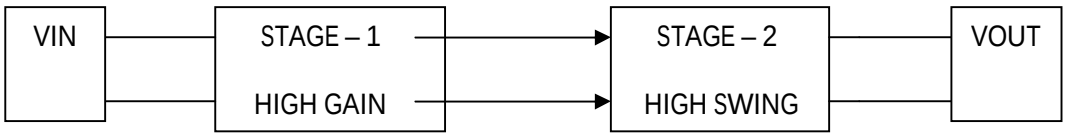
- The 'slow' corner (slow NMOS/slow PMOS parameters, 70 °C, 3.0 V)
- The 'fast' corner (fast NMOS/fast PMOS parameters, 0 °C, 3.6 V)
- Typical conditions (typical parameters, 27 °C, 3.3 V)

CIRCUIT DIAGRAM:



SUMMARY:-

A two-stage opamp configuration isolates the gain and swing requirements. The 1st stage provides high gain while the second stage gives large swings.



The first stage, however, consists of a mirror pole at node 2 in the above circuit diagram. Also, the differential pairs using active current mirrors exhibit a zero located at twice the mirror pole frequency.

The greater the spacing between the Gain Crossover Frequency and the Phase Crossover Frequency, the more stable the feedback system is. The above observation leads to the concept of phase margin. To improve the latter, Miller Compensation and Zero Cancelling Resistor have been used. The former moves the output pole away from the origin and moves the dominant pole towards the origin. This effect is called Pole-Splitting. The zero in the right half plane slows down the drop of the magnitude, thereby pushing the gain crossover away from the origin. To avoid this, a zero cancelling resistor with a value $Rz=gm_9^{-1}$ is used. In practice, the zero can even be moved into the left half plane so as to cancel the 1st non-dominant pole.

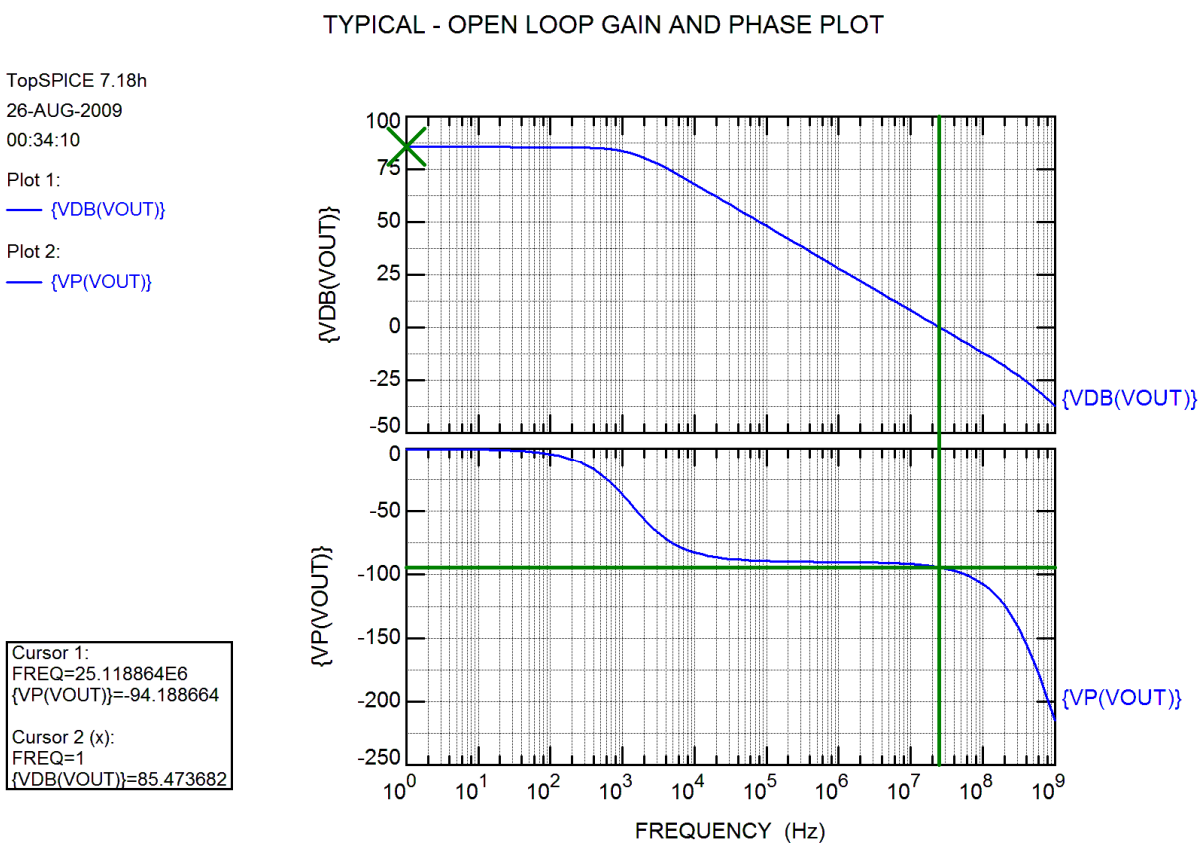
However, the process of cancelling the non-dominant pole has 2 important drawbacks:

1) If CL is unknown or variable, it is difficult to fix the value of Rz.

2) Rz, typically realised by a MOS transistor in triode region, changes substantially as output voltage excursions are coupled through Cc to node 5, thereby degrading the large-signal settling response.

SPECIFICATION	TYPICAL T=27C,Vdd=3.3V	SLOW CORNER T=70C,Vdd=3V	FAST CORNER T=0C,Vdd=3.6V
➢ DC Gain	**85.47 dB**	**82.45 dB**	**87.3 dB**
➢ Unity Gain Bandwidth	**25.11 MHz**	**19.95 MHz**	**31.62 MHz**
➢ Power Consumption (excluding Bias Circuit)	**0.5 mW**	**0.4464 mW**	**0.554 mW**
➢ Phase Margin	**85.47º**	**82.31º**	**87.9º**
➢ Static Current Consumption	**0.052 mA**	**0.1488 mA**	**0.1539 mA**
➢ Slew Rate	**14.82 V/us**	**12.56 V/us**	**17.77 V/us**

WAVEFORMS:-



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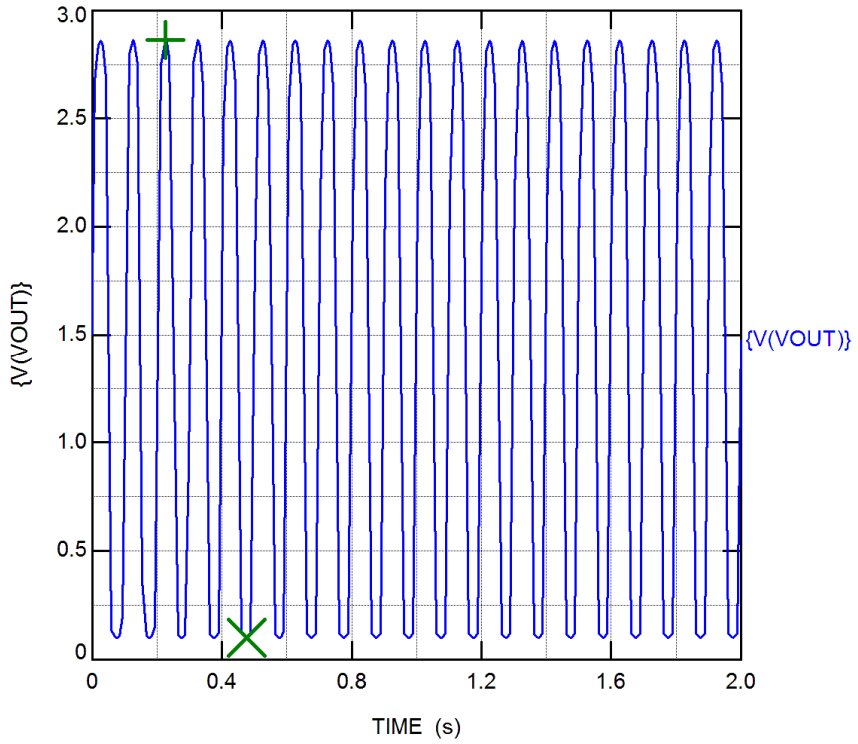
TYPICAL - OUTPUT SWING

TopSPICE 7.18h
26-AUG-2009
00:41:12

—— {V(VOUT)}



Cursor 1 (+):
TIME=225m
{V(VOUT)}=2.8629198

Cursor 2 (x):
TIME=475m
{V(VOUT)}=99.100299m

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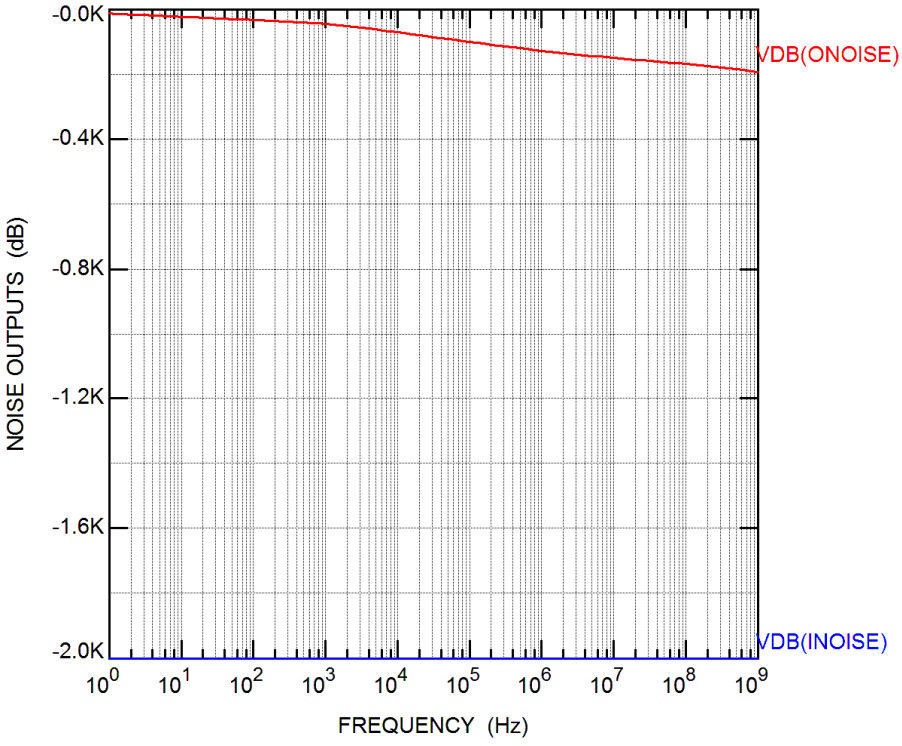
TYPICAL - NOISE SPECTRUM

TopSPICE 7.18h
26-AUG-2009
00:43:40

—— VDB(INOISE)
—— VDB(ONOISE)



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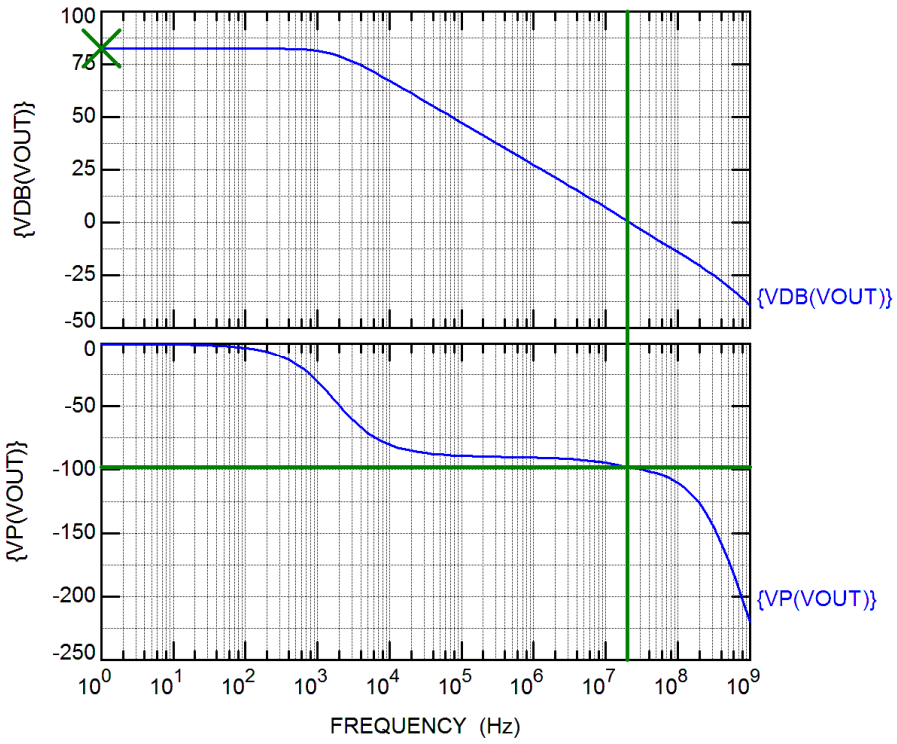
SLOW CORNER - OPEN GAIN LOOP AND PHASE PLOT

TopSPICE 7.18h
26-AUG-2009
00:49:52
Temp=70

Plot 1:
—— {VDB(VOUT)}

Plot 2:
—— {VP(VOUT)}



Cursor 1:
FREQ=19.952623E6
{VP(VOUT)}=-97.693258

Cursor 2 (x):
FREQ=1
{VDB(VOUT)}=82.453656

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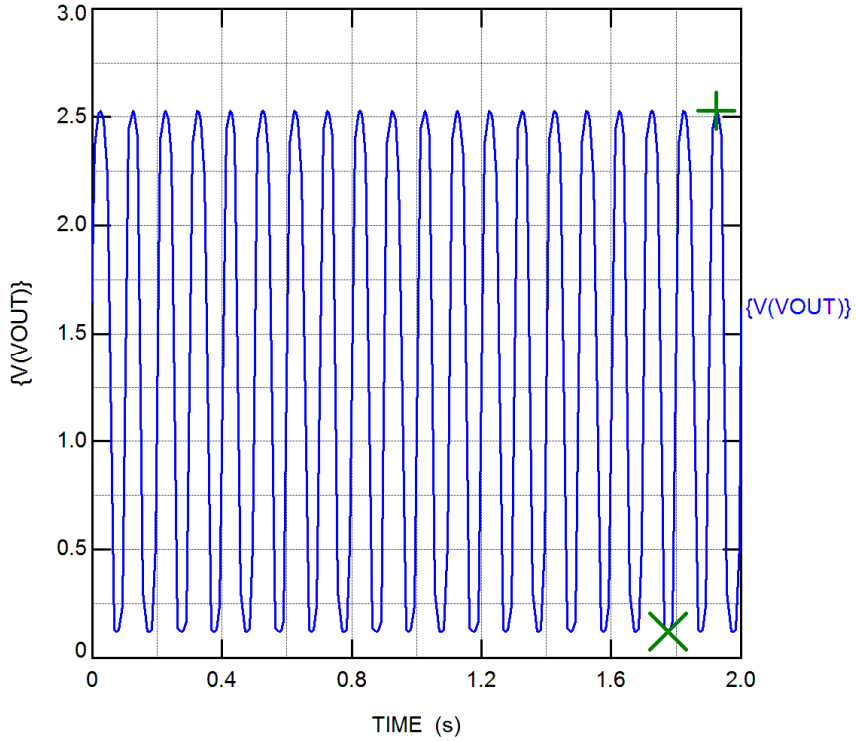
SLOW CORNER - OUTPUT SWING

TopSPICE 7.18h
26-AUG-2009
00:53:41
Temp=70

—— {V(VOUT)}



Cursor 1 (+):
TIME=1.925
{V(VOUT)}=2.5296236

Cursor 2 (x):
TIME=1.775
{V(VOUT)}=119.71876m

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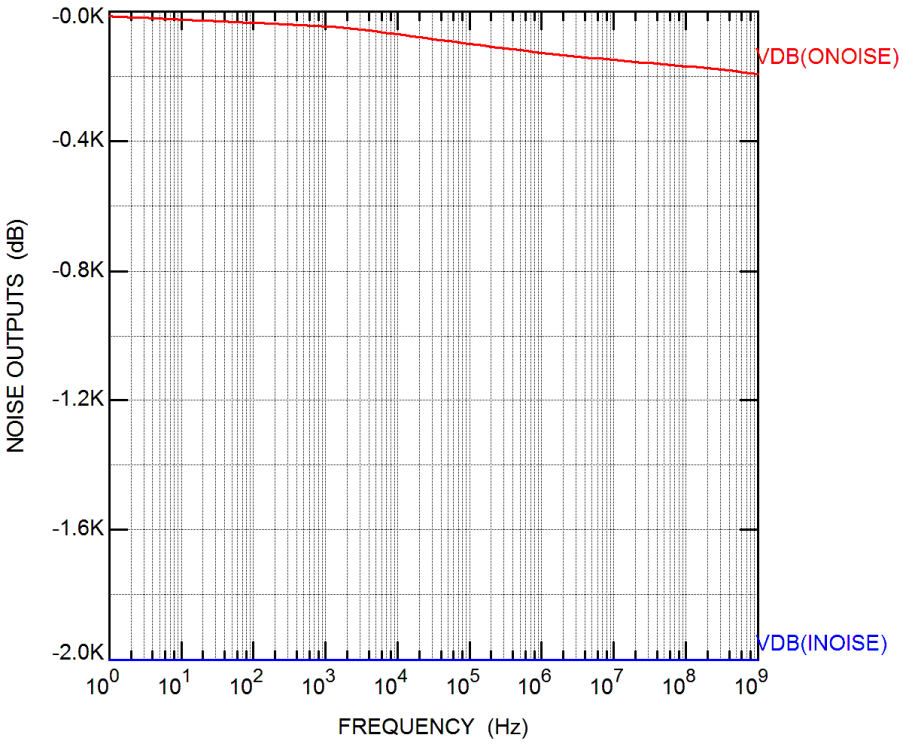
SLOW CORNER - NOISE SPECTRUM

TopSPICE 7.18h
26-AUG-2009
00:57:16
Temp=70

VDB(INOISE)
VDB(ONOISE)



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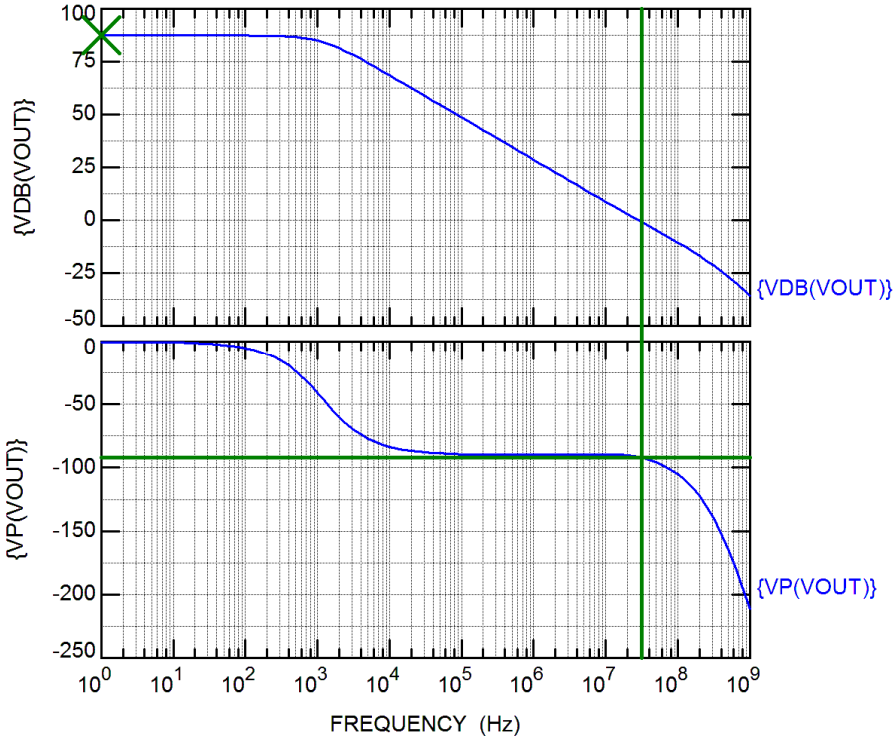
FAST CORNER - OPEN LOOP GAIN AND PHASE PLOT

TopSPICE 7.18h
26-AUG-2009
00:59:03
Temp=0

Plot 1:
{VDB(VOUT)}

Plot 2:
{VP(VOUT)}



Cursor 1:
FREQ=31.622777E6
{VP(VOUT)}=-92.068304

Cursor 2 (x):
FREQ=1
{VDB(VOUT)}=87.291754

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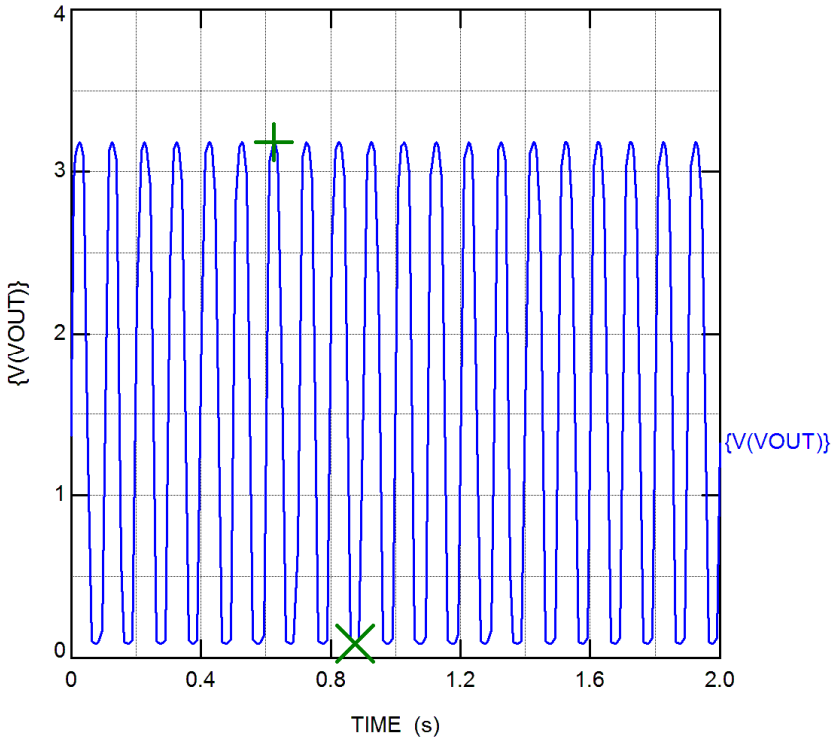
FAST CORNER - OUTPUT SWING

TopSPICE 7.18h
26-AUG-2009
01:03:15
Temp=0

—— {V(VOUT)}



Cursor 1 (+):
TIME=625m
{V(VOUT)}=3.183371

Cursor 2 (x):
TIME=875m
{V(VOUT)}=86.871681m

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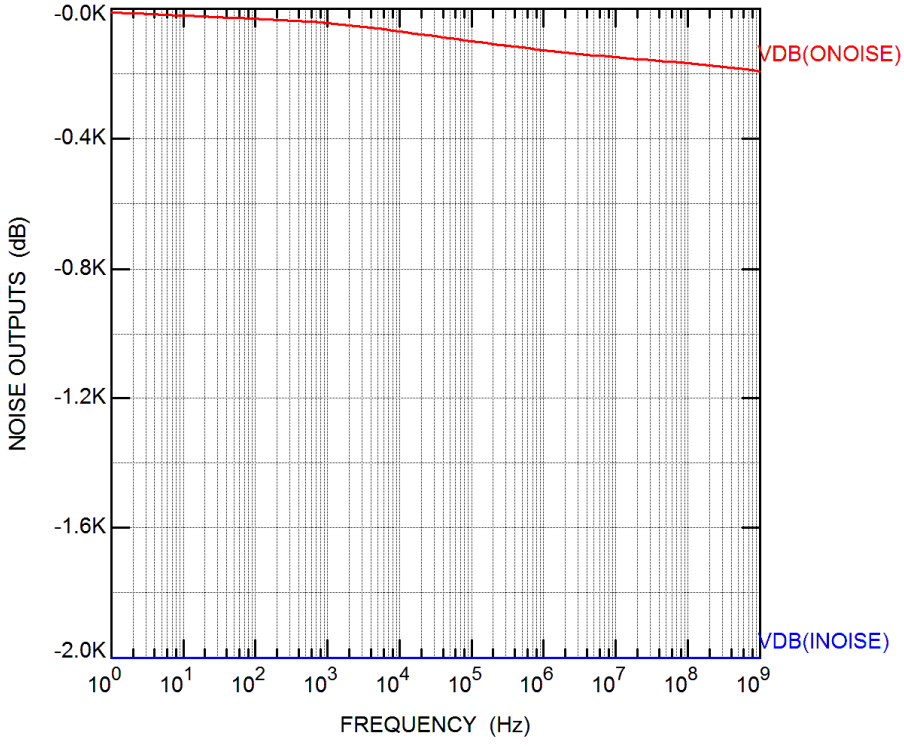
FAST CORNER - NOISE SPECTRUM

TopSPICE 7.18h
26-AUG-2009
01:04:29
Temp=0

—— VDB(INOISE)
—— VDB(ONOISE)



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REFERENCES:

- Design of MOS Operational Amplifier Design by P.Gray and R.Meyer
- Design of Analog Integrated Circuits, Behzad Razavi.