DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

MONSOON Semester | ECE 315/ ECE515: Analog CMOS Circuit Design | 2023 – 2024

Time: 2 hours | **End-Semester Exam** | **M.M.: 30**

Instructions: All questions carry sufficient information. **No further information will be provided during the exam.** Please answer all parts of the same question together at the same place, not here and there.

1. For the circuit shown in Fig. 1, V_{DD} = 1.8 V, R_D = 500 Ω and transistor M_1 is characterized by the following parameters: μC_{ox} = 200 μA/V^2, V_{TH} = 0.4 V, λ = 0, γ = 0. The circuit provides an input impedance of 50 Ω.
   (a) What is the output resistance of the circuit? **[1+1+2+1]**
   (b) What is the value of maximum allowable of drain current?
   (c) Calculate the required value of W/L for the maximum allowable value of drain current.
   (d) Compute the voltage gain.

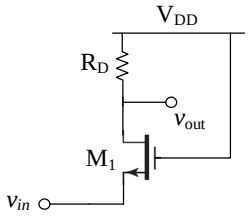

Fig. 1

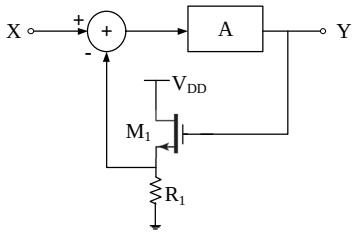

Fig. 2

2. (a) Find the loop-gain of the circuit shown in Fig. 2 where A is given as open-loop gain. Assume λ = 0, γ = 0 for M_1.
   (b) Find the small signal gain of the amplifier shown in Fig. 3. Assume λ ≠ 0, γ = 0 and $g_m r_o$ >> 1 for all the transistors. **[2+3]**

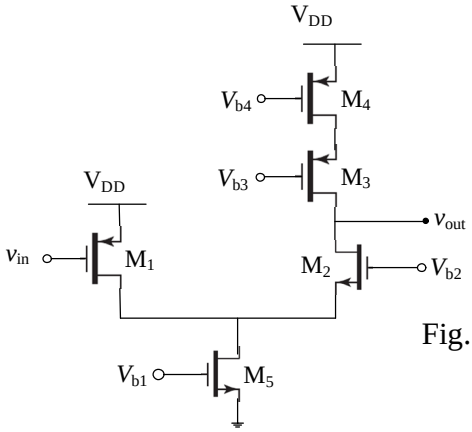

Fig. 3

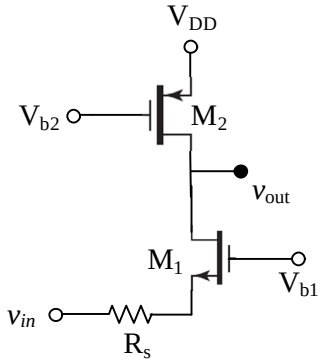

Fig. 4

3. Let us assume that the circuit in Fig. 4 is given for frequency response analysis.
   (a) Identify the capacitors, which experience Miller effect, if there is any. **[2+3]**
   (b) Identify the poles by inspection. Assume λ = 0, γ = 0 for M_1, λ ≠ 0, γ = 0 for M_2 and $g_m r_o$ >> 1 for all MOS devices.

4. (a) What are the usual bias conditions for the NMOS device shown in Fig. 5 to operate in deep triode region?
   (b) Neglecting all other capacitances, find the output impedance of the circuit shown in Fig. 6. Assume λ = 0, γ = 0 for the transistor and I_S is an ideal current source. **[1+2+2]**

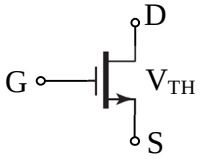

Fig. 5

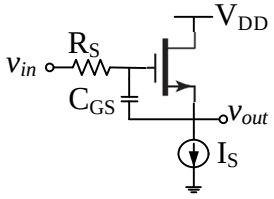

Fig. 6

(c) Draw the small-signal equivalent model for the circuit shown in Fig. 7 with proper labeling. Assume $\lambda \neq 0$ and $\gamma = 0$ for both the transistors.

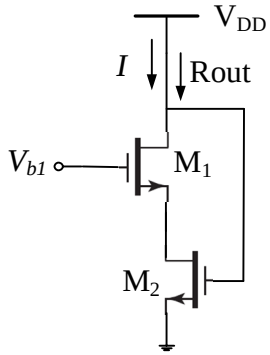

Fig. 7

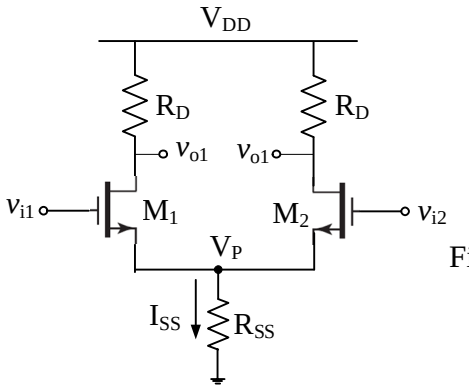

Fig. 8

5. For the circuit shown in Fig. 8, $V_{DD} = 3$ V, $R_{SS} = 500\ \Omega$, $(W/L)_{1,2} = 25/0.5$, $(\mu C_{ox})_{1,2} = 50\ \mu A/V^2$, $V_{TH1,2} = 0.6$ V. Assume $\lambda = 0$, $\gamma = 0$ for all the MOS devices. **[2+2+1]**
   (a) What is the required input CM voltage for which V_P can be at least 0.5 V?
   (b) Calculate R_D for which the differential mode gain is 4.
   (c) Calculate the amount of voltage the transistors are away from entering the triode region.

6. (a) Calculate the output resistance (R_{out}) denoted in the circuit of Fig 7. Assume $\lambda \neq 0$ and $\gamma = 0$ for both the transistors. **[2+1+2]**
   (b) Give just one disadvantage of having large voltage headroom in a MOS circuit.
   (c) Assume all MOS devices in Fig. 9 are identical having threshold voltage V_{TH}, and $\lambda = 0$, $\gamma = 0$ for all of them. Find minimum allowable voltage at node P of the circuit to operate all the transistors in saturation.

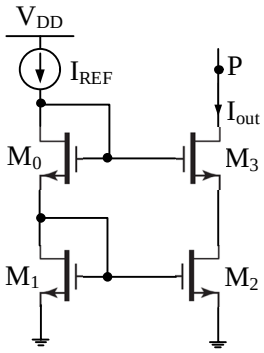

Fig. 9