Digital VLSI Design (ECE 314/514)
Mid-Sem 2023 Rubric

Q.1. Answer the following questions briefly.

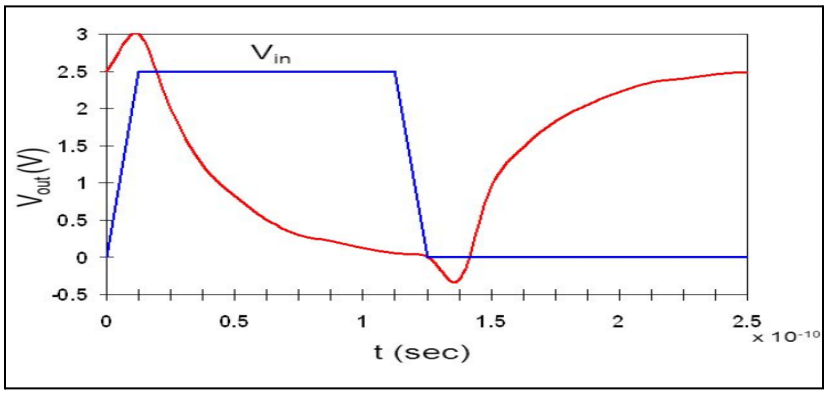
A. It is required to increase the propagation delay of a CMOS inverter. Without adding more stages or changing the sizes of the transistors, suggest how the delay can be increased. You can use additional NMOS/PMOSs? (1 mark)

Ans. We can make a stacked inverter by

1. adding one PMOS to the pull-up stack or one NMOS to the pull-down stack or
2. we can connect NMOS/PMOS as a capacitor to the output.

{either of the two responses is OK for getting 1 mark}

B. What is the reason for overshoots on the output signal of an inverter as shown in figure given below. (1 mark)



Ans. Overshoots in the output signal of an inverter's transient response occur due to **gate-drain capacitances** of the inverter transistors, which couple the steep voltage step at the input node directly to the output before the transistors can even start to react to the changes at input.

Or

Overshoots in an inverter's output signal during transient response occur due to the redistribution of charge when the input voltage is abruptly switched off. The transistors have an inversion layer in the "on" state. When the input voltage rapidly transitions to "off," the **charge accumulated in the inversion layer must be redistributed** between the source and drain regions. This redistribution process can lead to temporary voltage spikes or overshoots in the output signal as the charge dissipates.

{if any one of the above two is written - then 0.75 marks, if both, then 1 mark}

C. **A 10x unit-sized inverter driving a load of 100fF. The load is decreased to 1fF, the inverter's size is no longer effective. Why?. (1 mark)**

Ans. When a 10x unit-sized inverter initially drives a load of 100fF, the inverter's delay is mainly controlled by the large load capacitance. However, when the load is reduced to just 1fF, things change. The inverter's capacitance (diffusion capacitance) starts to dominate the extrinsic load i.e. 1fF. Hence large size inverter no longer helps in reducing the delay. It only makes the inverter larger in area. This effect is called **self-loading.**

Q2. Give reasons for the following: [CO1]

a) **We prefer to use strap cells instead of putting strap along every transistor in a standard cell library. (1 mark)**

Ans. The strap cell provides a low-impedance connection between the substrate and a power rail, in order to provide a stable substrate voltage at the body of a MOSFET.
To avoid latch-up, substrate resistance needs to be low. Technology teams typically give a DRC of a few 10s of microns for the frequency of substrate connections. *{0.25 marks}*
We prefer to use strap cells at a regular frequency instead of putting strap along every transistor to reduce the area loss that would happen if strap connections are added with every transistor. *{0.75 marks}*
This optimization helps improve the overall layout density of the chip, allowing for more functionality in a given silicon area.

b) **We leave only ½ DRC spacing from the pr-boundary when designing standard cell layouts. (1 mark)**

Ans. In standard cell topology, standard cells are abutted with each other.
Even if one leaves ½ the minimum DRC requirement across cell sharing, then after abutment, 1 full DRC is met. *{0.25 marks}*
Alternately, if a designer leaves full DRC from the pr-boundary, then after abutment 2 DRC spacing will appear in features close to the abutment boundary.
The method of leaving ½ DRC saves area while still achieving DRC clean layouts. *{0.75 marks}*

c) **While the height of standard cells is fixed, the width of standard cells changes in discrete units linked to DRC of wires. (1 mark)**

Ans. Standard cells have fixed height so that they can be placed in a row so VDD and GND can be shared, and it will be easier for the placement and route tool to generate automatic layouts.
The height of a standard cell is determined by the number of metal lines that need to be routed through the cell. Like when the Metal-2 (M2) layer is used in standard cells, it is typically drawn horizontally over the cell, and hence, the width of the cell is governed by the pitch of the M2 layer. The pitch of the M2 layer is equal to the **M2 wire width + 2*(½ DRC spacing for M2)**. Therefore, the height of standard cells is in multiples of M2 pitch. *{0.5 marks}*
Similarly, in a typical design methodology, M3 layer would be drawn vertically. To enable maximum routability of M3 over the standard cells, standard cell width increases in the multiples of (M3 wire width + 2*(½ DRC spacing for M3)) *{0.5 marks}*

d) **The diffusion layer of a PMOS device is overlaid with p+ layer in CAD. However, strap for the n-well has n+ layer on the diffusion. (2 mark)**

Ans. The p+ layer is heavily doped with p-type dopants, which increases the hole concentration in this region. In older technologies, this results in a **reverse-biased pn-junction** and enables transistor action. *{0.5 marks}* In advanced technology, this doping is still higher to maintain aspect ratio of the channel and reduce body effects.

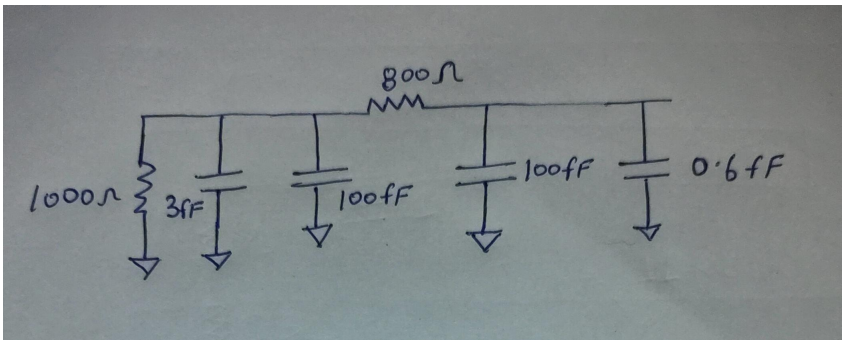
When one desires to connect the substrate to a supply, it is important to provide a low resistance contact without any voltage drop across it. If p+ doping of source and drain is used to provide substrate connection, then there will be a drop of **built-in potential** across the reverse biased junction. So, substrate connection will be ineffective. *{0.5 marks}*

On the other hand, n+ doping provides the required **low resistive contact** with the substrate supply. *{1 mark}*

Q3. A 10x unit-sized inverter drives a 2x inverter at the end of the 1 mm wire. Suppose that wire capacitance is 0.2 fF/μm and resistance is 800Ω and that unit-sized nMOS transistor has R= 10 KΩ and C=0.1 fF. Estimate the propagation delay using the Elmore delay model. (use wire modeled as π model). [CO1 & CO2] (5 mark)

The driver has a 10-unit nMOS transistor and a 20-unit pMOS transistor**,** The 10X driver has a resistance of **10kohm/10=1kohm** and an output Capacitance of **30*0.1fF=3fF**. The receiver has a 2-unit nMOS transistor and a 4-unit pMOS transistor so input capacitance is **6*0.1fF=0.6 fF**. The wire capacitance is 200 fF and the resistance of 800ohm. *{1.5 mark}*

The figure below shows an equivalent circuit for the system using a single-segment pi-model.



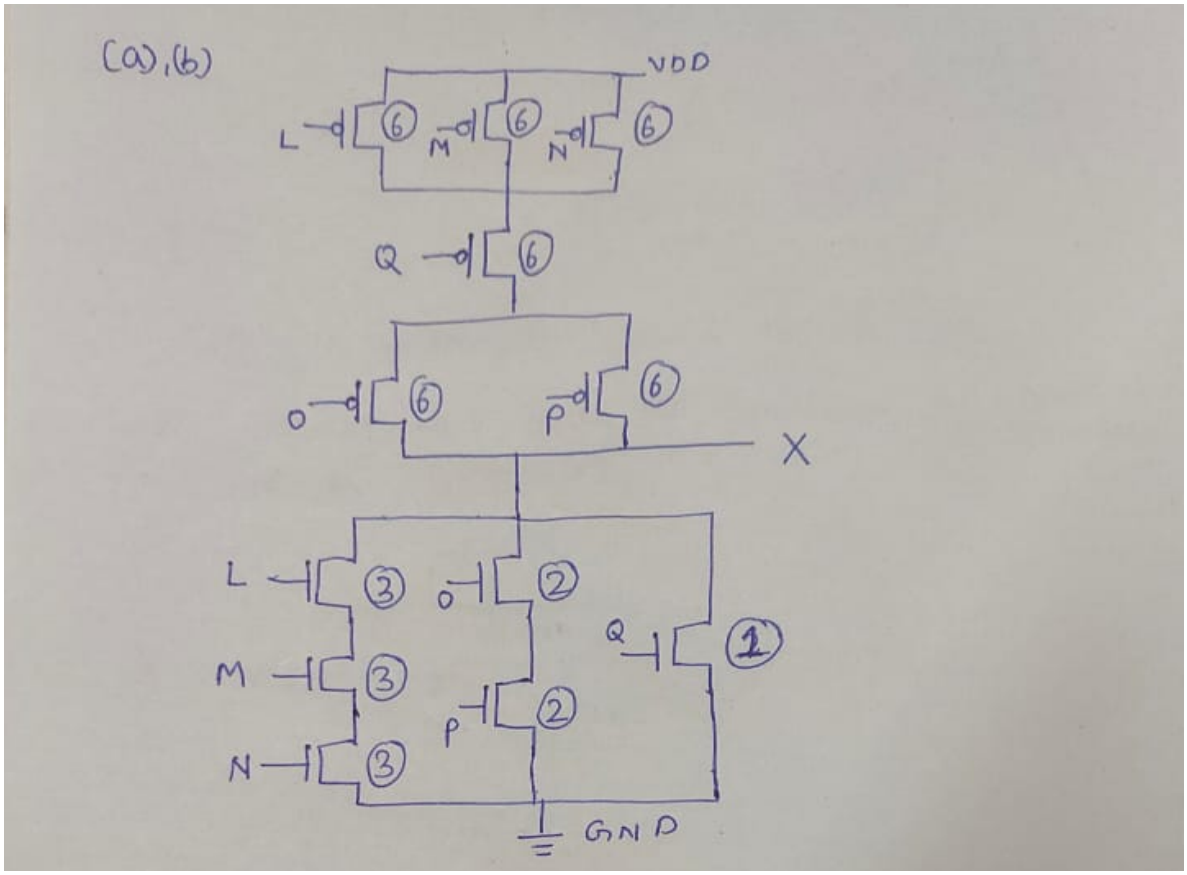
{1 mark}

The **Elmore delay** is tpd = (1000ohm)(103 fF) + (1000ohm + 800 ohm)(100 fF +0.6 fF) = **284.08 ps.** *{2.5 mark}*

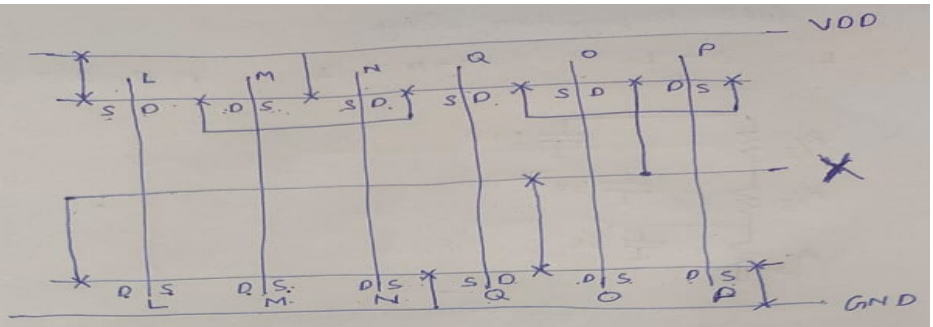
The capacitance of the long wire dominates the delay; the capacitance of the 2x inverter and 10x inverter is negligible in comparison

Q4. Answer the following questions: [CO2]

a) **Draw schematic for the CMOS logic given by (LMN +OP+Q)' (1 mark)**
b) **Size the transistors to match the resistance of a unit inverter and show on the schematic. (1 mark)**
c) **Draw the stick diagram considering appropriate sharing of source and drain regions. (consider N input close to GND supply) (1 mark)**
d) **Calculate the logical effort for inputs L and Q (1 mark)**
e) **Estimate the propagation delay for change in input L rise and fall in terms of R and C. (1 mark)**
f) Estimate the contamination delay for change in input N rise and fall in terms of RC. (2 marks)



(c)



(d)

Logical Effort for L ⇒

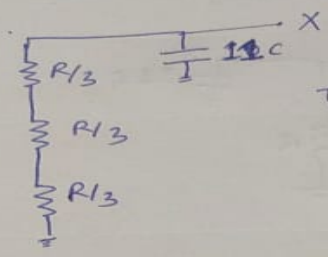
$$g = \frac{9C}{3C} = 3$$

Logical Effort for Q ⇒

$$g = \frac{7C}{3C} = 2.33$$

(e) (i) fall Propogation delay

L = 0 - 1 M = N = 1 P, Q, O = 0



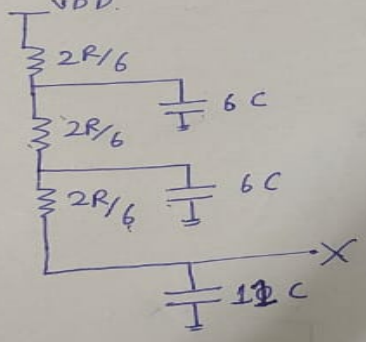
$\tau_{fall} = 11RC$

(ii) rise Propogation delay

L = 1 - 0

M = N = P = 1

O, Q = 0



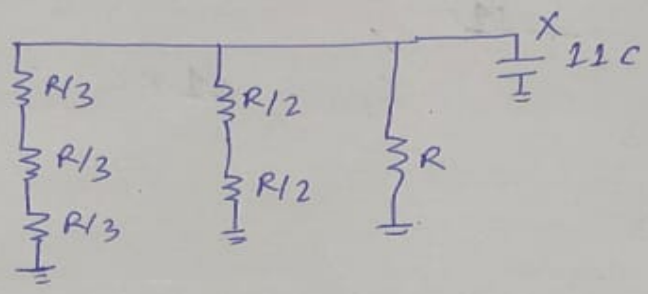
$$\tau_{rise} = R \times 11C + \frac{4R}{6} \times 6C + \frac{2R}{6} \times 6C$$

$$= 17RC$$

(f) (i) fall contamination delay

$N = 0 - 1$

$L, M, O, Q, P = 1$

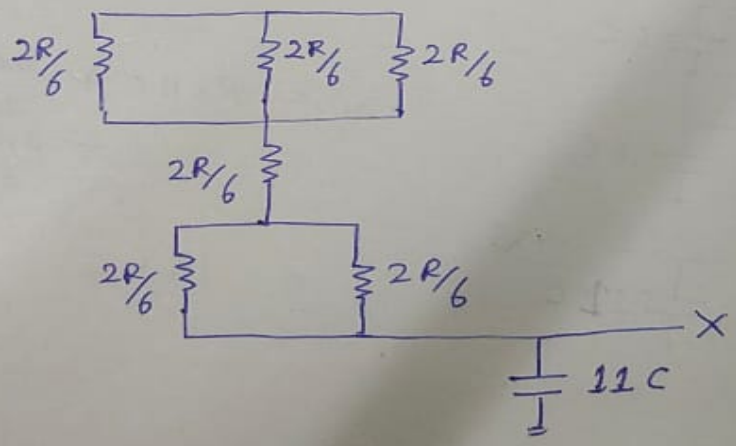


$T_{fall} = \frac{11}{3} RC$

(ii) rise contamination delay

$N = 1 - 0$

$L, M, O, Q, P = 0$

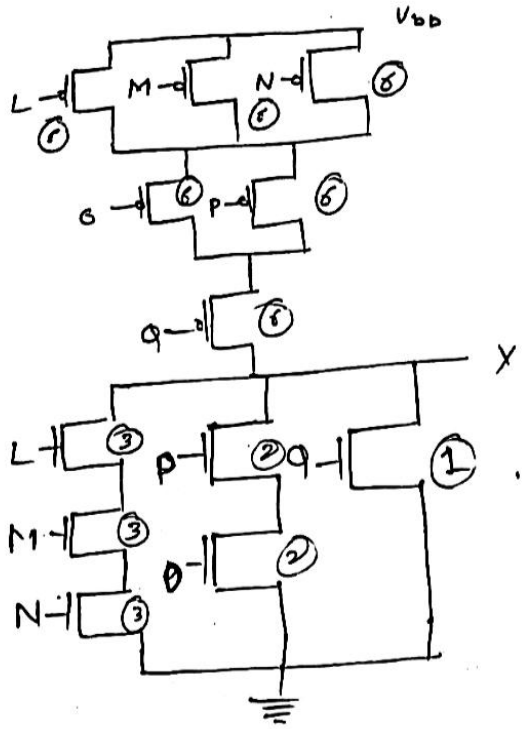


$T_{Rise} = \frac{121}{18} RC$

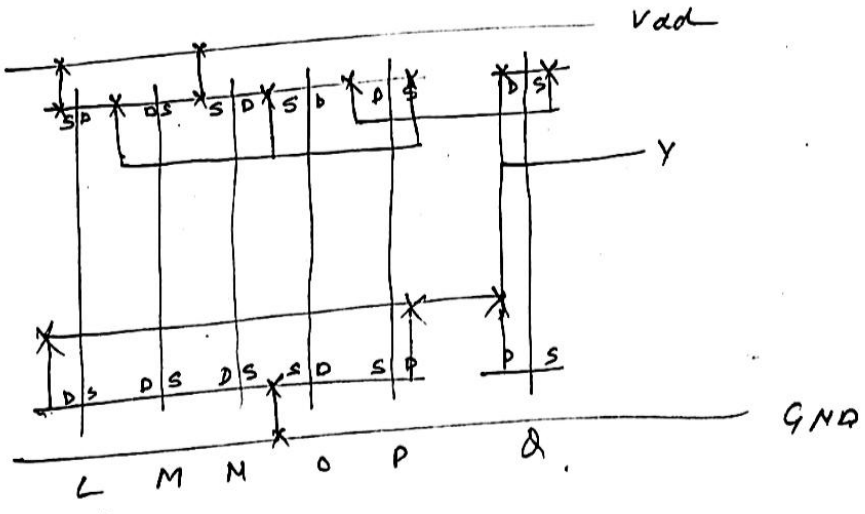
OR

a>

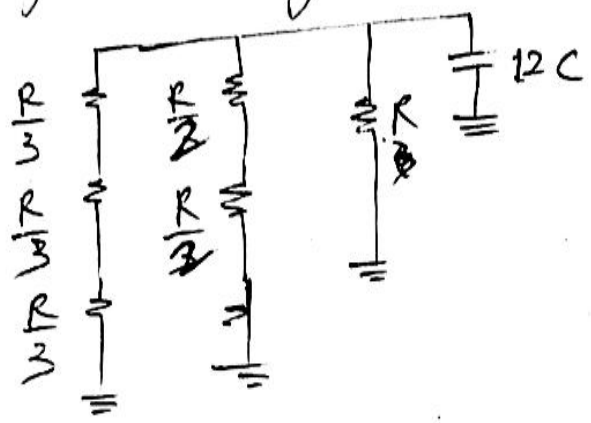
b>



c>

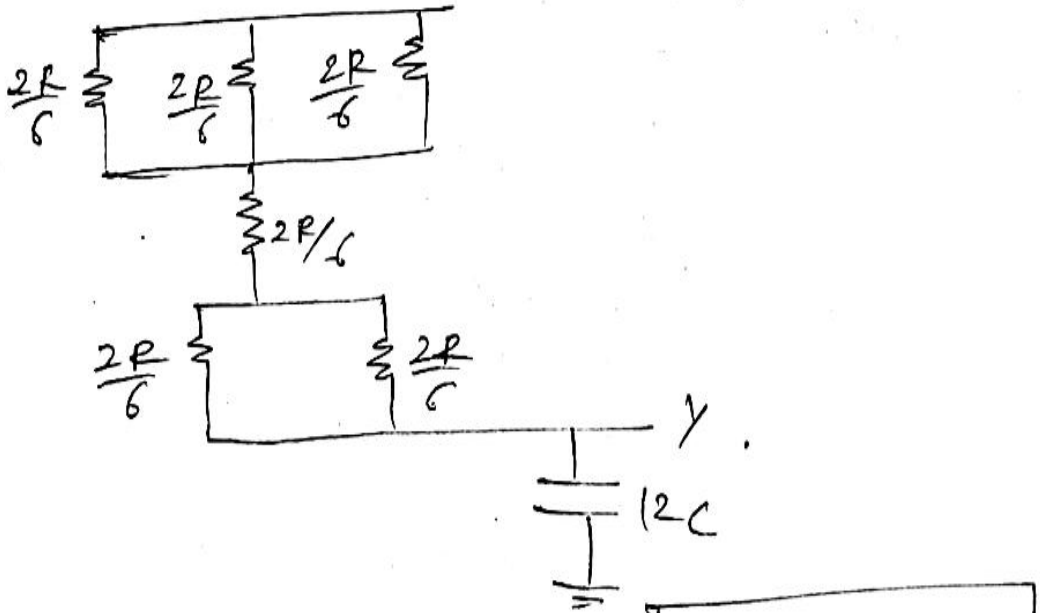


f7 fall cont delay



$$\tau_{fall} = 4RC$$

rise cont delay



$$\tau_{rise} = \frac{.13L\,RC}{18}$$

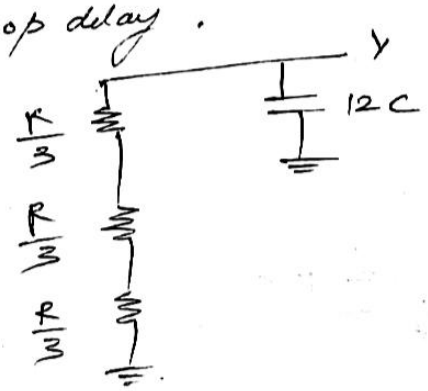
d) Logical effort for L →

$$g = \frac{9C}{3C} = 3$$

for Q

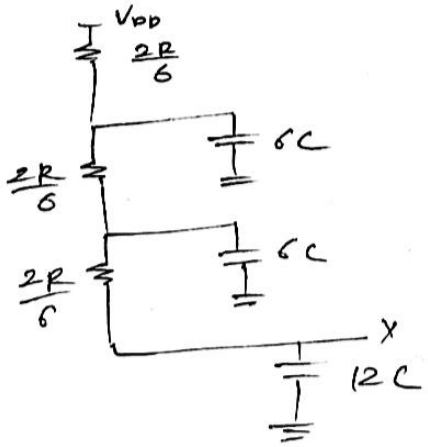
$$g = \frac{7C}{3C} = 2.33$$

e) fall prop delay.



$12RC = \tau_{fall}$

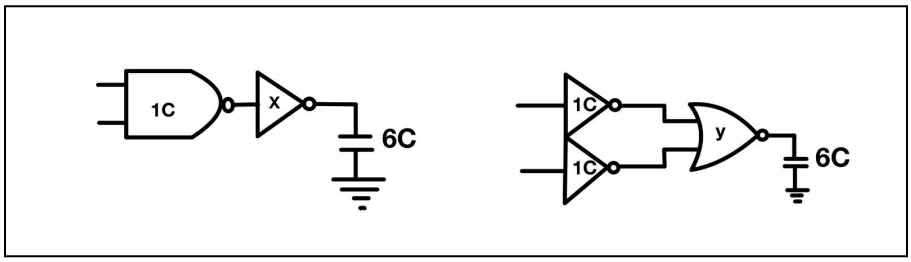
rise prop delay.



$12RC + \frac{4R}{6}6C + \frac{2R}{6}6C$

$18RC = \tau_{rise}$

Q5. Consider the two designs of a 2-input AND gate shown in Figure below. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the path effort, delay and input capacitances x and y to achieve this delay. [CO2] **(4 marks)**



(a) should be faster than (b) because the NAND has the same parasitic delay but lower logical effort than the NOR. *{1 mark}*

In each design, H = 6, B = 1, P = 1 + 2 = 3.

For (a), G = (4/3) * 1 = (4/3).

F = GBH = 8.

f = 8^1/2 = 2.8.

D = 2f + P = **8.6**τ. *{0.5 marks}*

x = 6C * 1 / f = **2.14C**. *{1 marks}*

For (b), G = 1 *(5/3).

F = GBH = 10.

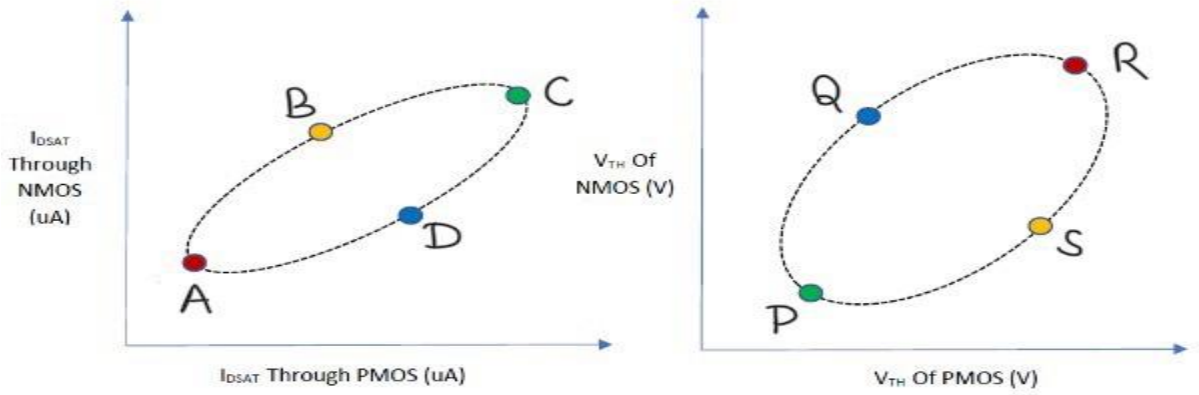
f = 10^1/2 = 3.2.

D = 2f + P = **9.3**τ**.** *{0.5 marks}*

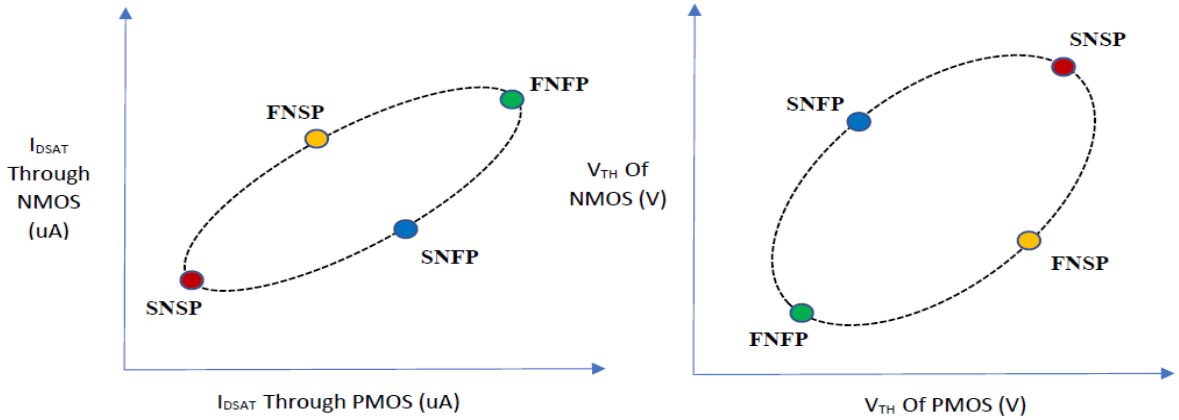
y = 6C * (5/3) / f = **3.16C** *{1 marks}*

Hence design (a) is faster.

Q6. Identify the location of SNSP, SNFP, FNSP, FNFP process corners on the curve for the given 2 distributions? [CO2] (4 marks)



Answer:



A- SNSP; B- FNSP; C- FNFP; D- SNFP

P- FNFP; Q- SNFP; R- SNSP; S- FNSP

{0.5 marks for every correct response}