DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

MONSOON Semester | ECE 315/ ECE515: Analog CMOS Circuit Design | 2023 – 2024

**Time: 1 hour** | **Mid-Semester Exam** | **M.M.: 25**

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**Instructions:** All questions carry sufficient information. **No further information will be provided during the exam.** Please answer all parts of the same question together at the same place, not here and there.

1. (a) For the circuit shown in Fig. 1, both transistors are characterized by the following parameters $\mu C_{ox} = 100\ \mu A/V^2$, $I_{bias} = 1$ mA, $(W/L) = 20/0.18$, $\lambda = 0$, $\gamma = 0$ and $R_D = 500\ \Omega$. What is the gain of the circuit? **[4+2]**
   (b) Is the circuit shown in Fig. 2 a current mirror circuit? Justify your answer in 2-3 sentences.

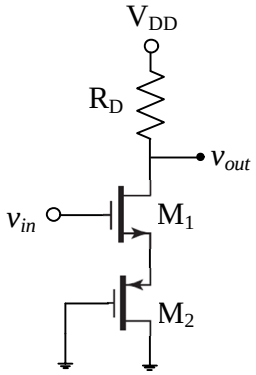


Fig. 1

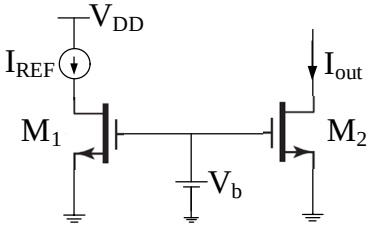


Fig. 2

2. For the circuit shown in Fig. 3, $V_{DD} = 1.8$ V, and $R_D = 500\ \Omega$. Assume $\mu_n C_{ox} = 100\ \mu A/V^2$, $V_{TH} = 0.4$ V, $\lambda = 0.1\ V^{-1}$, $\gamma = 0$ and $g_m r_o >> 1$ for both the transistors but $(W/L)_1 = 20/0.18$, $(W/L)_2 = 40/0.18$. **[4+3]**
   (a) What is the highest allowable value of $V_{b1}$ for $I_D = 1$ mA and both the transistors to be in saturation?
   (b) Calculate the small signal output resistance $R_{out}$.

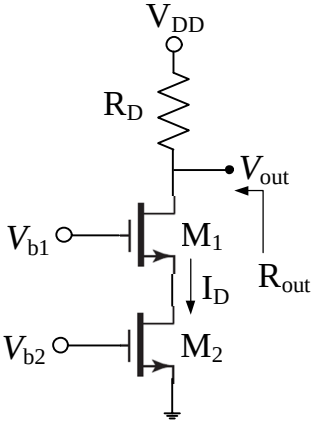


Fig. 3

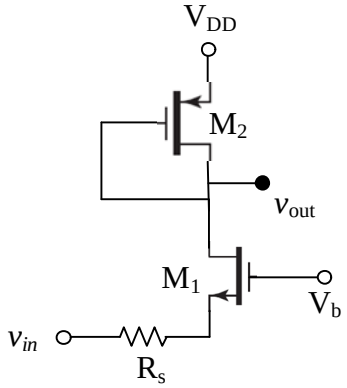


Fig. 4

3. Assuming all the MOSFETs in Fig. 4 are in saturation and $\lambda = 0$, $\gamma = 0$,
   (a) draw a simplified small-signal equivalent model of the circuit in Fig. 4. **[3+4]**
   (b) calculate the small-signal voltage gain of the circuit.

4. (a) Determine the voltage gain of the circuit in Fig. 5 preferably without using its detailed small-signal model. Assume $\gamma = 0$ and $g_m r_o >> 1$ for all the MOSFETs. **[3+1+1]**

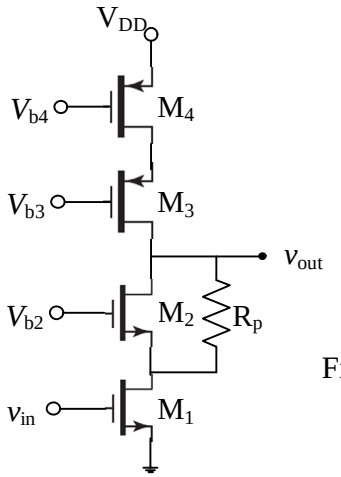


Fig. 5

(b) Out of the following four single-stage MOS amplifiers with resistive loads, which one gives the lowest input resistance?

(i) common-source, (ii) common-gate, (iii) common-drain, (iv) common-source with source degeneration

(c) Among the above four single-stage amplifiers, which one ensures better linearization in output current?