Digital VLSI Design (ECE 314/514)
Review Quiz-1 Rubric

Date: 21-8-2023 **Time:3:00 pm**
Duration: 15 minutes **Max Marks: 10**

Q.1. Fill in the blanks (5 marks)

a) **193 nm** wavelength of light is used for photholithography in 32nm technology.
b) Copper Interconnects are formed using the **Dual Damascene** process.
c) **Optical proximity correction/ Resolution Enhancement Techniques** is used to reduce the effect of diffraction so that resolution of patterns can be enhanced.
d) **Moore's Law**, **Dennard Scaling**, and Pollack's Law form a virtuous cycle to increase value offered by electronics
e) The three steps that are repeated over and over again during VLSI fabrication process are: **oxidation, implantation, and patterned removal (etching).**

Q.2. Why is verification required after every design step in the VLSI Design flow? (1 marks)

VLSI Design is very complex. It's important to verify design after every step to identify any mistakes early and cost of rework in the later stages. The cost of correcting a mistake increases as we go closer to the fabrication stage. Iterative steps allow the designer to verify at every step if the functionality and performance of the circuit meet the expectation.

Q.3. Why is the cost of mask set for advanced technology nodes very high? (1 marks)

The cost of mask sets for advanced technology nodes like 32nm or 22nm is high because these nodes involve intricate designs with smaller features, demanding complex manufacturing processes, advanced lithography methods, precise and more no. of mask creation, and increased inspection. These factors, along with design complexity and rapid technology changes, contribute to the overall expense of producing chips at these nodes.

Q.4. Multiple select Questions. (Please note that marks will be awarded only if all the options marked correctly) (3 marks)

I) Why are vias now made of copper and not tungsten?

a) Copper is less resistive
b) Fabricating vias with copper does not disturb energy bands in the substrate
c) Copper has higher ductility
d) In Dual-damascene process that can be enabled with Copper, both via and metal can be made in a single step which improves Yield

<u>Ans.</u> (a,b,c,d)

All these reasons are relevant.

Copper - being more ductile - can be deposited using the dual damascene process, therefore reducing alignment related Yield losses (which are high at advanced technology nodes).

Also, as the size of features reduces, resistance of Tungsten becomes very high and adversely affects performance. Using copper vias and wires avoids such performance degradation.

II) Which of the following is true with respect to the rotated substrate?

a) Crystals have anisotropic properties. So, conductivity changes when the direction of flow of current changes.
b) Centrifugal forces that come into the picture due to the rotation of substrate increase the speed of holes
c) When the direction of current flow changes, heavy holes start to behave as light, and their mobility increases.
d) Electron mobility is not impacted in rotated substrates.

Ans. (a,c,d)

Mobility of carriers does not change, with centrifugal forces coming into picture. Mobility is a material property that primarily depends on factors like the material's crystal structure, impurities, temperature, and the presence of electric fields

III) **Which factor determines the diameter of the wafer in the Czochralski process?**

a) Orientation at which the seed is dipped into the molten silicon
b) Speed at which the ingot is pulled out
c) Purity of the molten silicon used
d) Size of the initial seed used

Ans.(b) *Speed at which ingot is pulled out limits the diameter of the wafer... Slow speed results in larger diameter as more silicon solidifies in that duration*