

DVD Monsoon 2025: Quiz-4

Total points 8/10



Quiz Instruction

- The test will be live from **6:00 PM to 9:00 PM**.
- You must submit your response **before 9:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

Email *

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✗ Why are CMOS inverters more popular over BJT based inverters or Resistive load MOS inverter? *0/1

- CMOS inverters provide higher speed than BJT based inverters. ✗
- CMOS inverters have lower static power dissipation. ✓
- CMOS inverters have higher gain than BJT based inverters.
- CMOS inverters have higher noise immunity. ✓
- CMOS inverters have better rail to rail voltage swing. ✓

Correct answer

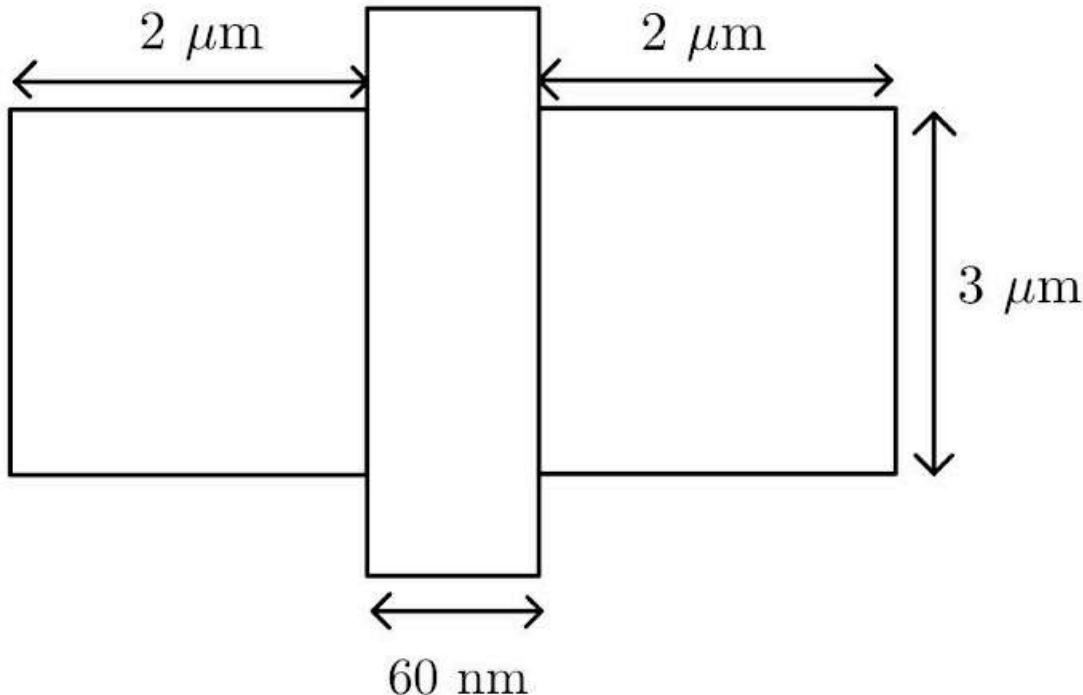
- CMOS inverters have lower static power dissipation.
- CMOS inverters have higher noise immunity.
- CMOS inverters have better rail to rail voltage swing.

Feedback

CMOS inverters have lower static power dissipation due to negligible gate current. They also have higher noise immunity and better rail to rail voltage swing as output reaches full logic levels (0 and VDD).



- ✓ For the given figure, $C_j=0.6 \text{ fF}/\mu\text{m}^2$, $C_{jsw}=0.3 \text{ fF}/\mu\text{m}$ and $C_{ox}=30 \text{ fF}/\mu\text{m}^2$. Which of the following values are correct? *2/2
 (All terms have their usual meaning as discussed in the class)



- Diffusion Capacitance, $C_{db}=5.7 \text{ fF}$ ✓
- $C_{ds}=2.7 \text{ fF}$
- When $V_{ds}=0$, $C_{gs}=2.7 \text{ fF}$ ✓
- When $V_{ds}=0$, $C_{gs}=1.8 \text{ fF}$
- Maximum gate capacitance, $C_g=5.4 \text{ fF}$ ✓
- Diffusion Capacitance, $C_{db}=6 \text{ fF}$
- $C_{ds}=1.8 \text{ fF}$
- Total Drain Capacitance, $C_d=7.8 \text{ fF}$
- When $V_{ds}=0$, $C_{gd}=1.8 \text{ fF}$
- Total Drain Capacitance, $C_d=8.4 \text{ fF}$ ✓
- When $V_{ds}=0$, $C_{gd}=2.7 \text{ fF}$ ✓



- Maximum gate capacitance, $C_g=3.6\text{ fF}$

Feedback

 Solution

Name *

Abhinav Maurya

✓ Which of the following statements are correct with respect to beta ratio *1/1 of CMOS inverter ?

At larger beta ratio, TPLH is low and TPHL is high.



At smaller beta ratio high noise margin NMH degrades.

At smaller beta ratio, TPHL is low and TPLH is high.



At larger beta ratio low noise margin NML degrades.

Feedback

At high beta ratio:

PMOS is stronger, thus TPLH is low and TPHL is high. Also NML is high and NMH is low.

At low beta ratio:

NMOS is stronger, thus TPLH is high and TPHL is low. Also NML is low and NMH is high.



✓ A CMOS metal layer has resistivity, 2×10^{-6} ohm-cm and height of metal layer is 0.8um. It is used to draw a wire which is 400um in length and 0.4um wide. Assuming current flows along length then how many squares N are there in this wire ? Also calculate the sheet resistance R_o and the resistance R of this wire.

R = 50 ohm

N = 250

R = 25 ohm



N = 500

$R_o = 0.05$ ohm

$R_o = 0.1$ ohm

Feedback

 Solution



✓ Which of the following statements are true regarding skewed gates? * 1/1

- We skew gates to improve the overall noise margin of devices.
- Skewed gates improve one of the noise margins NML or NMH while degrading the other. ✓
- Skewed gates favour either the rising or the falling edge at the expense of the other. ✓
- Low skew gates have better NMH compared to high skew gates. ✓

Feedback

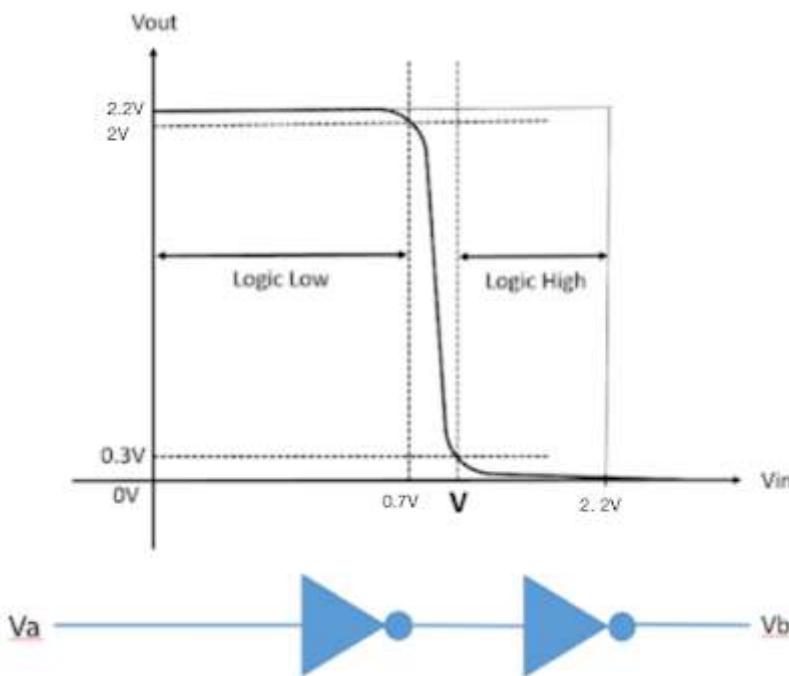
*Skewed gates favour either the rising or the falling edge at the expense of the other.
Skewed gates improve one of the noise margins NML or NMH while degrading the other.
Low skew gates have weaker PMOS, thus NMH is better compared to high skew gates.*

Roll Number *

2023024



- X** In the given there is a schematic shown in which two CMOS inverters are *0/1 connected in series. Both the CMOS inverters obey the given VTC as shown in figure. Input V_a is applied to be 0.7V. It is expected that the output V_b should lie in logic low region. What could be the possible values of voltage V labeled in VTC such that V_b lies in logic low region ?



- 0.9 V ✓
- 1.8 V ✓
- 2.2 V
- 2.1 V
- 2 V ✓
- 0.6 V
- 1.5 V ✓

Correct answer

- 0.9 V
- 1.5 V
- 1.8 V



2 V

Feedback

Since $V_a=0.7V$, we can see from the graph that output of 1st inverter will be 2V. Now we want this 2V to be treated as logic high input for next inverter so that V_b lies in low logic region. Since any value equal and greater than V will be treated as logic high input, we get $0.7V < V \leq 2V$

- Which of the following statements are false regarding post layout simulations? *1/1

- Delays may increase in post layout simulations because post-layout simulation models use higher threshold voltages for transistors. ✓
- Delays may decrease in post layout simulations due to sharing of source and drain regions, thus reducing the diffusion capacitances.
- Delays may increase in post layout simulations due to addition of parasitic capacitances and resistances.
- Delays may remain similar in post layout simulations as addition of parasitic capacitances/resistances is compensated by reduction in diffusion capacitances by sharing of source and drain regions.

Feedback

Delays may increase in post layout simulations due to addition of parasitic capacitances and resistances.

Or

Delays may decrease in post layout simulations due to sharing of source and drain regions, thus reducing the diffusion capacitances.

Or

Delays may remain similar in post layout simulations as addition of parasitic capacitances/resistances is compensated by reduction in diffusion capacitances by sharing of source and drain regions.



✓ Which of the following statements are incorrect regarding noise margin? * 1/1

- Improving low noise margin degrades high noise margin and vice versa.
- To increase low noise margin NML, we decrease low output voltage VOL which ✓ causes decrease in delays.
- To reduce the impact of noise, we use bigger devices, which causes increase in power consumption.
- Increasing noise margins causes increase in area as bigger devices are required.

Feedback

To increase low noise margin NML, we decrease low output voltage VOL which causes increase in delays as it takes more time to discharge.

To reduce the impact of noise, we use bigger devices, which causes increase in area and power consumption.

Improving low noise margin degrades high noise margin and vice versa.

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