Untitled form DVD Monsoon 2025:Quiz-10

Total points 7/10

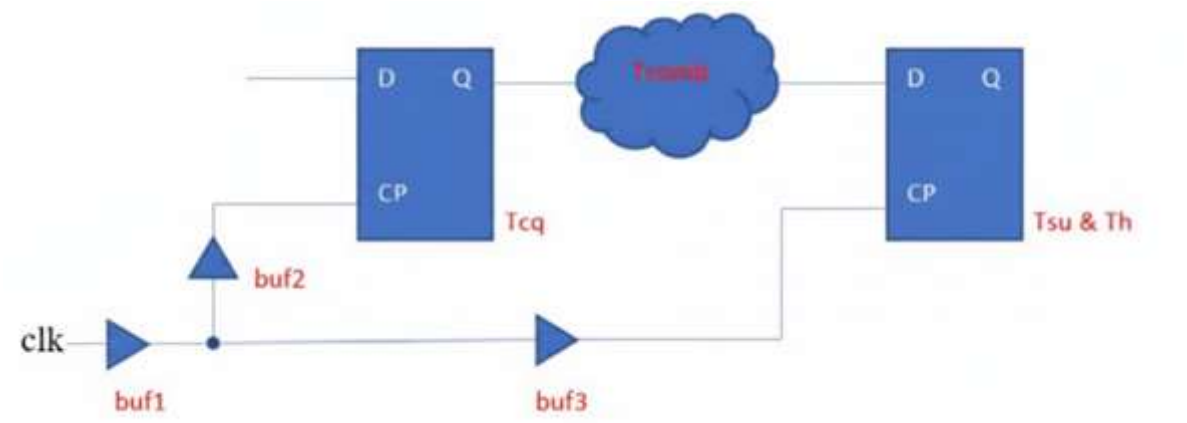
Quiz Instruction

- The test will be live from 6**:00 PM to 9:00 PM**.
- You must submit your response **before 9:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

✗ In the figure, three buffers, flip-flops, and a combinational circuit are shown. Each element has two delays: a **minimum delay** and a **maximum delay** (the maximum delay includes derating). Consider a **clock period of 8 ns**, and assume the **setup time and hold time are both 0.2 ns**. 0/2

buf1-> 0.70ns (max delay), 0.60ns (min delay)
buf2-> 0.65ns (max delay), 0.55ns (min delay)
buf3-> 0.75ns (max delay), 0.45ns (min delay)
Tcomb-> 3.6ns (max delay), 2.5ns (min delay)
Tcq-> 0.6ns (max delay), 0.48ns (min delay)



- [x] setup slack=3.4 ns, Hold slack=2.58 ✗
- [ ] setup slack =3.3, Hold slack = 2.58
- [ ] setup slack =3.9, Hold slack = 2.3
- [ ] setup slack =3.3, Hold slack = 2.48

Correct answer

- [x] setup slack =3.3, Hold slack = 2.48

✗ Given a **500 ps clock cycle** with **50 ps of clock skew** and assuming **no time borrowing**, calculate the maximum allowable logic delay for each of these sequencing methods:
a) Two-phase level-sensitive latches
b) Pulsed latches with an 80 ps pulse duration

0/1

	Setup Time	clk-to-Q Delay	D-to-Q Delay	Contamination D	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

- [ ] (a) 455 ps ; (b) 420 ps
- [ ] (a) 370 ps ; (b) 430 ps
- [ ] (a) 420 ps ; (b) 455 ps
- [x] (a) 400 ps ; (b) 455 ps ✗

Correct answer

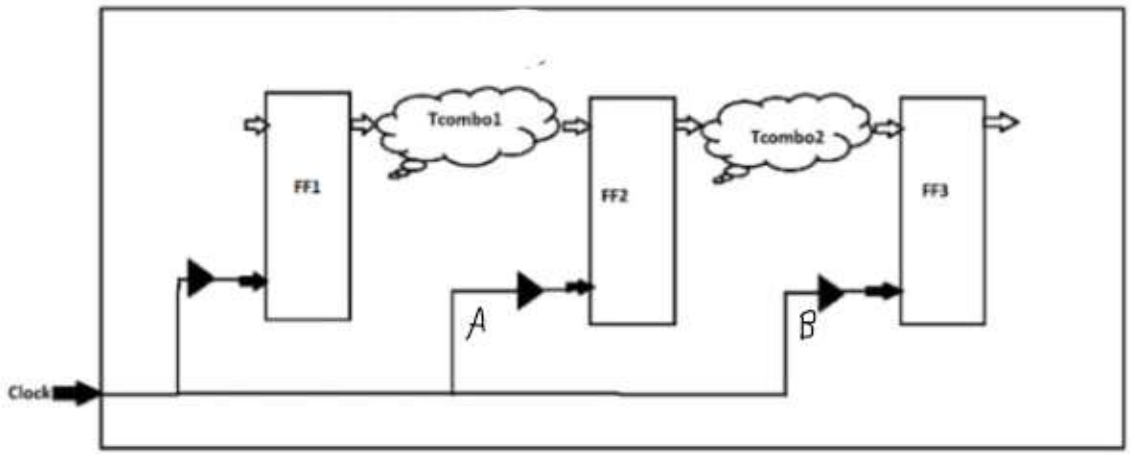
- [x] (a) 420 ps ; (b) 455 ps

✓ Consider the synchronous circuit shown below. 1/1

A single clock source drives three flip-flops: FF1 → FF2 → FF3.
The combinational delays are:
Comb1 = 300 ps (between FF1 and FF2) **Comb2 = 200 ps** (between FF2 and FF3)

Clock buffer delays are 0 ps.
Assume setup time and clock-to-Q delay are negligible for the setup-time analysis.

The clock distribution paths are labeled **A** (clock to FF2) and **B** (clock to FF3), as shown: determine the **minimum clock period** at which this circuit can operate without setup-time violation. We now want this circuit to operate at **4 GHz** To achieve this, you are allowed to introduce the useful skew.



- [ ] Circuit operates at 2GHZ and to operate at 4GHZ we need to add delay buffer of 20ps in the clock distribution path A .
- [ ] Circuit operates at 2.25GHZ and to operate at 4GHZ we need to add delay buffer of 20ps in the clock distribution path B.
- [ ] Circuit operates at 3.33GHZ and it is not possible to achieve the clock frequency of 4GHZ.

- [x] Circuit operates at 3.33 GHZ and to operate at 4GHZ we need to add delay buffer of 50 ps in the clock distribution path A . ✓

✓ Which of the following options are correct about the canary and Razor Scheme: 1/1

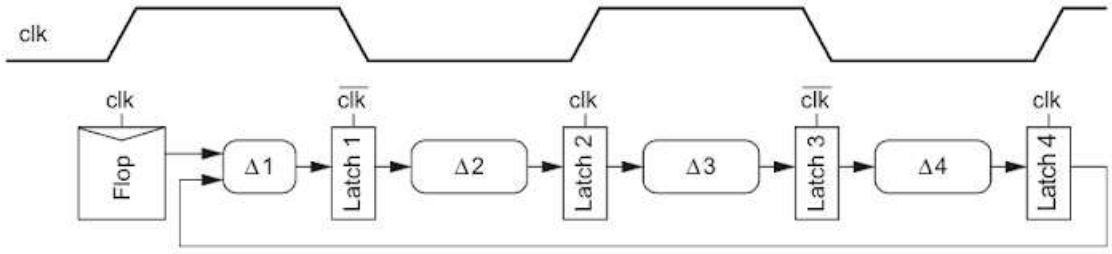
- [ ] The Canary Detects actual timing errors after they happen.
- [ ] . The Canary Always corrects errors by replaying instructions.
- [ ] The Razor Is designed to fail slightly earlier than the real path to give advance warning.
- [x] The Canary detects impending timing errors. ✓
- [ ] In safety-critical applications Razor is preferred because it detects actual timing errors and automatically corrects wrong outputs at the circuit level, so no unsafe output ever appears.
- [x] In safety-critical applications Canary is preferred because it is designed to fail before the real path, giving advance warning so the system can take preventive, deterministic action ✓

Feedback

Razor does detect actual timing errors, but it does not automatically correct them at the circuit level. Correction is performed by higher-level architectural mechanisms. For safety-critical systems, a predictive mechanism (canary) is usually preferred because it enables preventive action before an unsafe output can occur.
A canary is intentionally built to be slightly slower than the real critical path so it trips before the actual logic fails.

✓ For the path in the Figure, determine which latches borrow time and if any setup time violations occur for cycle times of 1000ps and 800 ps. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay and the Tsetup is 25ps. 2/2

a) Δ1 = 550 ps; Δ2 = 580 ps; Δ3 = 450 ps; Δ4 = 200 ps



- [x] 1000 ps: 50 ps borrowed through L1, 130 ps through L2, 80 ps through L3. ✓
- [x] 800 ps: 150 ps borrowed through L1, 330 ps borrowed through L2, L3 misses setup time. ✓
- [ ] 800 ps: no latches borrow time, no setup violations.
- [ ] 1000 ps: 80 ps borrowed through L1, 100 ps through L2, 50 ps through L3.

✓ Which statement best explains why fabs began using multi-patterning (e.g., LELE, SADP/SAQP, triple/quadruple patterning) instead of relying on single-exposure 193 nm immersion lithography for technology nodes below ~22 nm? 1/1

- [ ] Because 157 nm lithography completely replaced 193 nm at 22 nm, and multi-patterning was only used as a stopgap.
- [x] The Rayleigh-based resolution limit given by the Rayleigh's formula ($R=k1\lambda/NA$) hit the smallest value achievable with 193 nm optics, meaning further shrinking of printable feature sizes was no longer possible. ✓
- [ ] Because multi-patterning is always cheaper and simpler than single-exposure lithography, so fabs adopted it for cost reasons.
- [ ] None of the above

Roll No. *

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✓ Intentional clock skew (delaying or advancing clock arrival at some registers) is sometimes used to close timing. Why is clock skew *not* always a reliable tool for timing closure? 1/1

- [ ] Because any skew that helps setup slack on some paths will always improve hold slack on the same paths, making skew redundant.
- [ ] Because skew is deterministic and thus cannot compensate for process, voltage, temperature (PVT) variations, so it never helps timing closure.
- [x] Because an intentional skew that improves setup margin for certain register-to-register paths necessarily changes the relative capture/launch timing for other paths driven by the same clocks, potentially creating new hold or setup violations elsewhere; additionally, skew is limited by jitter, PVT uncertainty, and design-wide coupling, which makes it brittle and sometimes harmful. ✓
- [ ] Because clock skew only affects the clock network and has no effect on data path timing, so it cannot help timing closure.

Feedback

Clock skew can trade setup slack for hold slack — helping one set of paths while hurting others — because changing the arrival time at a register affects all paths that launch from or capture into that register. Real-world uncertainties (jitter, PVT, overlay) and the global impact of skew mean a skew that appears beneficial in one corner/path can break timing in another. Thus skew is a useful local tool when applied carefully, but it is not a universal or always-safe fix.

Name *

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✓ For the circuit shown below calculate the setup and hold slack for a clock period of 10ns. 1/1

Both the flops have setup and hold time of 2ns and 1 ns respectively?
Note: Slack is the extra time/margin available after meeting the setup or hold requirement.

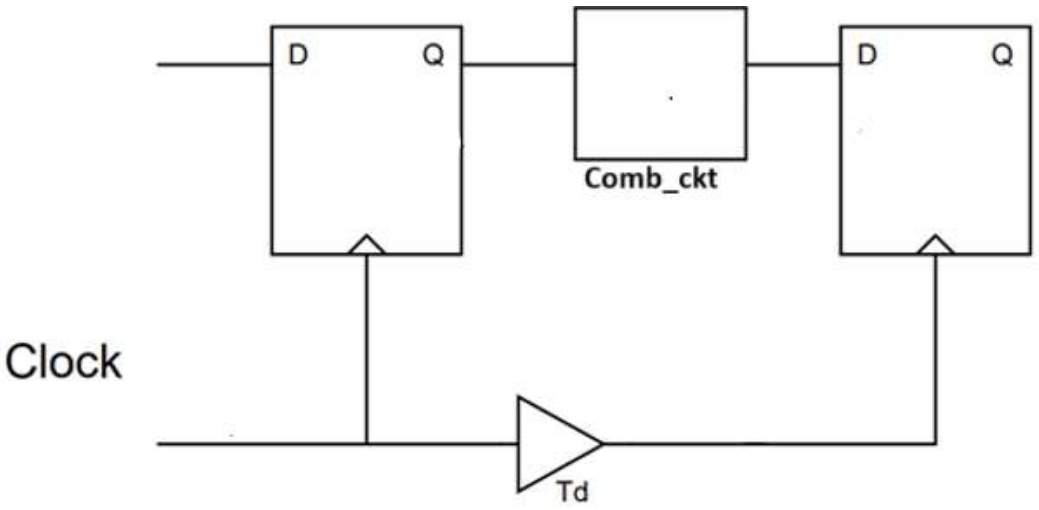
Clock jitter =20ps

Tpcq (propagation delay clock-to-Q) =2ns
Tccq (contamination delay clock-to-Q) = 1ns

Tpd_comb=4ns

Tcd_comb= 2ns

Td=1ns



- ○ setup slack is -1.98ns, the hold slack is 8.98ns
- ○ setup slack is 1.8ns, the hold slack is -0.8ns
- ◉ setup slack is 2.96ns, the hold slack is 0.96ns ✓
- ○ setup slack is -1.98ns, the hold slack is 0.98 ns

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