DVD Monsoon 2025: Review Quiz-3

Total points 5/10

Quiz Instruction

- The test will be live from **4:00 PM to 7:00 PM**.
- You must submit your response **before 7:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

Email *

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✓ Which of the following statement are correct? * 1/1

- [x] MOSFET shows higher capacitance at high frequency since the inversion charge is supplied by source and drain. ✓
- [x] MOSCAP shows lower capacitance at high frequency since the bulk cannot supply inversion charge fast enough. ✓
- [x] To achieve a high-capacity MOSCAP, it is typically designed to operate in the accumulation region, where the capacitance is at its maximum, independent of frequency. ✓
- [ ] MOSFET shows lower capacitance at high frequency since the bulk cannot supply inversion charge fast enough.
- [ ] As we increase the doping, depletion width increases which causes decrease in capacitance.
- [ ] To achieve a high-capacity MOSCAP, it is typically designed to operate in the inversion region, where the capacitance is at its maximum, independent of frequency.

Feedback

To achieve a high-capacity MOSCAP, it is typically designed to operate in the accumulation region, where the capacitance is at its maximum.
MOSCAP shows lower capacitance at high frequency since the bulk cannot supply inversion charge fast enough. Therefore, in inversion, the capacitor looks like oxide capacitance in series with depletion capacitance giving a much smaller capacitance.
MOSFET shows higher capacitance at high frequency since the inversion charge is supplied by highly doped source and drain.
As we increase the doping, depletion width decreases which causes increase in capacitance.

Roll Number *

2023024

✗ Which of the following statements is true regarding strong inversion of n-type MOSCAP? *0/1

- [ ] When the (Ei-Ef) at surface is equal to (Ei-Ef) at bulk, where Ef is fermi level and Ei is intrinsic fermi level, it is said to be in strong inversion.
- [ ] When the material is as n-type at surface as material is n-type in bulk, it is said to be in strong inversion.
- [x] When the density of holes in inversion layer is equal to density of electrons in bulk, it is said to be in strong inversion. ✓
- [x] When the material is as p-type at surface as material is n-type in bulk, it is said to be in strong inversion. ✓
- [x] When the (Ei-Ef) at surface is equal to (Ef-Ei) at bulk, where Ef is fermi level and Ei is intrinsic fermi level, it is said to be in strong inversion. ✓
- [ ] When the density of electrons in inversion layer is equal to density of holes in bulk, it is said to be in strong inversion.
- [ ] When the number of electrons in inversion layer is equal to number of holes in bulk, it is said to be in strong inversion.
- [x] When the number of holes in inversion layer is equal to number of electrons in bulk, it is said to be in strong inversion. ✗

Correct answer

- [x] When the material is as p-type at surface as material is n-type in bulk, it is said to be in strong inversion.
- [x] When the density of electrons in inversion layer is equal to density of holes in bulk, it is said to be in strong inversion.
- [x] When the density of holes in inversion layer is equal to density of electrons in bulk, it is said to be in strong inversion.
- [x] When the (Ei-Ef) at surface is equal to (Ef-Ei) at bulk, where Ef is fermi level and Ei is intrinsic fermi level, it is said to be in strong inversion.

Feedback

For n-type MOSCAP, strong Inversion is defined as:
When material is as p-type at the surface as material is n-type in the bulk.
Density (not number) of holes at the surface is equal to density of electrons in the bulk.
From mass action law, density of electrons at the surface is also equal to density of holes

in the bulk.
Also the difference of fermi levels (Ei-Ef) at the surface is equal to (Ef-Ei) in the bulk, where Ef is fermi level and Ei is intrinsic fermi level.

✗ Which of the following statements are incorrect regarding Velocity Saturation? *0/1

- [x] In velocity saturation, as electric field increases mobility decreases. ✗
- [x] Drain current is more for short channel device as compared to long channel device for same drain-source voltage. ✓
- [x] Velocity saturation happens earlier in long channel device as compared to short channel device. ✓
- [ ] Velocity saturation occurs due to collision of carriers with the lattice at high electric field.

Correct answer

- [x] Velocity saturation happens earlier in long channel device as compared to short channel device.
- [x] Drain current is more for short channel device as compared to long channel device for same drain-source voltage.

Feedback

Velocity saturation happens earlier in short channel device because electric field is high due to short channel length.

Drain current is less for short channel device because velocity saturation occurs earlier in short channel devices which limits the further increase in current.

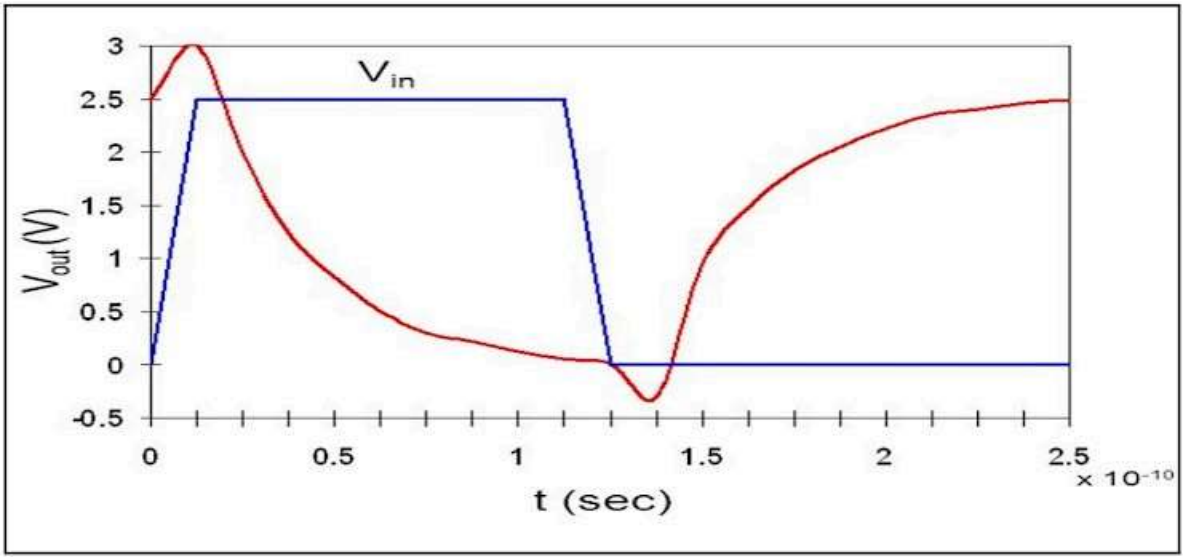
✓ Which of the following statements are false regarding use of MOS devices in subthreshold region? *1/1

- [ ] They have less power consumption as voltage at which they are operated is low.
- [ ] They provide high delays due to low current because of low inversion charge density.
- [x] They provide low gain due to low inversion charge density. ✓
- [ ] They are used in applications such as sensor dust because they have low power budget and don't require high speed.
- [ ] They provide low noise immunity due to high change in inversion charge density.

Feedback

MOS devices which are operated in subthreshold region consume less power because they are operated at low voltages. They have high delays due to low current which is due to low inversion charge density. They also have high gain and low noise immunity due to high change in inversion charge density. Applications like Sensor dust have limited power budget and don't require high speed, so MOS devices can be used in subthreshold region.

✗ What were the reasons for overshoots and undershoots of output signal of inverter when you performed eldo simulations in the Assignment 1, as shown in the image. *0/1



- [x] Due to capacitive coupling of gate-source capacitances of inverter transistors. ✗
- [ ] These are just simulation and tool dependent glitches and don't happen on actual hardware.
- [ ] Undershoots are due to Vt drop across NMOS transistor in CMOS inverter.
- [x] Due to redistribution of charge accumulated in inversion layer between source and drain regions leading to temporary voltage spikes. ✓
- [x] Due to capacitive coupling of gate-drain capacitances of inverter transistors. ✓

Correct answer

- [x] Due to capacitive coupling of gate-drain capacitances of inverter transistors.
- [x] Due to redistribution of charge accumulated in inversion layer between source and drain regions leading to temporary voltage spikes.

Feedback

Overshoots in the output signal of an inverter's transient response occur due to gate-drain capacitances of the inverter transistors, which couple the steep voltage step at the input node directly to the output before the transistors can even start to react to the changes at input.

Overshoots in an inverter's output signal during transient response occur due to the

redistribution of charge when the input voltage is abruptly switched off. The transistors have an inversion layer in the "on" state. When the input voltage rapidly transitions to "off," the charge in the inversion layer must be redistributed between the source and drain regions. This redistribution process can lead to temporary voltage spikes or overshoots in the output signal as the charge dissipates.

✗ Pranav used an additional M2 metal layer while creating his standard cell layout. When he presented it to Anuj sir, Anuj sir advised him to restrict the layout to M1 and expressed concerns about how using M2 could affect the overall chip design. What potential concerns do you think he was referring to? (Assume number of metal layers for routing are fixed) *0/1

- [ ] Additional metal layer leads to at least 2 additional masks which leads to increase in cost.
- [ ] It increases Time To Market (TTM) of chip.
- [ ] It causes increase in delays as more metal layers means more delays.
- [ ] Using an additional metal layer requires at least two extra masks, which increases the carbon footprint and makes it a less sustainable choice.
- [x] It leads to increase in die area. ✗

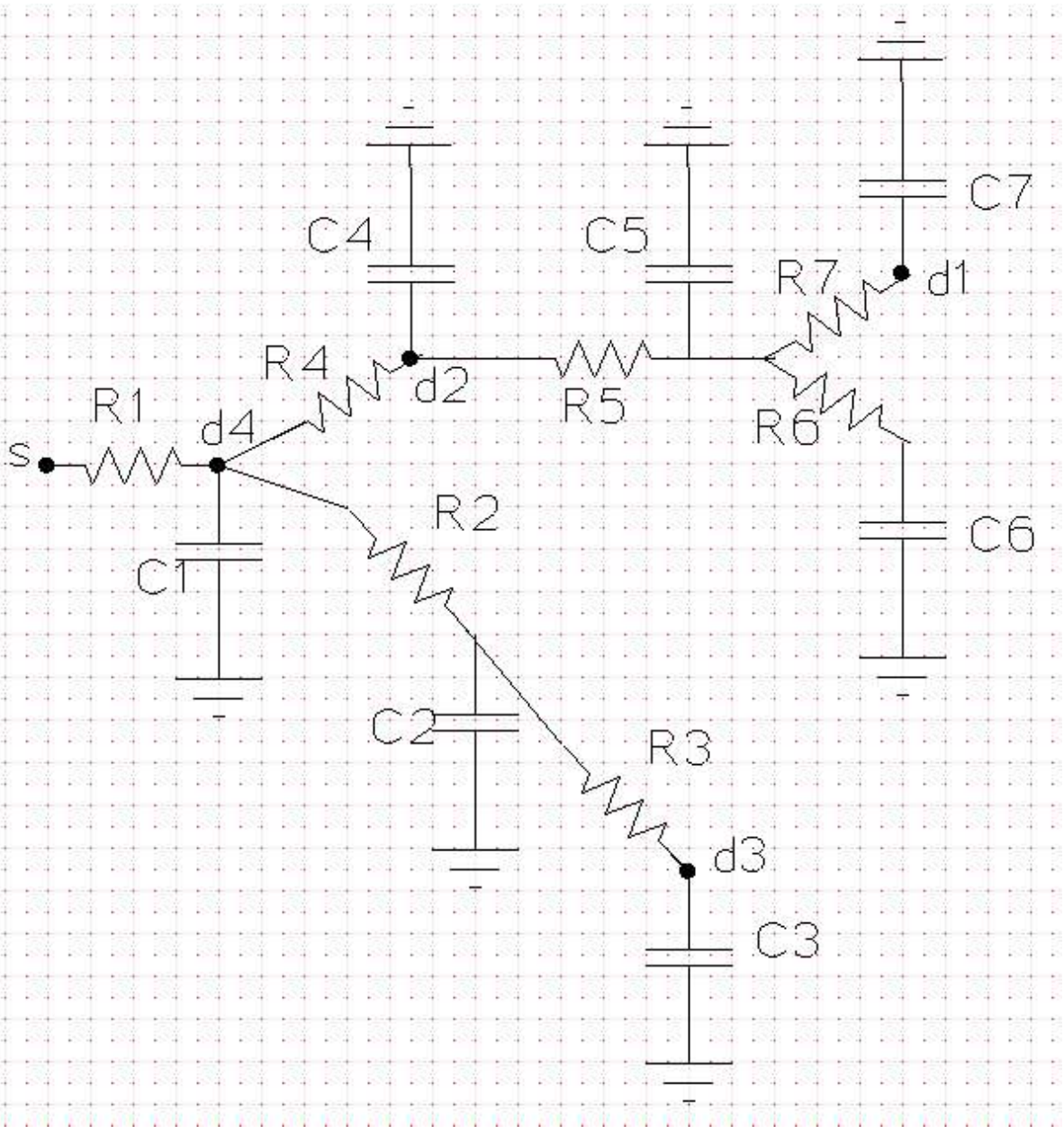
Correct answer

- [x] Additional metal layer leads to at least 2 additional masks which leads to increase in cost.
- [x] It increases Time To Market (TTM) of chip.
- [x] Using an additional metal layer requires at least two extra masks, which increases the carbon footprint and makes it a less sustainable choice.

Feedback

Additional metal layer leads at least 2 additional masks - 1 for metal layer and 1 for via. This causes increase in cost and time to market as more time is being spent during fabrication. Furthermore additional masks result in increase of carbon footprint, particularly embodied carbon footprint (eCFP), which makes it a less sustainable choice.

✓ For the figure given below, calculate the Elmore delay at nodes d1, d2, d3 and d4. Consider all resistances of value 1mΩ, all capacitances of value 1nF and s as source node. *2/2



- [x] d1 = 15ps ✓
- [ ] d1 = 10ps
- [x] d3 = 10ps ✓
- [ ] d2 = 3ps
- [ ] d4 = 1ps

- [ ] d3 = 6ps
- [x] d2 = 11ps ✓
- [x] d4 = 7ps ✓

Feedback

Solution

✗ Which of the following statements are correct regarding MOS devices? * 0/1

- [ ] Polysilicon gates provide smooth interface between gate and SiO2 reducing surface states and providing better control of gate.
- [x] High K dielectric are used instead of SiO2 as they help increase gate capacitance. ✓
- [x] Low K dielectric are used in intermetal dielectric to reduce parasitic capacitance and thus reduce RC delay, crosstalk and power consumption. ✓
- [x] At advanced technology nodes, since High K dielectrics are replacing SiO2, we are using metal gates over polysilicon gates as they give wide range of work functions and provide smoother gate-oxide interface. ✓

Correct answer

- [x] Polysilicon gates provide smooth interface between gate and SiO2 reducing surface states and providing better control of gate.
- [x] High K dielectric are used instead of SiO2 as they help increase gate capacitance.
- [x] Low K dielectric are used in intermetal dielectric to reduce parasitic capacitance and thus reduce RC delay, crosstalk and power consumption.
- [x] At advanced technology nodes, since High K dielectrics are replacing SiO2, we are using metal gates over polysilicon gates as they give wide range of work functions and provide smoother gate-oxide interface.

Feedback

All options are correct.

Name *

Abhinav Maurya

✓ Which of the following statements regarding standard cell format are correct? *1/1

- [ ] We leave half DRC spacing while designing layouts in standard cell format because foundries allow DRC violations in standard cell as they are of fixed height.
- [ ] If a standard cell is limited to Metal1, then the height of the cell is measured using pitch of Metal1 layer.
- [x] We fix the height of standard cells because it helps in regularity and ease of placement. ✓
- [x] If a standard cell is limited to Metal1, then the height of the cell is measured using pitch of Metal2 layer. ✓
- [x] If the width of devices can not be accomdated within the height of standard cell, we divide our transistor into multiple fingers. ✓

Feedback

In standard cell topology, one cell is abutted with another cell. Now if one leaves ½ the minimum DRC requirement across cell sharing, then after abutment, 1 full DRC is met. This will enable abutting cells at minimum possible spacings saving the area and time/effort to make DRC clean layouts.
If a standard cell is limited to Metal1, then the height of the cell is measured using pitch of Metal2 layer as it will be used to route above the standard cells.
We fix the height of standard cells because it helps in regularity and ease of placement. It ensures optimal use of area.
If the width of transistors is very large such that they can't fit into the height of the standard cell (within the tracks allotted), we divide our transistor into multiple fingers. This ensures our standard cells are of same height without compromising on device size.