Tab 1

Digital VLSI Design (ECE-314/514)

Mid-Sem Exam Set-A

22nd September 2025 [Time: 3:00-4:00 PM]

Maximum Marks: 25 Marks | Duration: 60 minutes

Name _____ | Roll No. _____

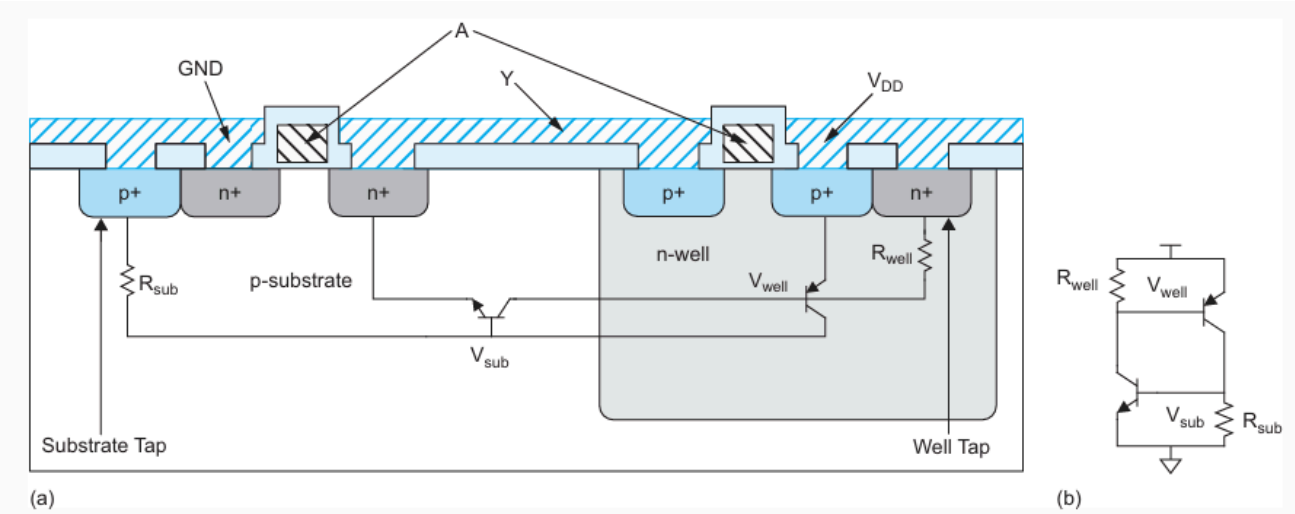
Instructions

1. This is a closed-book exam
2. Use of calculators is permitted. Use of mobile phones is strictly not allowed.
3. There are multiple sets of question papers. Write your set on your answer sheet.
3. There are a total of 7 questions in the paper and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following questions. **(CO1, 8 marks)**

a) What is the phenomenon in which CMOS chips tend to develop a low resistance path between VDD and GND, causing catastrophic meltdown? Describe briefly this phenomenon - how and when this phenomenon is triggered? How can this be prevented? **(2 marks)**

Latch-up is a condition where multiple p-n junctions of the S/D regions of MOSFETs form a back-to-back pnp-npn BJT latch.



These create a positive feedback loop when Rwell and Rsub are large, causing the BJTs to turn ON. This results in a sudden current surge. Due to positive feedback, this current keeps growing and can result in chip meltdown (burnout).

It can be prevented by using a sufficient number of taps/strap connections, which results in a small value of Rsub and Rwell, preventing these parasitic BJTs from turning ON.

b) Why is Tungsten (W) preferred over Copper (Cu) for making contacts in CMOS technology? **(1 mark)**

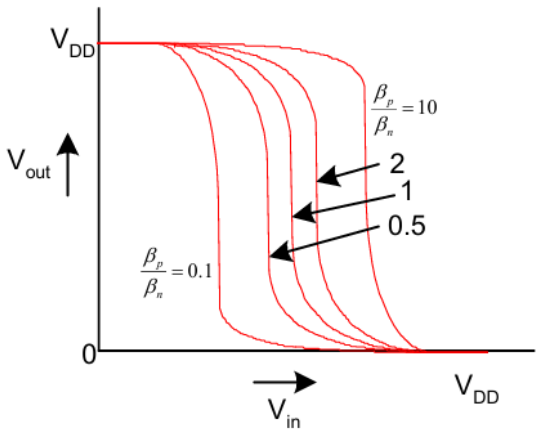
Copper diffuses rapidly into silicon and silicon dioxide and creates intermediate energy states in the band gap of silicon. This degrades the semiconductor behaviour of silicon, and transistor action is severely impacted.

Tungsten has a much higher melting point and is ductile. It doesn't interact with Silicon substrate. Thus it is a good choice for contacts.

c) Explain the effect of β-ratio on noise margins and propagation delays in a CMOS inverter**.** **(2 marks)**

When we increase the beta ratio, PMOS gets stronger, the VTC curve as shown in the image shifts towards right, so the ability to detect low logic levels (VIL) increases, thus low noise margin NML (VIL-VOL) improves and high noise margin NMH (VOH-VIH) degrades as VIH increases.

Rise propagation delay Tplh decreases as stronger PMOS is able to charge the output load faster and fall propagation delay Tphl increases as it takes more time for weaker NMOS to discharge the same output load.



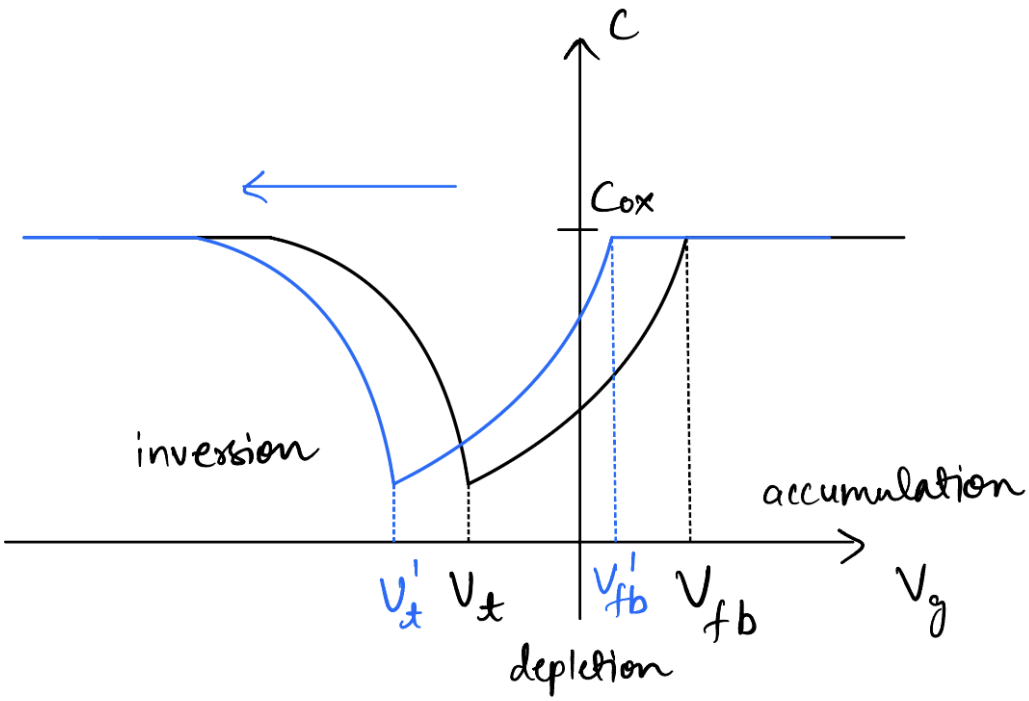
OR

When we decrease the beta ratio, NMOS gets stronger, the VTC curve as shown in the image shifts towards left, so the ability to detect high logic levels increases (VIH reduces), thus high noise margin NMH (VOH-VIH) improves and low noise margin NML (VIL-VOL) degrades as VIL reduces.

Fall propagation delay Tphl decreases as stronger NMOS is able to discharge the output load faster and rise propagation delay Tplh increases as it takes more time for weaker PMOS to charge the same output load.

d) Draw the C–V characteristics plot of a PMOS transistor with proper labelling. If positive charges are implanted in the oxide layer, redraw the curve showing in which direction it shifts? **(2 marks)**

If positive charges are implanted in the oxide layer, we need to apply more negative Vg to create the inversion layer. This can be seen as threshold voltage becomes more negative and the C-V curve shifts towards left.



e) Explain the effect of change in temperature on subthreshold current and ON current. **(1 mark)**

In the subthreshold region of operation, there are few free carriers. As the temperature increases, carriers are generated due to thermal generation. Due to the availability of more charge carriers, the subthreshold current increases.

On the other hand, ON current is constituted by free carriers present in the conduction band. Due to higher voltage at the gate, there are a large number of carriers in the conduction band. As we increase the temperature, the increase in the number of carriers due to thermal generation is only marginal. However, there are more lattice vibrations and therefore the number of collisions between the carriers increases. This results in reduced mobility of the carriers, resulting in a decrease in the ON current.

Q2) Complete the table below with the worst-case PVT conditions for different FOMs. **(CO1, 1.5 marks)**

Figure of Merit (FoM)	Process	Voltage	Temperature
Power	FF	High	Low
Leakage	FF	High	High
Contamination Delay	FF	High	Low

Q3) Nikhil is a design engineer at company X. While performing the verification process of a digital circuit at low voltage and high temperature, the delay specifications are met. He expects the specification to be met at low voltage and low temperature also, but it fails. Explain the reason behind this? **(CO3, 1 mark)**

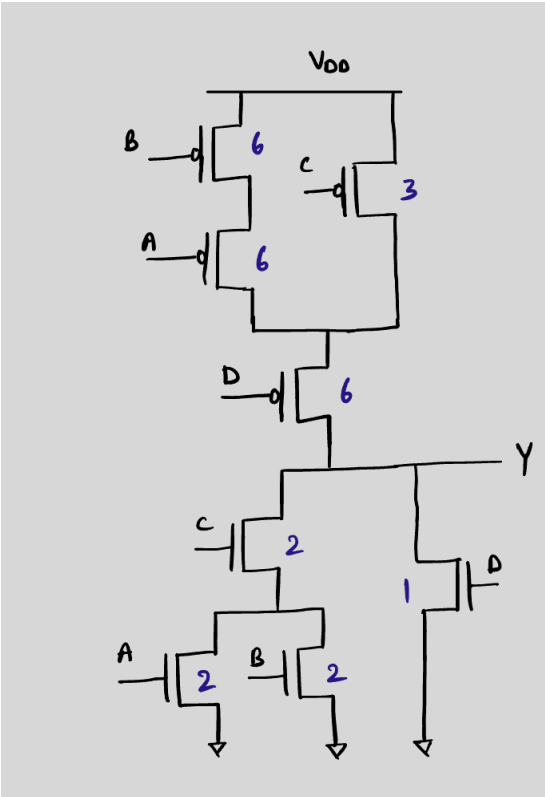
At high temperatures, there are more lattice vibrations. This results in an increased number of collisions between the charge carriers and the lattice. This results in reduced mobility at high temperatures.

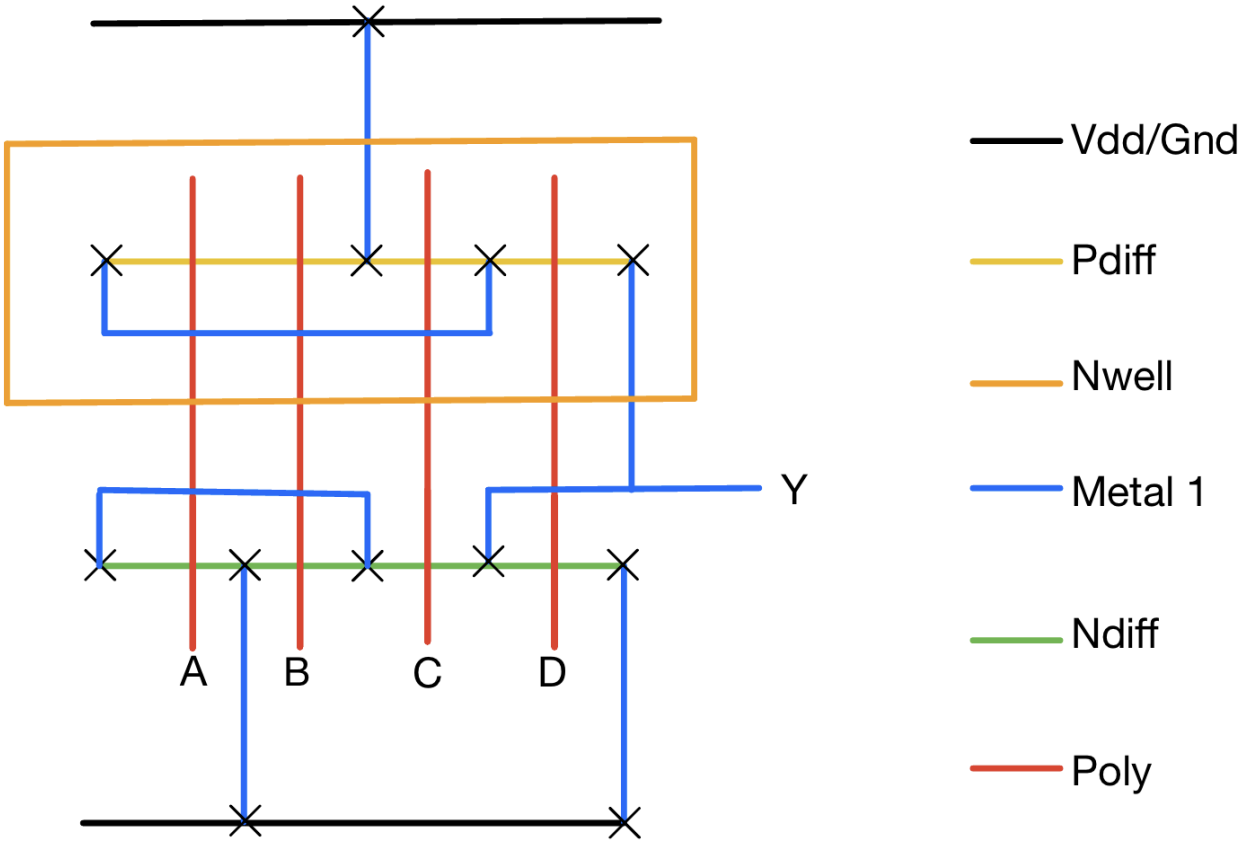
However, at low voltages, high temperature also results in more thermal generation. At low voltages, free carriers are few in number and therefore thermal generation induced carriers result in a significant increase in ON current (sufficient enough to offset the impact of reduced mobility due to lattice vibrations).

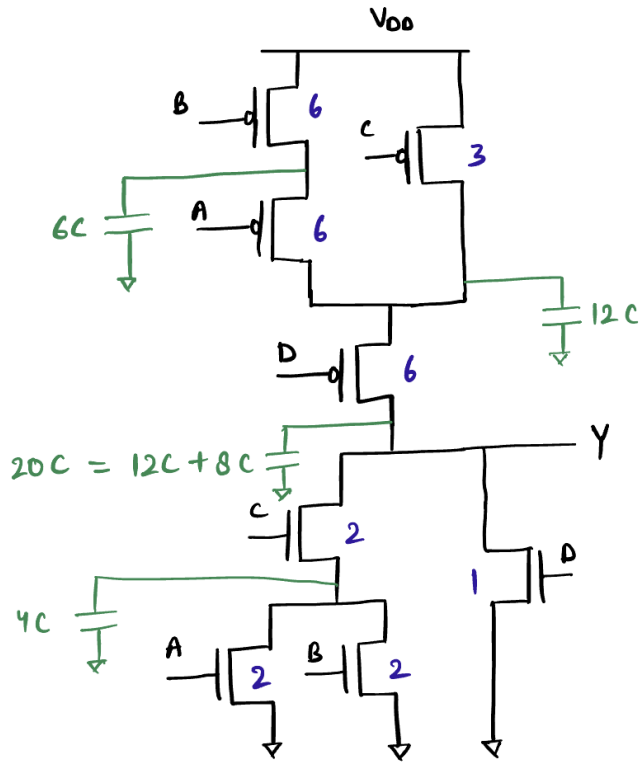
Therefore, while at high voltages, Nikhil's assumption would have been correct, it is not valid at low voltages. This phenomenon is called temperature inversion.

Q4) Consider the Boolean expression Y = ((A+B).C+D)'. Implement its schematic in static CMOS design style and size the transistors with respect to unit inverter **(1 mark)** and draw the stick diagram **(2 marks)** considering as much sharing of S/D as possible and do the following: **(9 marks)**

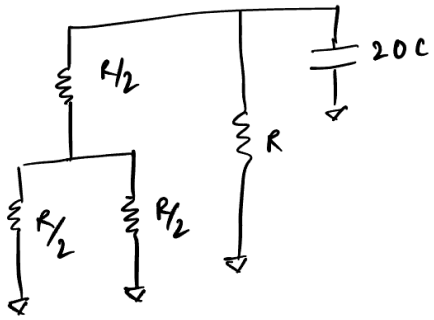
- **a)** Indicate the capacitances at each node in the schematic while also considering an additional load of 12C at the output. **(CO1, 1 mark)**
- **b)** Calculate the Contamination Rise/Fall Delay using Elmore Delay. **(CO2, 2 marks)**
- **c)** Calculate the Propagation Rise/Fall Delay using Elmore Delay. **(CO3, 2 marks)**
- **d)** Calculate the logical effort of each input. **(CO3, 1 mark)**




Y
A
B
C
D
Vdd/Gnd
Pdiff
Nwell
Metal 1
Ndiff
Poly



CD fall :

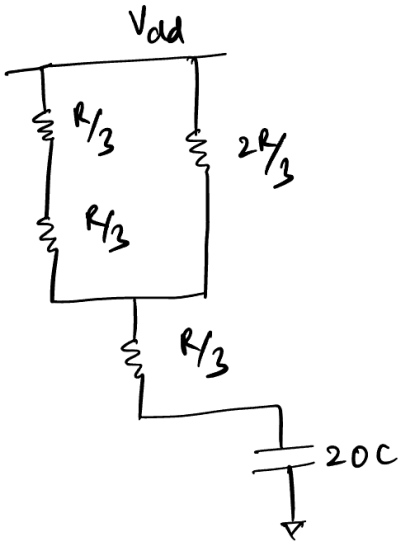


$t_{cdf} = 20\,C \cdot R_{eq}$

$t_{cdf} = 20 \cdot \frac{3R}{7}$

$t_{cdf} = \frac{60RC}{7}$

CD Rise

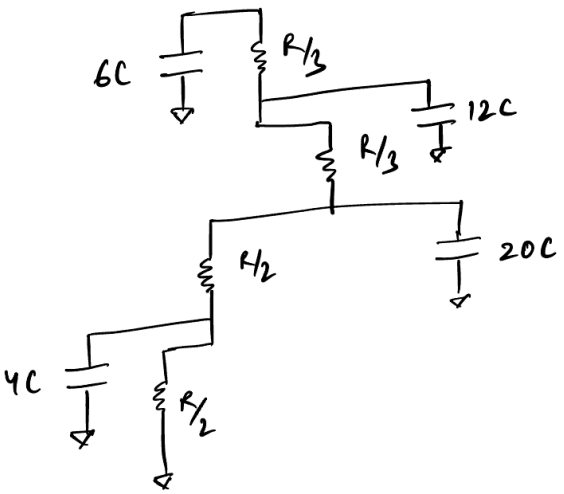


$t_{cdr} = 20\,C \cdot R_{eq}$

$t_{cdr} = 20\,C \cdot \frac{2R}{3}$

$t_{cdr} = \frac{40}{3} RC$.

PD fall



$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 20C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 12C + \left(\frac{R}{2}+\frac{R}{2}\right)6C$$

$$= 2RC + 20RC + 12RC + 6RC$$

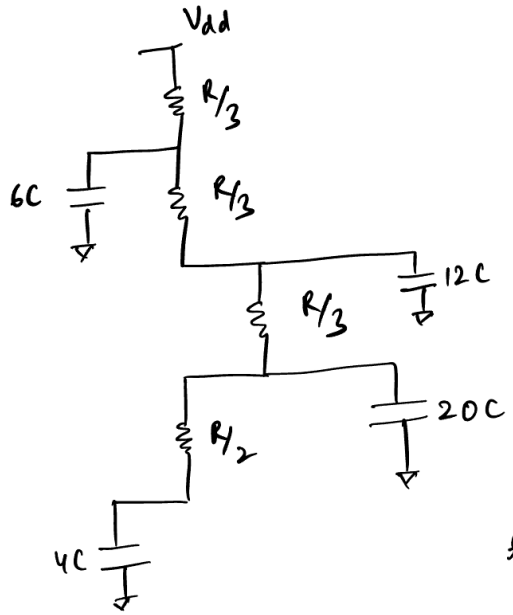
$$t_{pdf} = 40RC$$

Considering only 50 %.

$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 20C$$

$$= 22RC$$

PD Rise



$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 20C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 4C$$

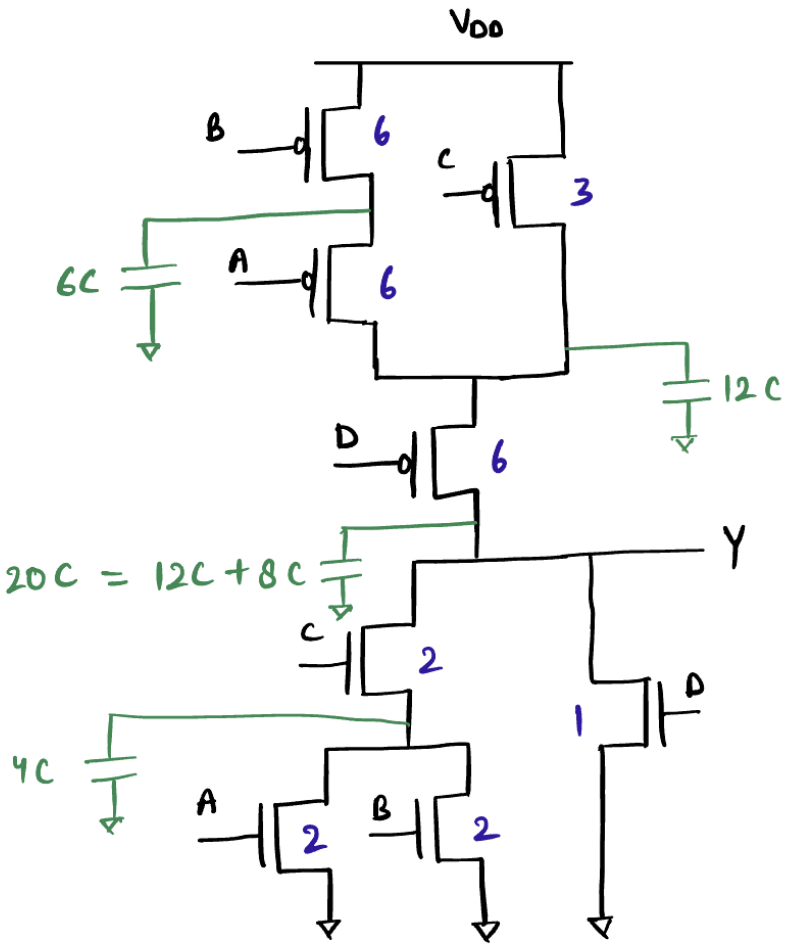
$$t_{pdr} = 2RC + 8RC + 20RC + 4RC$$

$$= 34RC.$$

Considering only 50 %.

$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 20C$$

$$t_{pdr} = 30RC$$



Logical effort :-

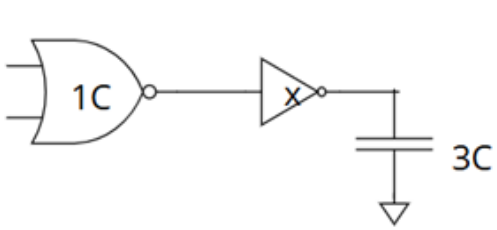
$g_A = \frac{8C}{3C} = \frac{8}{3}$

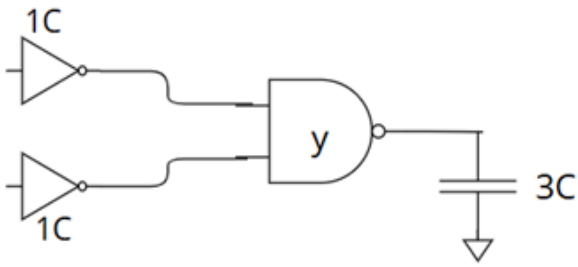
$g_B = \frac{8C}{3C} = \frac{8}{3}$

$g_C = \frac{5C}{3C} = \frac{5}{3}$

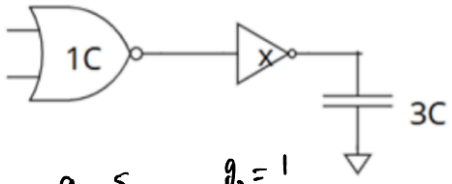
$g_D = \frac{7C}{3C} = \frac{7}{3}$

Q5) Consider the two alternative circuit implementations of a 2-input OR gate as shown in the figure below. Provide an intuitive argument to determine which design is expected to demonstrate slow performance. **(0.5 marks)** Support your reasoning with a quantitative analysis by calculating the path effort, delay **(1 mark)**, and the input capacitances x and y required to achieve this delay **(1 mark)**. Also size the corresponding transistors accordingly **(1 mark)**. **(CO2, 3.5 marks)**





Path logical effort for 1st circuit, G1 = (5/3)*1 = 5/3 and for 2nd circuit, G2 = 1*(4/3) = 4/3
Since G1>G2, intuitively it seems design 1 is expected to demonstrate slow performance.



$g_1 = \frac{5}{3}$ $\quad g_2 = 1$

$G_1 = g_1 g_2 = \frac{5}{3}$

$B = 1$

$H = \frac{3C}{1C} = 3$

$F = G_1 B H$

$F = 5$

$\hat{f} = (F)^{1/N} = (5)^{1/2}$

$\hat{f} = 2.23$

$D_1 = N\hat{f} + P$

$D_1 = 2 \times 2.23 + (2+1)$

$D_1 = 7.46$

$\hat{f} = g_2 h_2$

$2.23 = 1 \cdot \frac{3C}{x}$

$x = 1.345C$

Let inverter be upsized by k_1

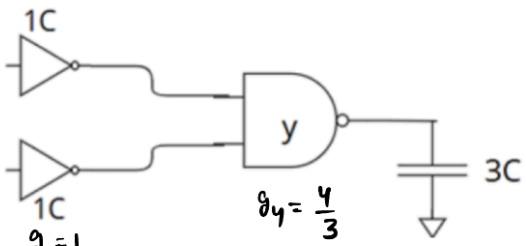
$3 \cdot k_1 C = 1.345C$

$k_1 = 0.45$

for pmos $\Rightarrow 2 \times 0.45 = 0.9$

for nmos $\Rightarrow 1 \times 0.45 = 0.45$

$g_5 = 1$



$g_3 = 1$ $\quad g_4 = \frac{4}{3}$

$G_2 = g_3 g_4 = \frac{4}{3}$

$B = 1$

$H = \frac{3C}{1C} = 3$

$F = G_2 B H$

$F = 4$

$\hat{f} = (F)^{1/N} = (4)^{1/2}$

$\hat{f} = 2$

$D_2 = N\hat{f} + P$

$D_2 = 2 \times 2 + (1+2)$

$D_2 = 7$

As we can see $D_1 > D_2$

$\hat{f} = g_4 h_4$

$2 = \frac{4}{3} \cdot \frac{3C}{y}$

$y = 2C$

Let NAND gate be upsized by k_2

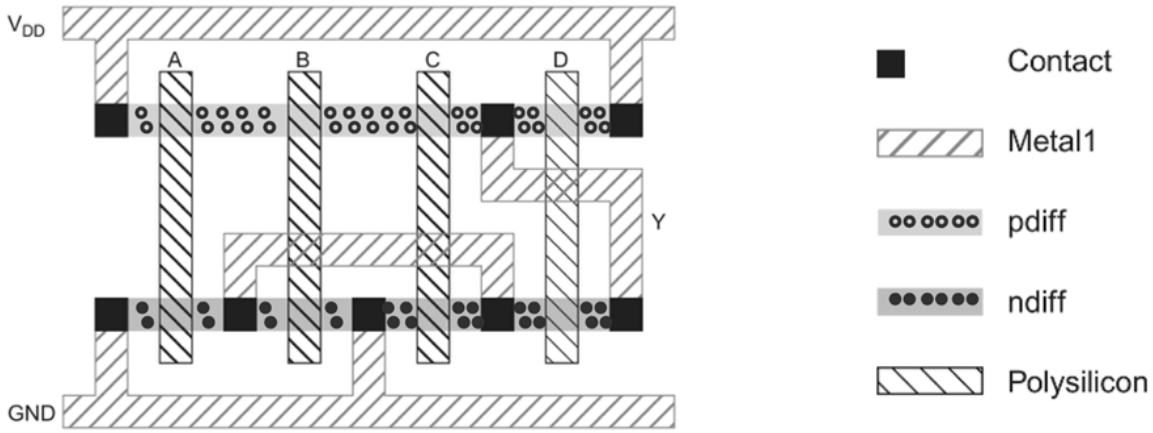
$4 \cdot k_2 C = 2C$

$k_2 = 0.5$

for pmos $\Rightarrow 2 \times 0.5 = 1$

for nmos $\Rightarrow 2 \times 0.5 = 1$

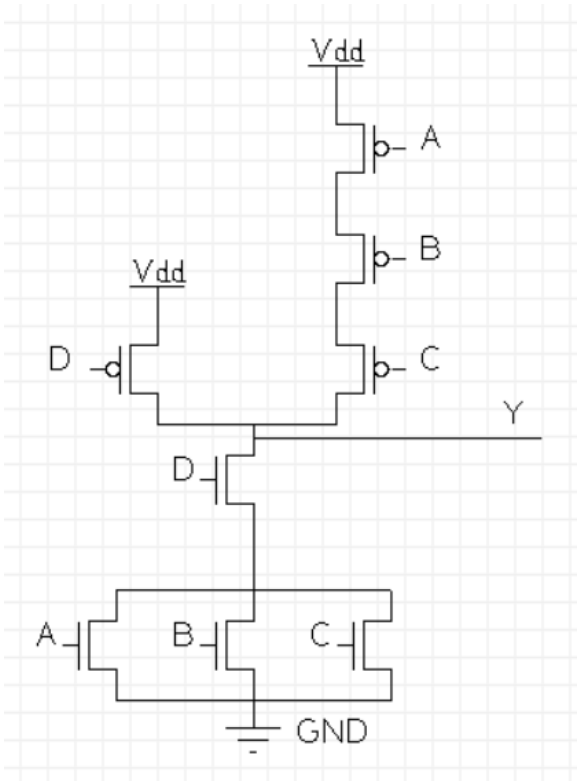
Q6) For the given layout **(CO5, 2 marks)**



a) Draw the transistor level schematic. **(1 mark)**

b) Derive the boolean expression of output Y **(1 mark)**

a)



b) Y = ((A+B+C).D)'

Q7) [Bonus] A product is designed in 90nm technology and takes up 100mm2 area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs.10. The designers use a denser version of libraries to reduce the area to 80mm2. Assuming the same Defectivity, D0, what is the new expected Yield? The product is still sold for Rs.100/-. How much profit does the company make now per product sold? **(CO1, 2 marks)**

Assume that 100 dies were manufactured per wafer.
At 56% yield, every wafer earns Rs.5600/-
At this sale price, profit is Rs.560/- (Rs. 10/- per die sold).

Yield is inversely dependent on Area.
When the Area reduces to 80mm2. Yield changes to 56/(0.8) = 70%
Total dies made now = (100/80)*100=125
Therefore, no of non-defective dies are= 125*0.7=87.5, which is equivalent to 87.
So, now 31 extra dies can be sold at Rs.100/-
Extra profit = Rs. 3100/
Total profit = Rs. 3660/ Profit per die = 3660 / 87 = Rs. 42 (approx)

So, with a 20% reduction in area, total profit jumped to almost 7 times, and profit per sold die increased to about 4 times. Therefore, the area is considered as one of the most important Figures of Merit in the VLSI industry.

Tab 2

Digital VLSI Design (ECE-314/514)

Mid-Sem Exam Set-B

22nd September 2025 [Time: 3:00-4:00 PM]

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Q1) Answer the following questions. **(CO1, 8 marks)**

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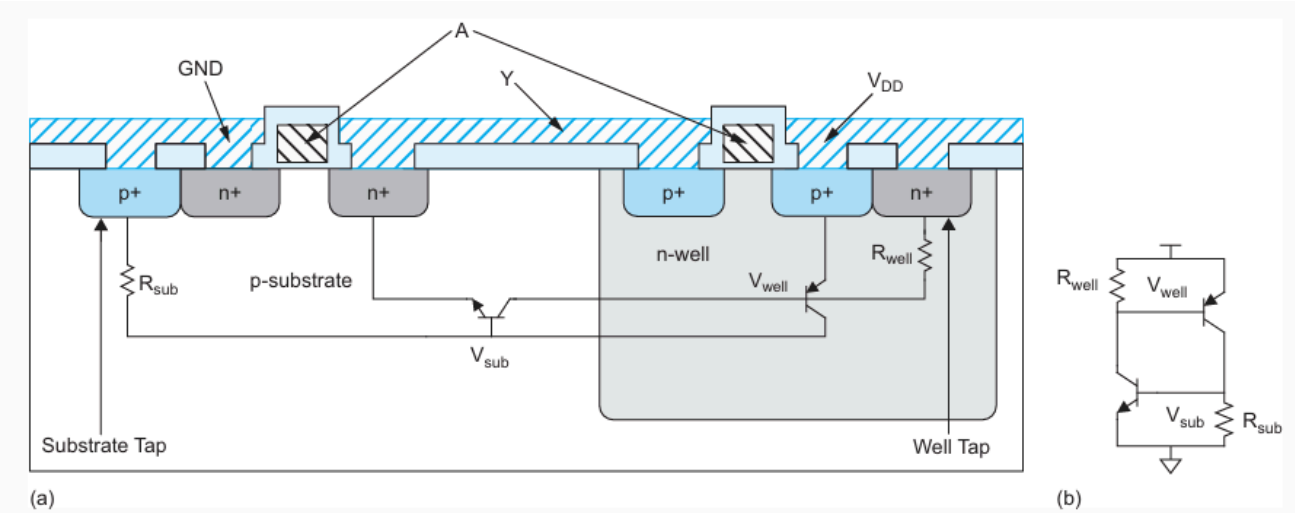

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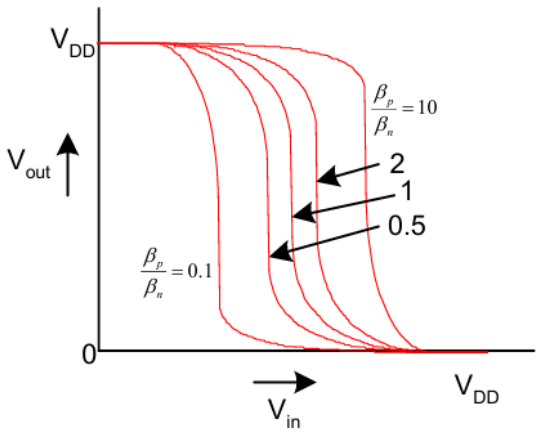

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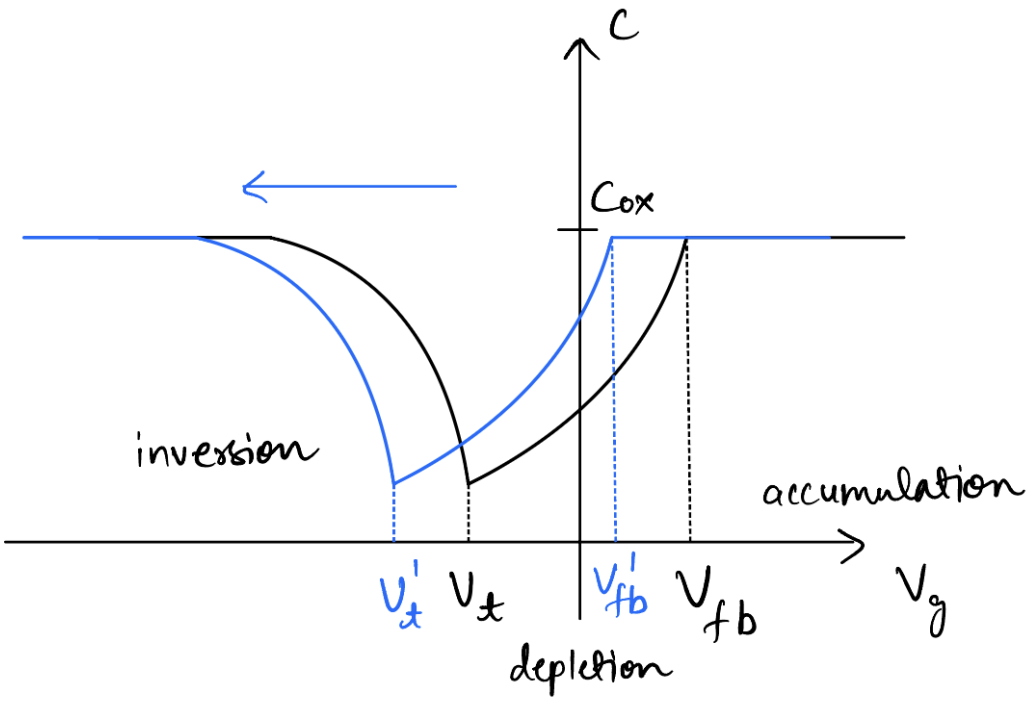

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Power	FF	High	Low

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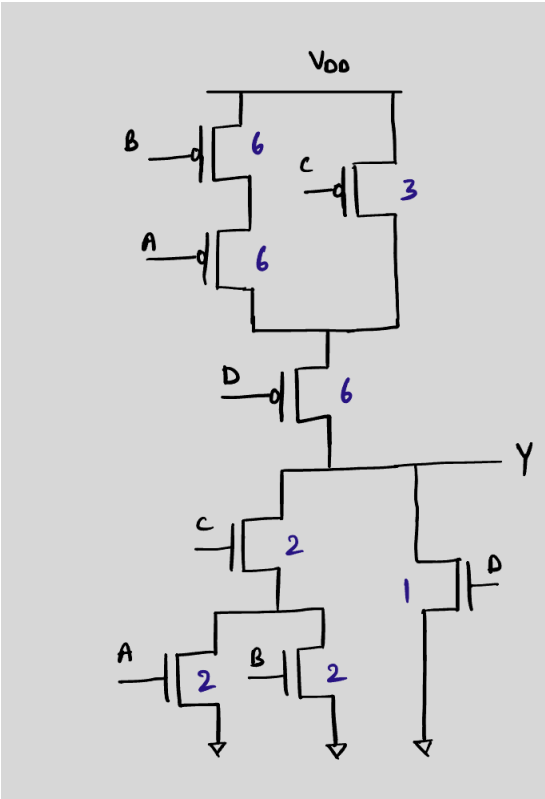
At high temperatures, there are more lattice vibrations. This results in an increased number of collisions between the charge carriers and the lattice. This results in reduced mobility at high temperatures.

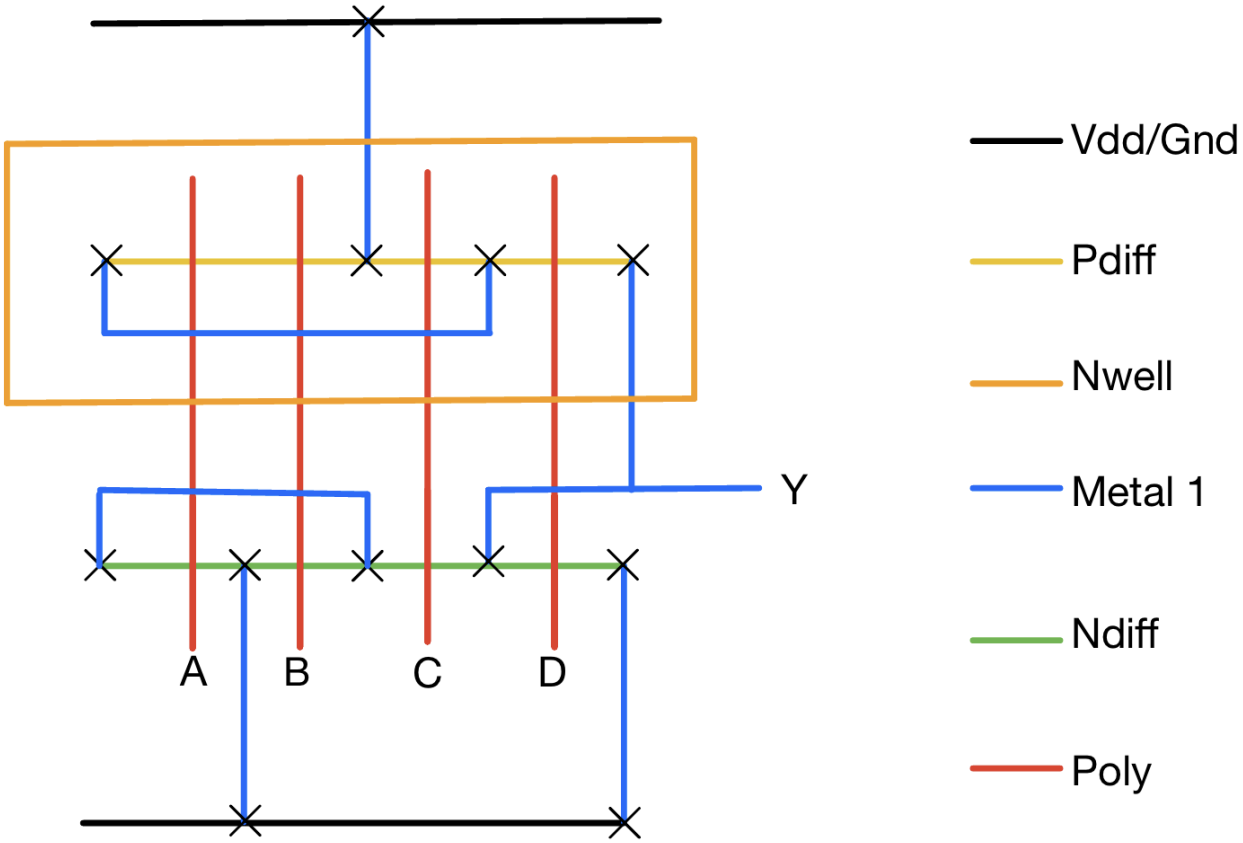
However, at low voltages, high temperature also results in more thermal generation. At low voltages, free carriers are few in number and therefore thermal generation induced carriers result in a significant increase in ON current (sufficient enough to offset the impact of reduced mobility due to lattice vibrations).

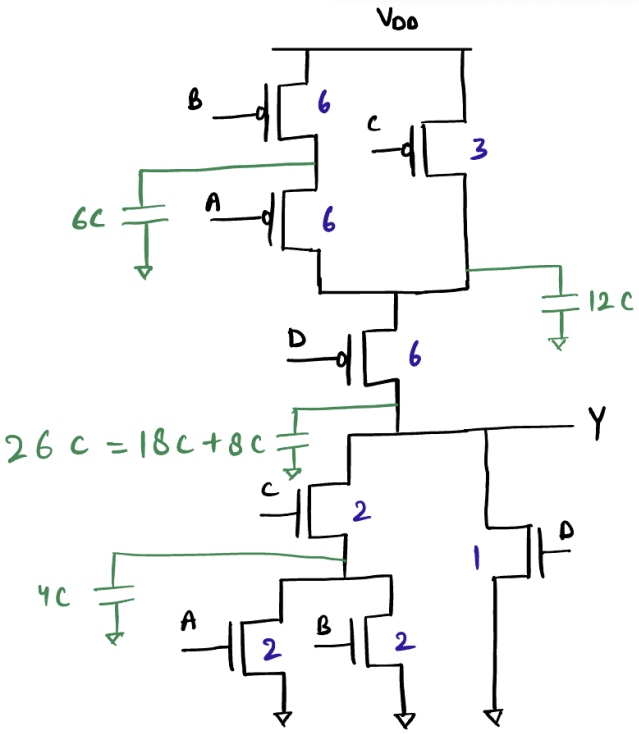
Therefore, while at high voltages, Nikhil's assumption would have been correct, it is not valid at low voltages. This phenomenon is called temperature inversion.

Q4) Consider the Boolean expression Y = ((A+B).C+D)'. Implement its schematic in static CMOS design style and size the transistors with respect to unit inverter **(1 mark)** and draw the stick diagram **(2 marks)** considering as much sharing of S/D as possible and do the following: **(9 marks)**

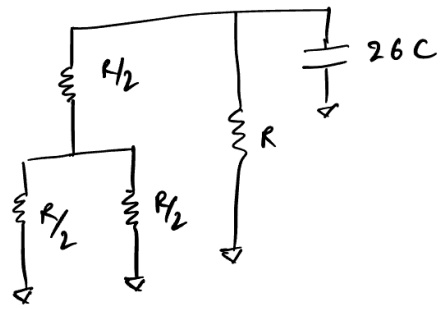
- **a)** Indicate the capacitances at each node in the schematic while also considering an additional load of 18C at the output. **(CO1, 1 mark)**
- **b)** Calculate the Contamination Rise/Fall Delay using Elmore Delay. **(CO2, 2 marks)**
- **c)** Calculate the Propagation Rise/Fall Delay using Elmore Delay. **(CO3, 2 marks)**
- **d)** Calculate the logical effort of each input. **(CO3, 1 mark)**




Y
A
B
C
D
Vdd/Gnd
Pdiff
Nwell
Metal 1
Ndiff
Poly



CD fall :

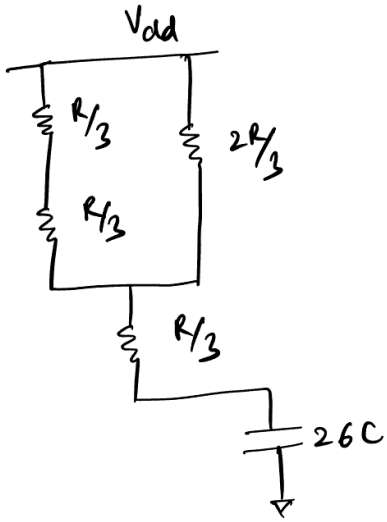


$t_{cdf} = 26\ C . R_{eq}$

$t_{cdf} = 26C . \frac{3R}{7}$

$t_{cdf} = \frac{78}{7} RC$

CD Rise

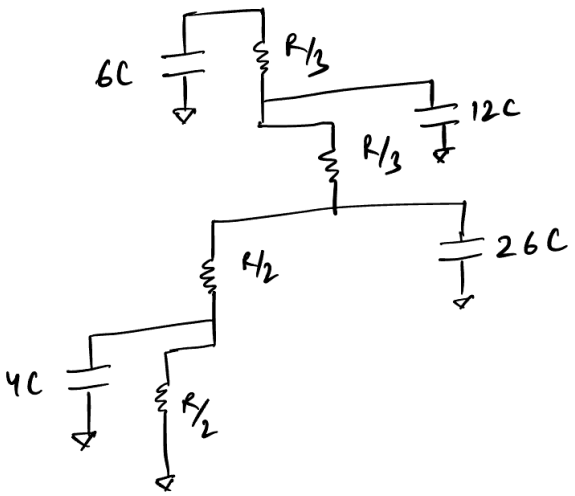


$t_{cdr} = 26\ C . R_{eq}$

$t_{cdr} = 26\ C . \frac{2R}{3}$

$t_{cdr} = \frac{52}{3} RC$

PD fall



$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 26C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 12C + \left(\frac{R}{2}+\frac{R}{2}\right)6C$$

$$= 2RC + 26RC + 12RC + 6RC$$

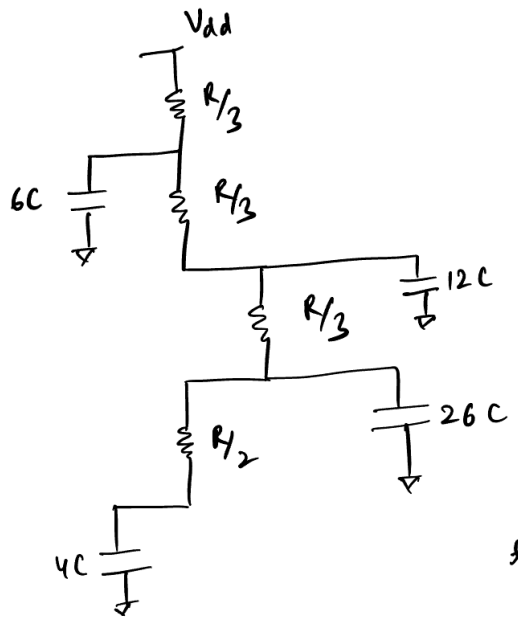
$$t_{pdf} = 46\,RC$$

Considering only 50 %.

$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 26C$$

$$= 28\,RC$$

PD Rise



$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 26C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 4C$$

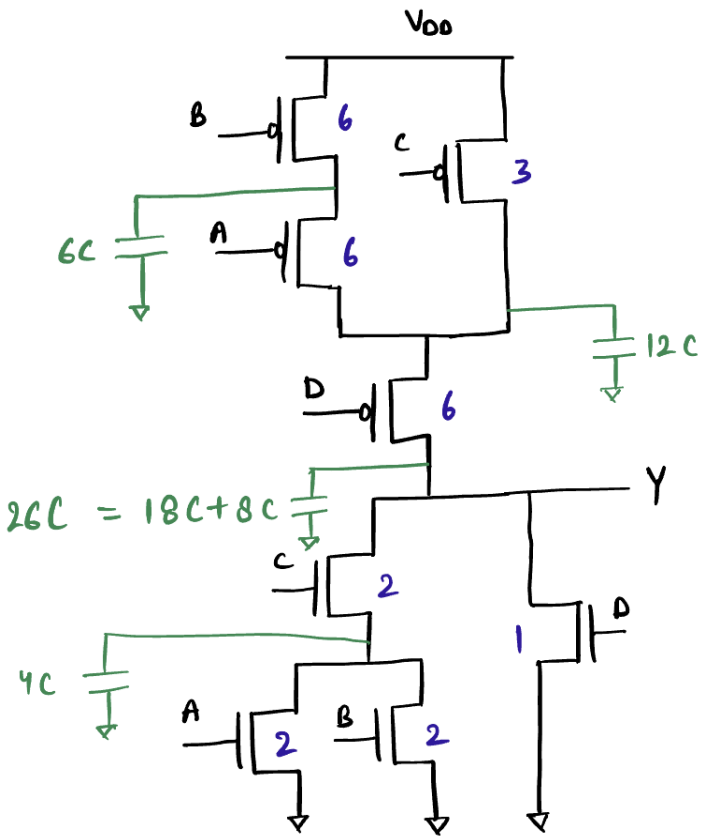
$$t_{pdr} = 2RC + 8RC + 26RC + 4RC$$

$$= 40\,RC$$

Considering only 50 %.

$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 26C$$

$$t_{pdr} = 36\,RC$$



Logical effort :-

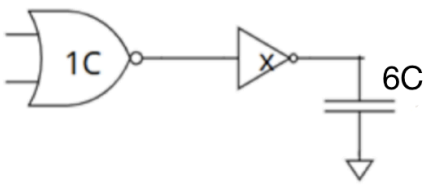
$g_A = \frac{8C}{3C} = \frac{8}{3}$

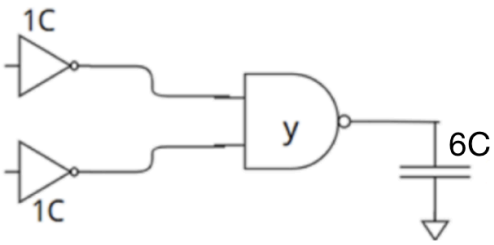
$g_B = \frac{8C}{3C} = \frac{8}{3}$

$g_C = \frac{5C}{3C} = \frac{5}{3}$

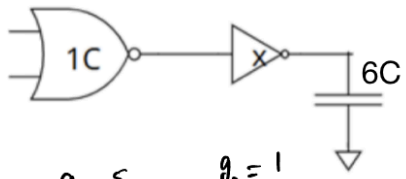
$g_D = \frac{7C}{3C} = \frac{7}{3}$

Q5) Consider the two alternative circuit implementations of a 2-input OR gate as shown in the figure below. Provide an intuitive argument to determine which design is expected to demonstrate slow performance. **(0.5 marks)** Support your reasoning with a quantitative analysis by calculating the path effort, delay **(1 mark)**, and the input capacitances x and y required to achieve this delay **(1 mark)**. Also size the corresponding transistors accordingly **(1 mark)**. **(CO2, 3.5 marks)**





Path logical effort for 1st circuit, G1 = (5/3)*1 = 5/3 and for 2nd circuit, G2 = 1*(4/3) = 4/3
Since G1>G2, intuitively it seems design 1 is expected to demonstrate slow performance.



$g_1 = \frac{5}{3}$ $\quad g_2 = 1$

$e_1 = g_1 g_2 = \frac{5}{3}$

$B = 1$

$H = \frac{6C}{1C} = 6$

$F = e_1 B H$

$F = 10$

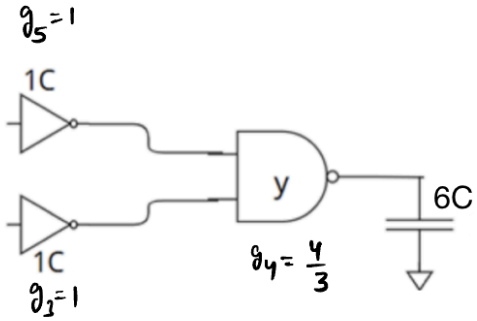
$\hat{f} = (F)^{1/N} = (10)^{1/2}$

$\hat{f} = 3.16$

$D_1 = N\hat{f} + P$

$D_1 = 2 \times 3.16 + (2+1)$

$D_1 = 9.32$



$g_5 = 1$

$g_3 = 1$ $\quad g_4 = \frac{4}{3}$

$e_2 = g_2 g_4 = \frac{4}{3}$

$B = 1$

$H = \frac{6C}{1C} = 6$

$F = e_2 B H$

$F = 8$

$\hat{f} = (F)^{1/N} = (8)^{1/2}$

$\hat{f} = 2.83$

$D_2 = N\hat{f} + P$

$D_2 = 2 \times 2.83 + (1+2)$

$D_2 = 8.66$

As we can see $D_1 > D_2$

$\hat{f} = g_2 h_2$

$3.16 = 1 \cdot \frac{6C}{x}$

$x = \frac{6}{3.16} = 1.9C$

Let inverter be upsized by k_1

$3 \cdot k_1 C = 1.9C$

$k_1 = 0.63$

for pmos $\Rightarrow 2 \times 0.63 = 1.26$

for nmos $\Rightarrow 1 \times 0.63 = 0.63$

$\hat{f} = g_4 h_4$

$2.83 = \frac{4}{3} \cdot \frac{6C}{y}$

$y = 2.83C$

Let NAND gate be upsized by k_2

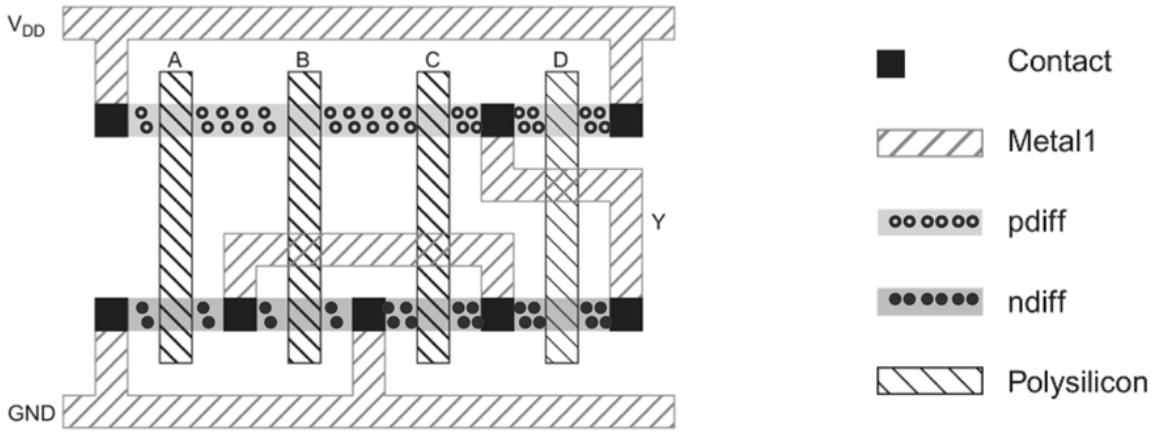
$4 \cdot k_2 C = 2.83C$

$k_2 = 0.71$

for pmos $\Rightarrow 2 \times 0.71 = 1.42$

for nmos $\Rightarrow 2 \times 0.71 = 1.42$

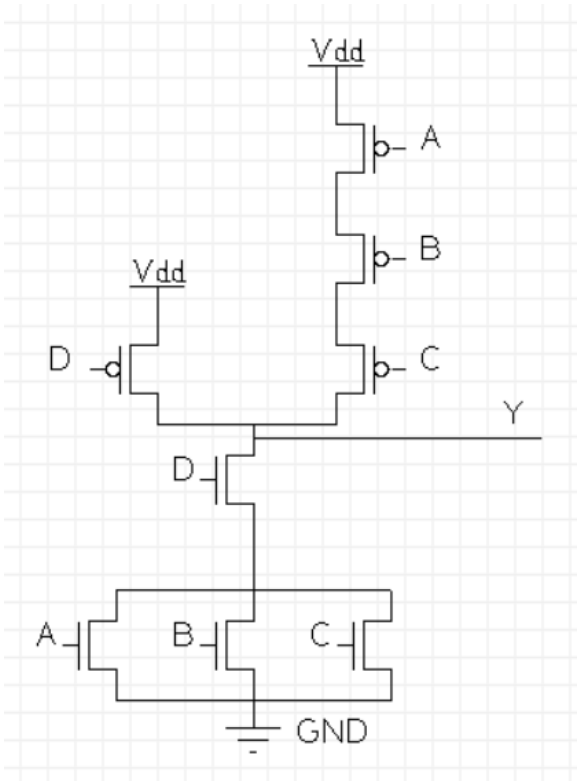
Q6) For the given layout **(CO5, 2 marks)**



a) Draw the transistor level schematic. **(1 mark)**

b) Derive the boolean expression of output Y **(1 mark)**

a)



b) Y = ((A+B+C).D)'

Q7) [Bonus] A product is designed in 90nm technology and takes up 100mm2 area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs.10. The designers use a denser version of libraries to reduce the area to 70mm2. Assuming the same Defectivity, D0, what is the new expected Yield? The product is still sold for Rs.100/-. How much profit does the company make now per product sold? **(CO1, 2 marks)**

Assume that 100 dies were manufactured per wafer.
At 56% yield, every wafer earns Rs.5600/-
At this sale price, profit is Rs.560/- (Rs. 10/- per die sold).

Yield is inversely dependent on Area.
When the Area reduces to 70mm2. Yield changes to 56/(0.7) = 80%
Total dies made now = (100/70)*100=142
Therefore, no of non-defective dies are= 142*0.8=113.6, which is equivalent to 113.
So, now 57 extra dies can be sold at Rs.100/-
Extra profit = Rs. 5700/
Total profit = Rs. 6260/ Profit per die = 6260 / 113 = Rs. 55 (approx)

So, with a 30% reduction in area, total profit jumped to almost 11 times, and profit per sold die increased to about 5 times. Therefore, the area is considered as one of the most important Figures of Merit in the VLSI industry.

Tab 3

Digital VLSI Design (ECE-314/514)

Mid-Sem Exam Set-C

22nd September 2025 [Time: 3:00-4:00 PM]

Maximum Marks: 25 Marks | Duration: 60 minutes

Name _____ | Roll No. _____

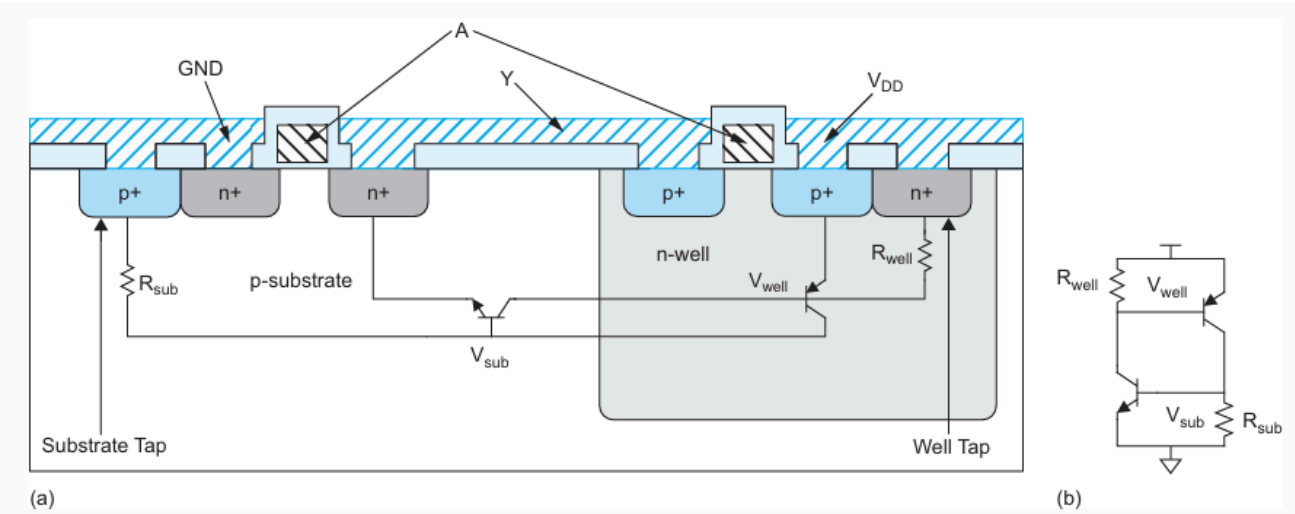
Instructions

1. This is a closed-book exam
2. Use of calculators is permitted. Use of mobile phones is strictly not allowed.
3. There are multiple sets of question papers. Write your set on your answer sheet.
3. There are a total of 7 questions in the paper and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following questions. **(CO1, 8 marks)**

a) What is the phenomenon in which CMOS chips tend to develop a low resistance path between VDD and GND, causing catastrophic meltdown? Describe briefly this phenomenon - how and when this phenomenon is triggered? How can this be prevented? **(2 marks)**

Latch-up is a condition where multiple p-n junctions of the S/D regions of MOSFETs form a back-to-back pnp-npn BJT latch.



These create a positive feedback loop when Rwell and Rsub are large, causing the BJTs to turn ON. This results in a sudden current surge. Due to positive feedback, this current keeps growing and can result in chip meltdown (burnout).

It can be prevented by using a sufficient number of taps/strap connections, which results in a small value of Rsub and Rwell, preventing these parasitic BJTs from turning ON.

b) Why is Tungsten (W) preferred over Copper (Cu) for making contacts in CMOS technology? **(1 mark)**

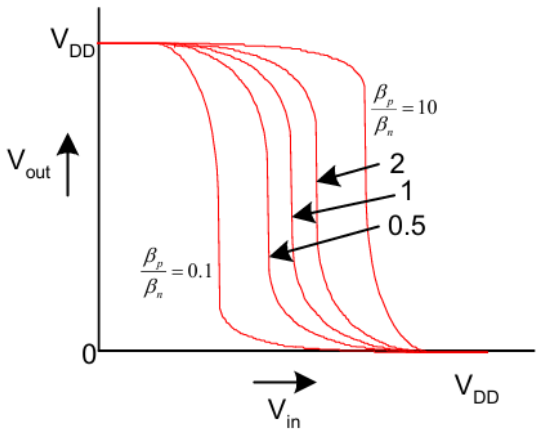
Copper diffuses rapidly into silicon and silicon dioxide and creates intermediate energy states in the band gap of silicon. This degrades the semiconductor behaviour of silicon, and transistor action is severely impacted.

Tungsten has a much higher melting point and is ductile. It doesn't interact with Silicon substrate. Thus it is a good choice for contacts.

c) Explain the effect of β-ratio on noise margins and propagation delays in a CMOS inverter**.** **(2 marks)**

When we increase the beta ratio, PMOS gets stronger, the VTC curve as shown in the image shifts towards right, so the ability to detect low logic levels (VIL) increases, thus low noise margin NML (VIL-VOL) improves and high noise margin NMH (VOH-VIH) degrades as VIH increases.

Rise propagation delay Tplh decreases as stronger PMOS is able to charge the output load faster and fall propagation delay Tphl increases as it takes more time for weaker NMOS to discharge the same output load.



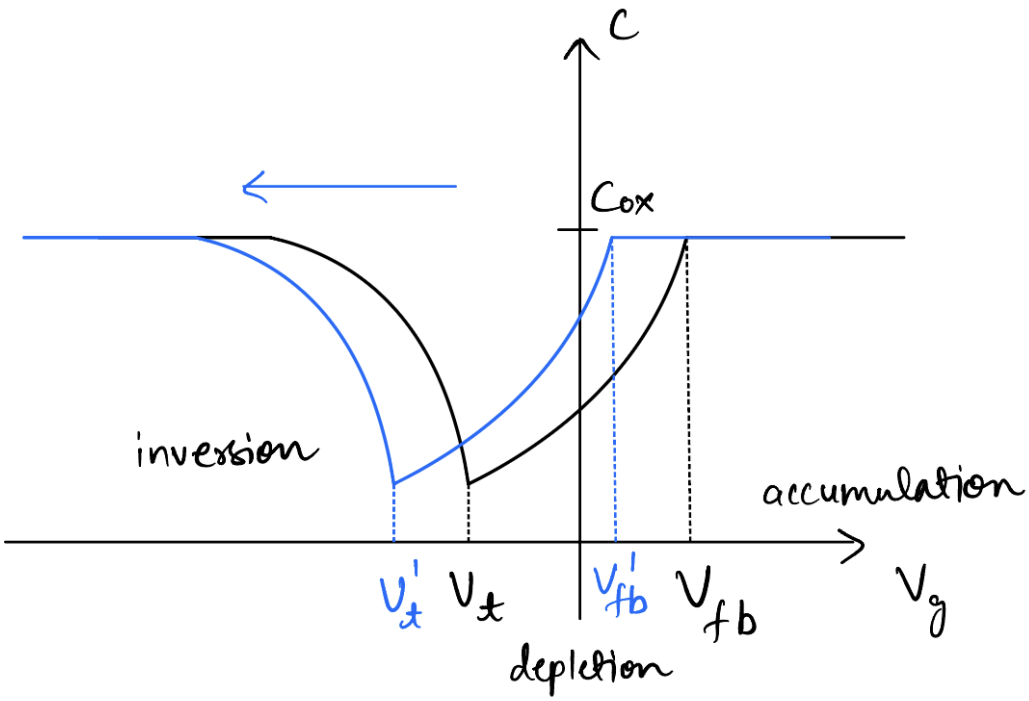
OR

When we decrease the beta ratio, NMOS gets stronger, the VTC curve as shown in the image shifts towards left, so the ability to detect high logic levels increases (VIH reduces), thus high noise margin NMH (VOH-VIH) improves and low noise margin NML (VIL-VOL) degrades as VIL reduces.

Fall propagation delay Tphl decreases as stronger NMOS is able to discharge the output load faster and rise propagation delay Tplh increases as it takes more time for weaker PMOS to charge the same output load.

d) Draw the C–V characteristics plot of a PMOS transistor with proper labelling. If positive charges are implanted in the oxide layer, redraw the curve showing in which direction it shifts? **(2 marks)**

If positive charges are implanted in the oxide layer, we need to apply more negative Vg to create the inversion layer. This can be seen as threshold voltage becomes more negative and the C-V curve shifts towards left.



e) Explain the effect of change in temperature on subthreshold current and ON current. **(1 mark)**

In the subthreshold region of operation, there are few free carriers. As the temperature increases, carriers are generated due to thermal generation. Due to the availability of more charge carriers, the subthreshold current increases.

On the other hand, ON current is constituted by free carriers present in the conduction band. Due to higher voltage at the gate, there are a large number of carriers in the conduction band. As we increase the temperature, the increase in the number of carriers due to thermal generation is only marginal. However, there are more lattice vibrations and therefore the number of collisions between the carriers increases. This results in reduced mobility of the carriers, resulting in a decrease in the ON current.

Q2) Complete the table below with the worst-case PVT conditions for different FOMs. **(CO1, 1.5 marks)**

Figure of Merit (FoM)	Process	Voltage	Temperature
Power	FF	High	Low
Leakage	FF	High	High
Contamination Delay	FF	High	Low

Q3) Nikhil is a design engineer at company X. While performing the verification process of a digital circuit at low voltage and high temperature, the delay specifications are met. He expects the specification to be met at low voltage and low temperature also, but it fails. Explain the reason behind this? **(CO3, 1 mark)**

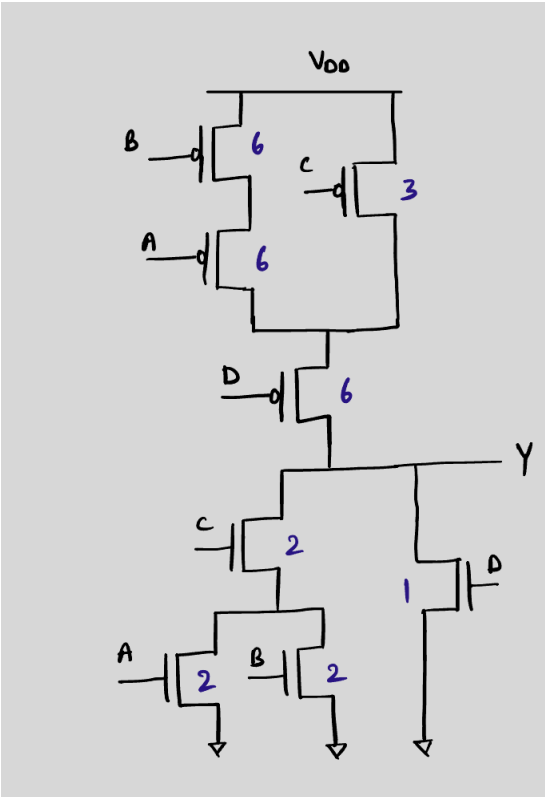
At high temperatures, there are more lattice vibrations. This results in an increased number of collisions between the charge carriers and the lattice. This results in reduced mobility at high temperatures.

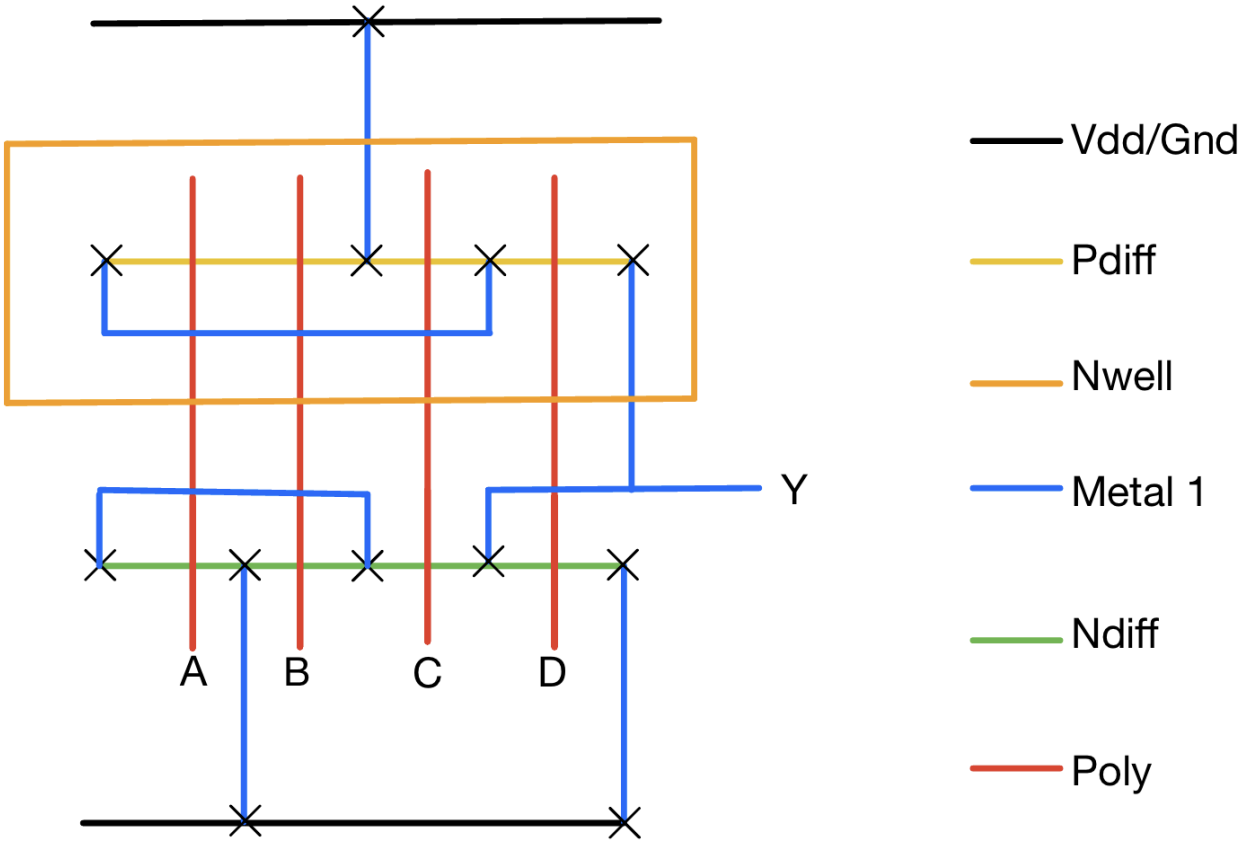
However, at low voltages, high temperature also results in more thermal generation. At low voltages, free carriers are few in number and therefore thermal generation induced carriers result in a significant increase in ON current (sufficient enough to offset the impact of reduced mobility due to lattice vibrations).

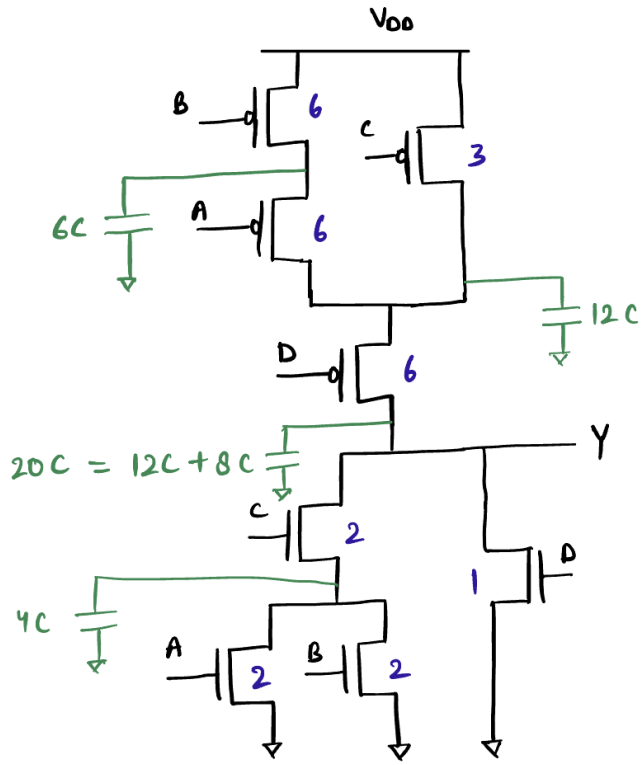
Therefore, while at high voltages, Nikhil's assumption would have been correct, it is not valid at low voltages. This phenomenon is called temperature inversion.

Q4) Consider the Boolean expression Y = ((A+B).C+D)'. Implement its schematic in static CMOS design style and size the transistors with respect to unit inverter **(1 mark)** and draw the stick diagram **(2 marks)** considering as much sharing of S/D as possible and do the following: **(9 marks)**

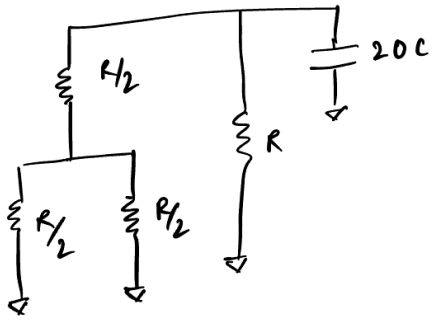
- **a)** Indicate the capacitances at each node in the schematic while also considering an additional load of 12C at the output. **(CO1, 1 mark)**
- **b)** Calculate the Contamination Rise/Fall Delay using Elmore Delay. **(CO2, 2 marks)**
- **c)** Calculate the Propagation Rise/Fall Delay using Elmore Delay. **(CO3, 2 marks)**
- **d)** Calculate the logical effort of each input. **(CO3, 1 mark)**




Y
A
B
C
D
Vdd/Gnd
Pdiff
Nwell
Metal 1
Ndiff
Poly



CD fall :

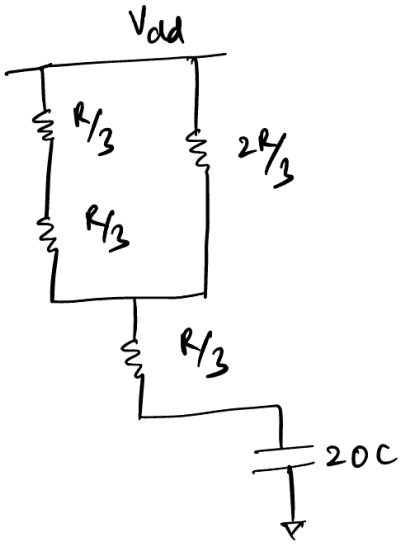


$t_{cdf} = 20\,C \cdot R_{eq}$

$t_{cdf} = 20 \cdot \frac{3R}{7}$

$t_{cdf} = \frac{60RC}{7}$

CD Rise

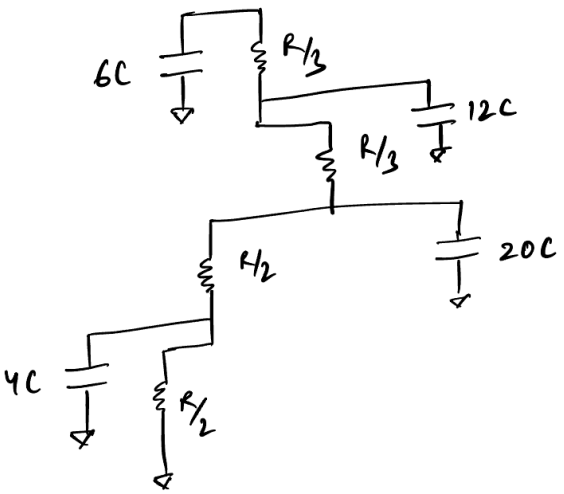


$t_{cdr} = 20\,C \cdot R_{eq}$

$t_{cdr} = 20\,C \cdot \frac{2R}{3}$

$t_{cdr} = \frac{40}{3} RC$.

PD fall



$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 20C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 12C + \left(\frac{R}{2}+\frac{R}{2}\right)6C$$

$$= 2RC + 20RC + 12RC + 6RC$$

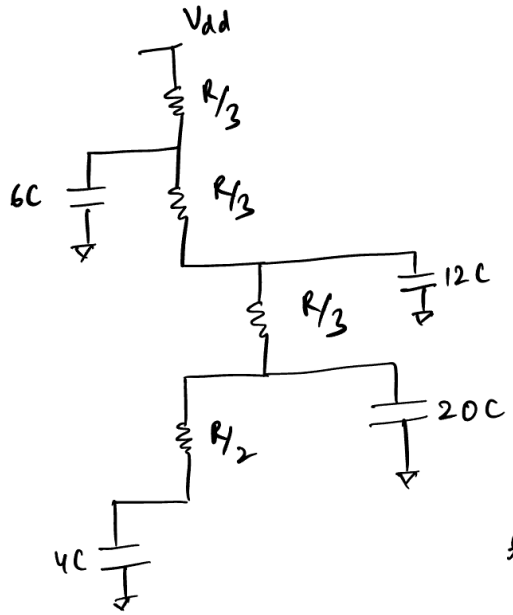
$$t_{pdf} = 40RC$$

Considering only 50 %.

$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 20C$$

$$= 22RC$$

PD Rise



$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 20C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 4C$$

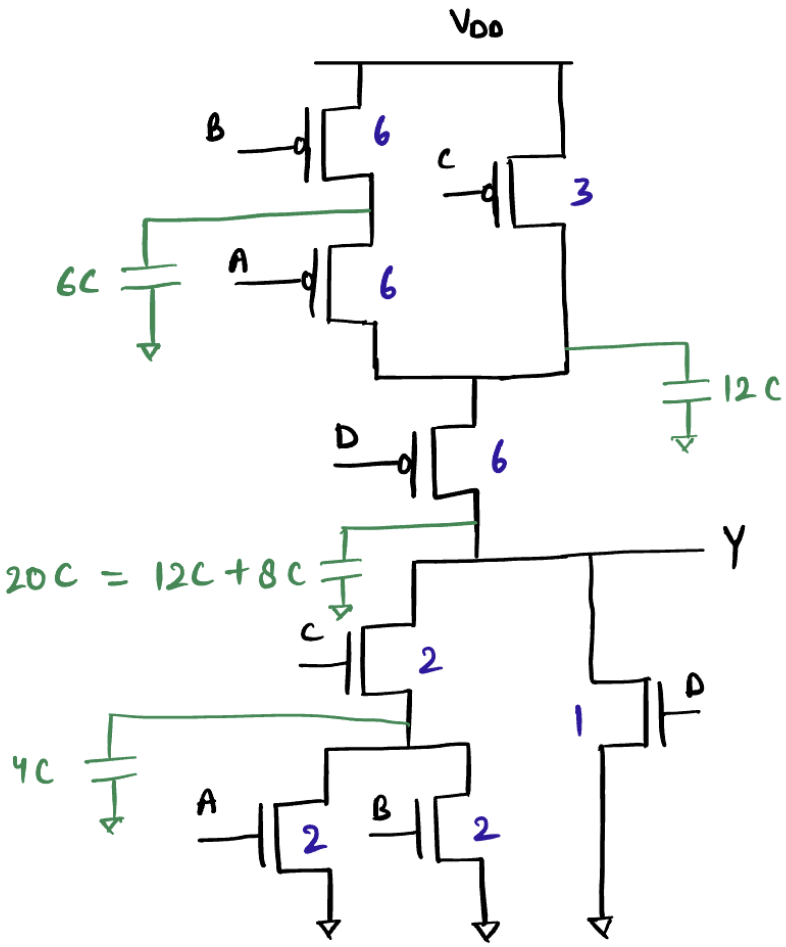
$$t_{pdr} = 2RC + 8RC + 20RC + 4RC$$

$$= 34RC.$$

Considering only 50 %.

$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 20C$$

$$t_{pdr} = 30RC$$



Logical effort :-

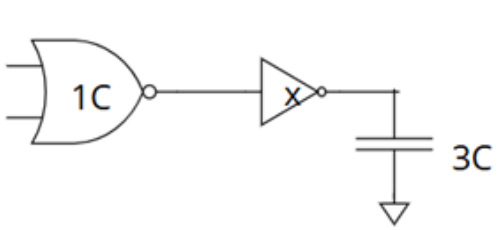
$g_A = \frac{8C}{3C} = \frac{8}{3}$

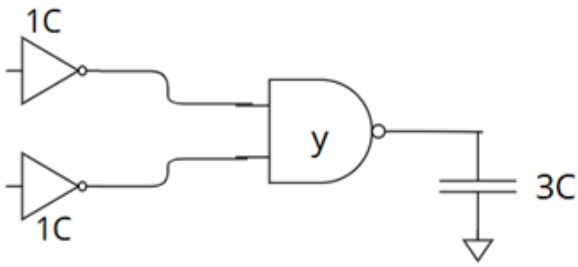
$g_B = \frac{8C}{3C} = \frac{8}{3}$

$g_C = \frac{5C}{3C} = \frac{5}{3}$

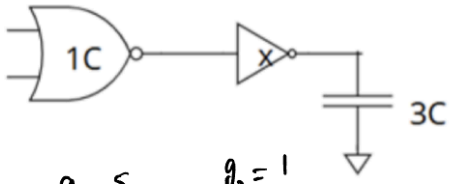
$g_D = \frac{7C}{3C} = \frac{7}{3}$

Q5) Consider the two alternative circuit implementations of a 2-input OR gate as shown in the figure below. Provide an intuitive argument to determine which design is expected to demonstrate slow performance. **(0.5 marks)** Support your reasoning with a quantitative analysis by calculating the path effort, delay **(1 mark)**, and the input capacitances x and y required to achieve this delay **(1 mark)**. Also size the corresponding transistors accordingly **(1 mark)**. **(CO2, 3.5 marks)**





Path logical effort for 1st circuit, G1 = (5/3)*1 = 5/3 and for 2nd circuit, G2 = 1*(4/3) = 4/3
Since G1>G2, intuitively it seems design 1 is expected to demonstrate slow performance.



$g_1 = \frac{5}{3}$ $\quad g_2 = 1$

$G_1 = g_1 g_2 = \frac{5}{3}$

$B = 1$

$H = \frac{3C}{1C} = 3$

$F = G_1 B H$

$F = 5$

$\hat{f} = (F)^{1/N} = (5)^{1/2}$

$\hat{f} = 2.23$

$D_1 = N\hat{f} + P$

$D_1 = 2 \times 2.23 + (2+1)$

$D_1 = 7.46$

$\hat{f} = g_2 h_2$

$2.23 = 1 \cdot \frac{3C}{x}$

$x = 1.345C$

Let inverter be upsized by k_1

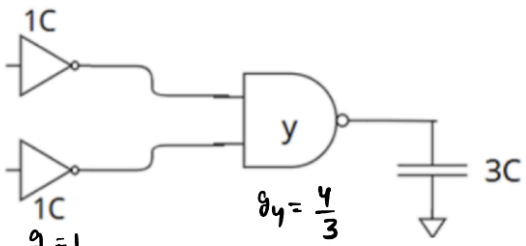
$3 \cdot k_1 C = 1.345C$

$k_1 = 0.45$

for pmos $\Rightarrow 2 \times 0.45 = 0.9$

for nmos $\Rightarrow 1 \times 0.45 = 0.45$

$g_5 = 1$



$g_3 = 1$ $\quad g_4 = \frac{4}{3}$

$G_2 = g_3 g_4 = \frac{4}{3}$

$B = 1$

$H = \frac{3C}{1C} = 3$

$F = G_2 B H$

$F = 4$

$\hat{f} = (F)^{1/N} = (4)^{1/2}$

$\hat{f} = 2$

$D_2 = N\hat{f} + P$

$D_2 = 2 \times 2 + (1+2)$

$D_2 = 7$

As we can see $D_1 > D_2$

$\hat{f} = g_4 h_4$

$2 = \frac{4}{3} \cdot \frac{3C}{y}$

$y = 2C$

Let NAND gate be upsized by k_2

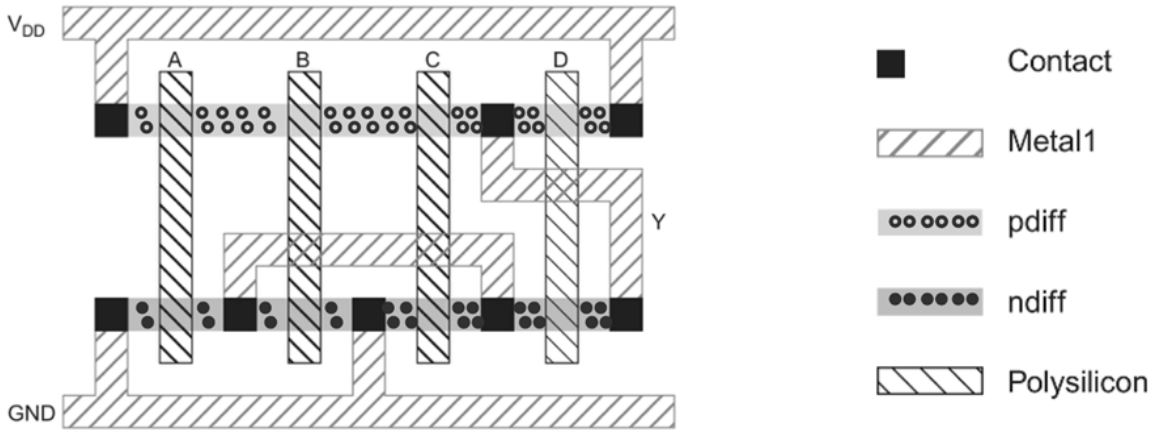
$4 \cdot k_2 C = 2C$

$k_2 = 0.5$

for pmos $\Rightarrow 2 \times 0.5 = 1$

for nmos $\Rightarrow 2 \times 0.5 = 1$

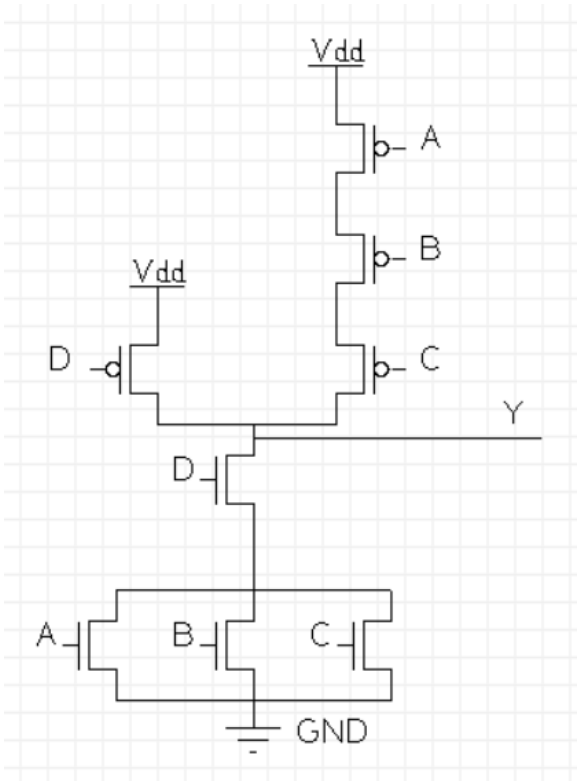
Q6) For the given layout **(CO5, 2 marks)**



a) Draw the transistor level schematic. **(1 mark)**

b) Derive the boolean expression of output Y **(1 mark)**

a)



b) Y = ((A+B+C).D)'

Q7) [Bonus] A product is designed in 90nm technology and takes up 100mm2 area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs.10. The designers use a denser version of libraries to reduce the area to 80mm2. Assuming the same Defectivity, D0, what is the new expected Yield? The product is still sold for Rs.100/-. How much profit does the company make now per product sold? **(CO1, 2 marks)**

Assume that 100 dies were manufactured per wafer.
At 56% yield, every wafer earns Rs.5600/-
At this sale price, profit is Rs.560/- (Rs. 10/- per die sold).

Yield is inversely dependent on Area.
When the Area reduces to 80mm2. Yield changes to 56/(0.8) = 70%
Total dies made now = (100/80)*100=125
Therefore, no of non-defective dies are= 125*0.7=87.5, which is equivalent to 87.
So, now 31 extra dies can be sold at Rs.100/-
Extra profit = Rs. 3100/
Total profit = Rs. 3660/ Profit per die = 3660 / 87 = Rs. 42 (approx)

So, with a 20% reduction in area, total profit jumped to almost 7 times, and profit per sold die increased to about 4 times. Therefore, the area is considered as one of the most important Figures of Merit in the VLSI industry.

Tab 4

Digital VLSI Design (ECE-314/514)

Mid-Sem Exam Set-D

22nd September 2025 [Time: 3:00-4:00 PM]

Maximum Marks: 25 Marks | Duration: 60 minutes

Name _____ | Roll No. _____

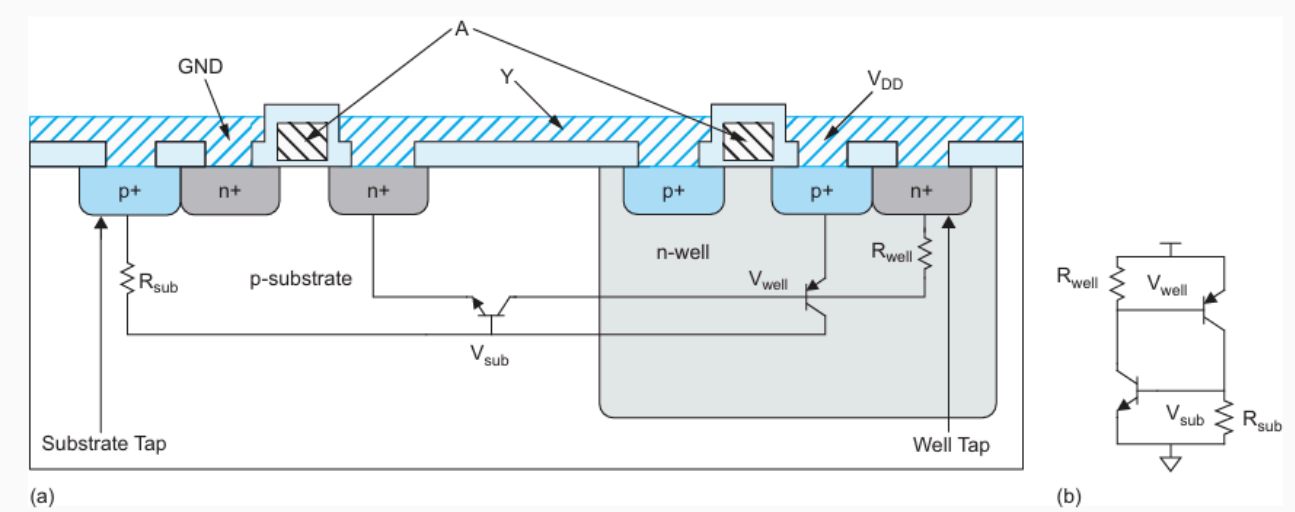
Instructions

1. This is a closed-book exam
2. Use of calculators is permitted. Use of mobile phones is strictly not allowed.
3. There are multiple sets of question papers. Write your set on your answer sheet.
3. There are a total of 7 questions in the paper and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following questions. **(CO1, 8 marks)**

a) What is the phenomenon in which CMOS chips tend to develop a low resistance path between VDD and GND, causing catastrophic meltdown? Describe briefly this phenomenon - how and when this phenomenon is triggered? How can this be prevented? **(2 marks)**

Latch-up is a condition where multiple p-n junctions of the S/D regions of MOSFETs form a back-to-back pnp-npn BJT latch.



These create a positive feedback loop when Rwell and Rsub are large, causing the BJTs to turn ON. This results in a sudden current surge. Due to positive feedback, this current keeps growing and can result in chip meltdown (burnout).

It can be prevented by using a sufficient number of taps/strap connections, which results in a small value of Rsub and Rwell, preventing these parasitic BJTs from turning ON.

b) Why is Tungsten (W) preferred over Copper (Cu) for making contacts in CMOS technology? **(1 mark)**

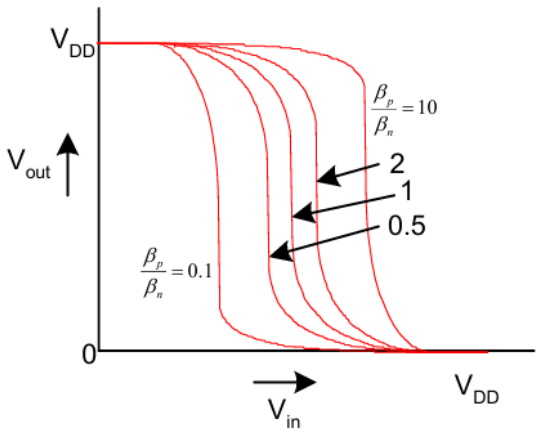
Copper diffuses rapidly into silicon and silicon dioxide and creates intermediate energy states in the band gap of silicon. This degrades the semiconductor behaviour of silicon, and transistor action is severely impacted.

Tungsten has a much higher melting point and is ductile. It doesn't interact with Silicon substrate. Thus it is a good choice for contacts.

c) Explain the effect of β-ratio on noise margins and propagation delays in a CMOS inverter**.** **(2 marks)**

When we increase the beta ratio, PMOS gets stronger, the VTC curve as shown in the image shifts towards right, so the ability to detect low logic levels (VIL) increases, thus low noise margin NML (VIL-VOL) improves and high noise margin NMH (VOH-VIH) degrades as VIH increases.

Rise propagation delay Tplh decreases as stronger PMOS is able to charge the output load faster and fall propagation delay Tphl increases as it takes more time for weaker NMOS to discharge the same output load.



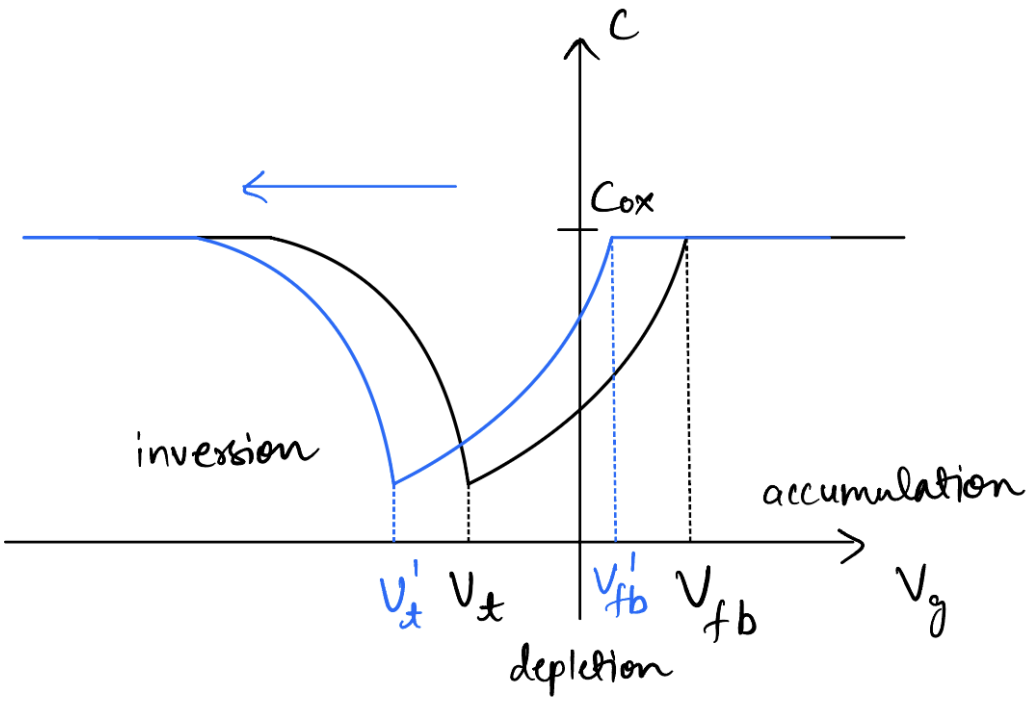
OR

When we decrease the beta ratio, NMOS gets stronger, the VTC curve as shown in the image shifts towards left, so the ability to detect high logic levels increases (VIH reduces), thus high noise margin NMH (VOH-VIH) improves and low noise margin NML (VIL-VOL) degrades as VIL reduces.

Fall propagation delay Tphl decreases as stronger NMOS is able to discharge the output load faster and rise propagation delay Tplh increases as it takes more time for weaker PMOS to charge the same output load.

d) Draw the C–V characteristics plot of a PMOS transistor with proper labelling. If positive charges are implanted in the oxide layer, redraw the curve showing in which direction it shifts? **(2 marks)**

If positive charges are implanted in the oxide layer, we need to apply more negative Vg to create the inversion layer. This can be seen as threshold voltage becomes more negative and the C-V curve shifts towards left.



e) Explain the effect of change in temperature on subthreshold current and ON current. **(1 mark)**

In the subthreshold region of operation, there are few free carriers. As the temperature increases, carriers are generated due to thermal generation. Due to the availability of more charge carriers, the subthreshold current increases.

On the other hand, ON current is constituted by free carriers present in the conduction band. Due to higher voltage at the gate, there are a large number of carriers in the conduction band. As we increase the temperature, the increase in the number of carriers due to thermal generation is only marginal. However, there are more lattice vibrations and therefore the number of collisions between the carriers increases. This results in reduced mobility of the carriers, resulting in a decrease in the ON current.

Q2) Complete the table below with the worst-case PVT conditions for different FOMs. **(CO1, 1.5 marks)**

Figure of Merit (FoM)	Process	Voltage	Temperature
Leakage	FF	High	High
Contamination Delay	FF	High	Low
Power	FF	High	Low

Q3) Nikhil is a design engineer at company X. While performing the verification process of a digital circuit at low voltage and high temperature, the delay specifications are met. He expects the specification to be met at low voltage and low temperature also, but it fails. Explain the reason behind this? **(CO3, 1 mark)**

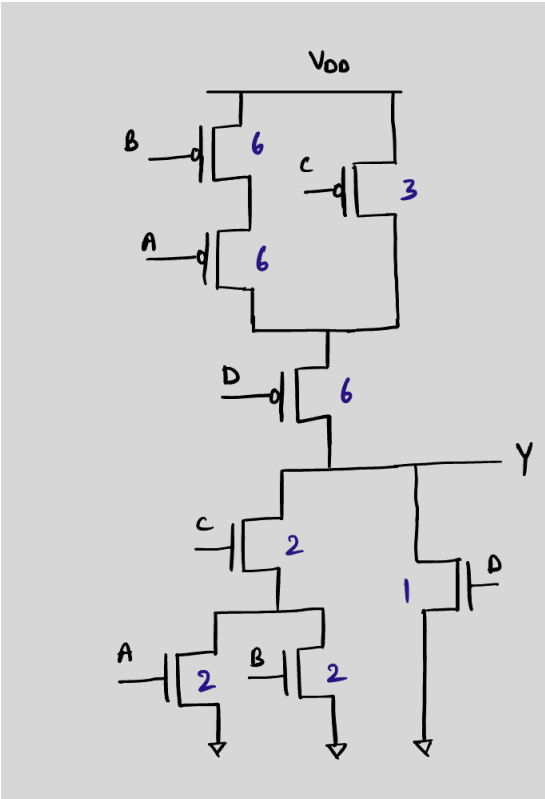
At high temperatures, there are more lattice vibrations. This results in an increased number of collisions between the charge carriers and the lattice. This results in reduced mobility at high temperatures.

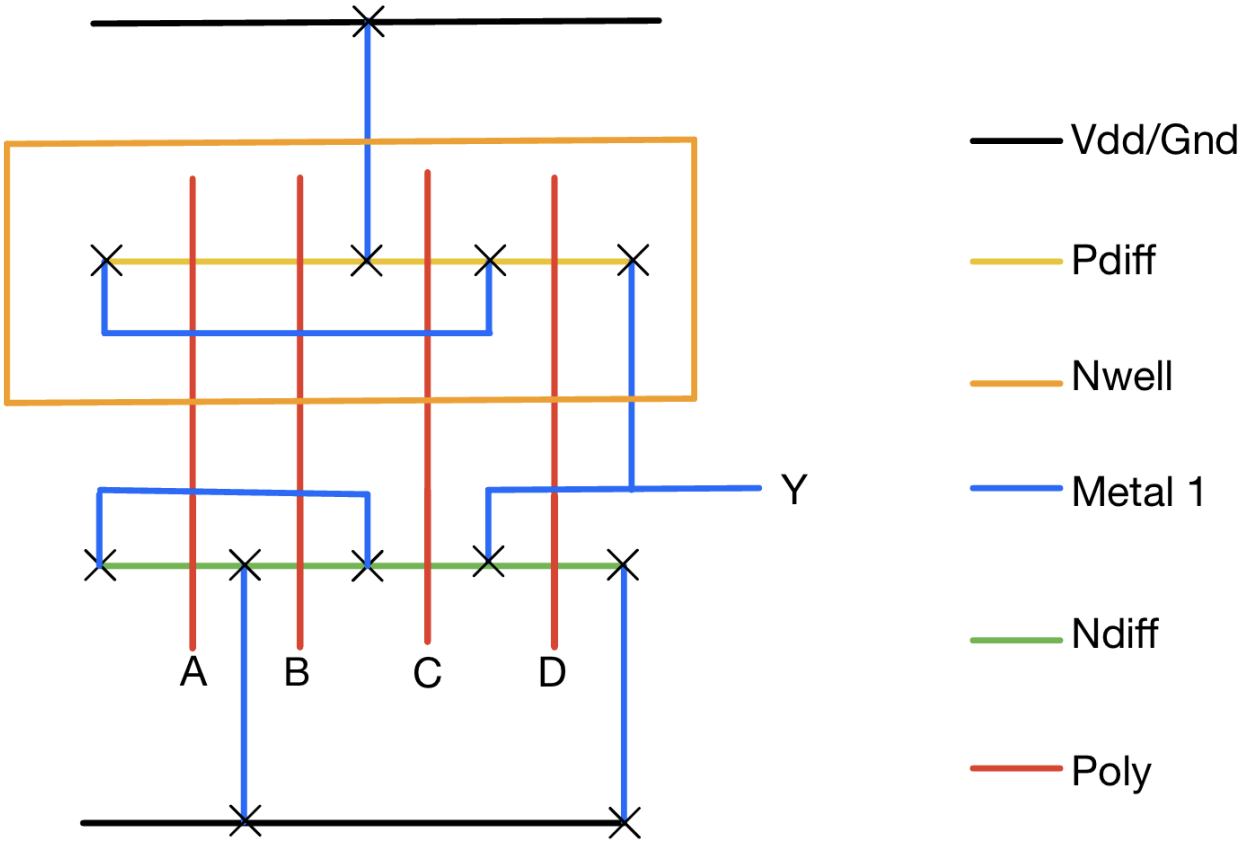
However, at low voltages, high temperature also results in more thermal generation. At low voltages, free carriers are few in number and therefore thermal generation induced carriers result in a significant increase in ON current (sufficient enough to offset the impact of reduced mobility due to lattice vibrations).

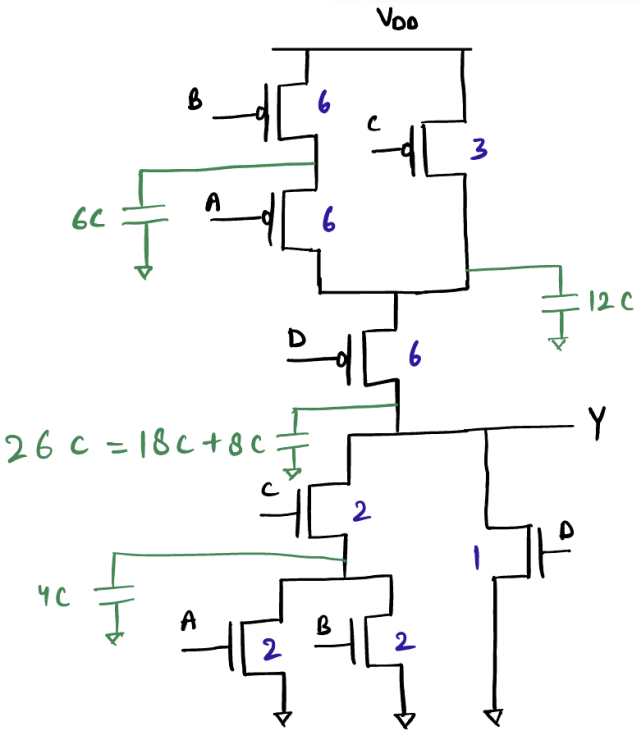
Therefore, while at high voltages, Nikhil's assumption would have been correct, it is not valid at low voltages. This phenomenon is called temperature inversion.

Q4) Consider the Boolean expression Y = ((A+B).C+D)'. Implement its schematic in static CMOS design style and size the transistors with respect to unit inverter **(1 mark)** and draw the stick diagram **(2 marks)** considering as much sharing of S/D as possible and do the following: **(9 marks)**

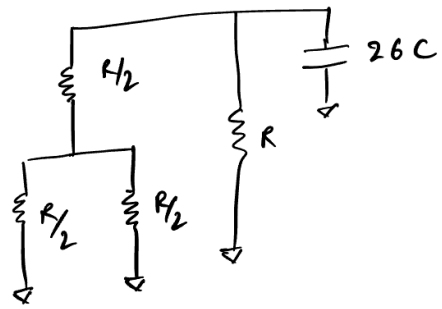
- **a)** Indicate the capacitances at each node in the schematic while also considering an additional load of 18C at the output. **(CO1, 1 mark)**
- **b)** Calculate the Contamination Rise/Fall Delay using Elmore Delay. **(CO2, 2 marks)**
- **c)** Calculate the Propagation Rise/Fall Delay using Elmore Delay. **(CO3, 2 marks)**
- **d)** Calculate the logical effort of each input. **(CO3, 1 mark)**




Y
A
B
C
D
Vdd/Gnd
Pdiff
Nwell
Metal 1
Ndiff
Poly



CD fall :

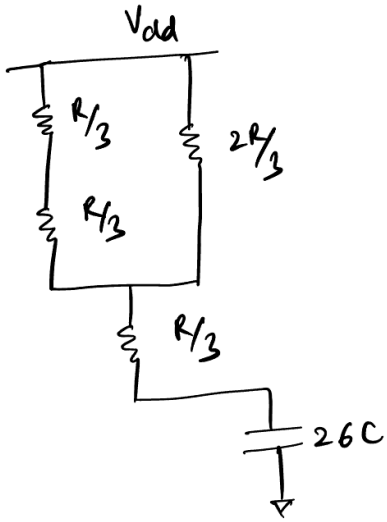


$t_{cdf} = 26\ C . R_{eq}$

$t_{cdf} = 26C . \frac{3R}{7}$

$t_{cdf} = \frac{78}{7} RC$

CD Rise

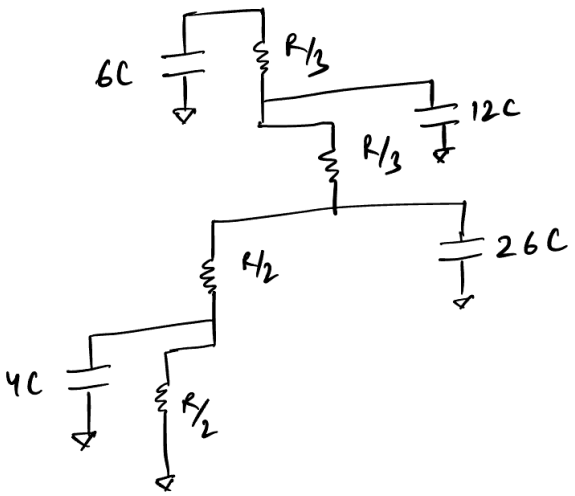


$t_{cdr} = 26\ C . R_{eq}$

$t_{cdr} = 26\ C . \frac{2R}{3}$

$t_{cdr} = \frac{52}{3} RC$

PD fall



$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 26C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 12C + \left(\frac{R}{2}+\frac{R}{2}\right)6C$$

$$= 2RC + 26RC + 12RC + 6RC$$

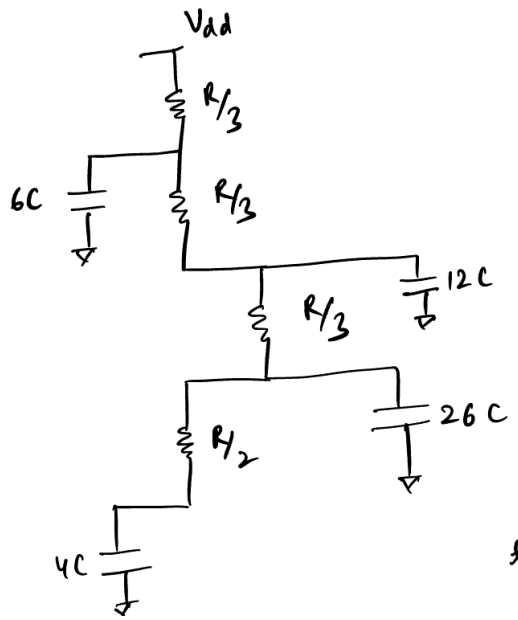
$$t_{pdf} = 46\,RC$$

Considering only 50 %.

$$t_{pdf} = \frac{R}{2}\cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right)\cdot 26C$$

$$= 28\,RC$$

PD Rise



$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 26C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 4C$$

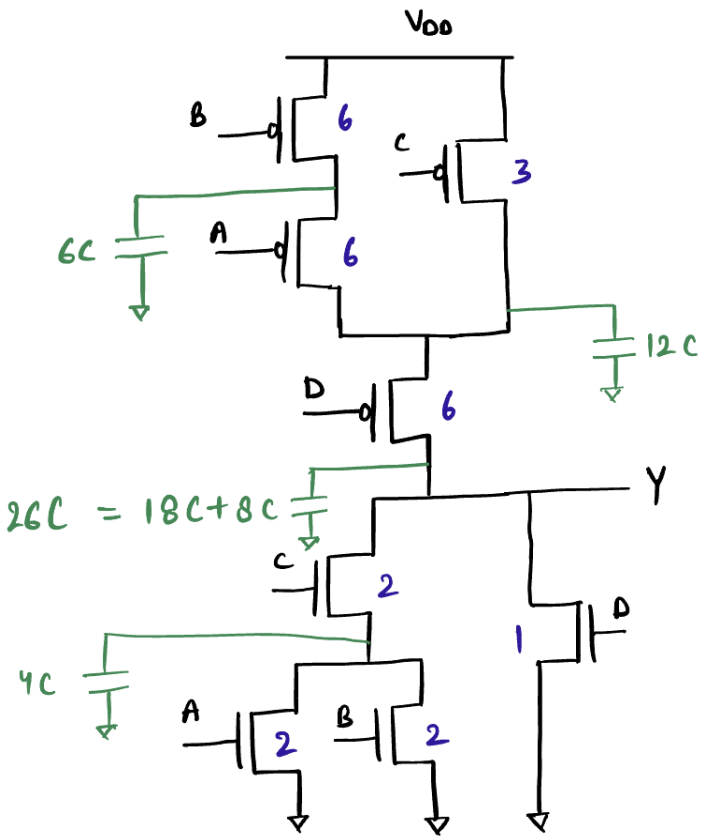
$$t_{pdr} = 2RC + 8RC + 26RC + 4RC$$

$$= 40\,RC$$

Considering only 50 %.

$$t_{pdr} = \frac{R}{3}\cdot 6C + \left(\frac{R}{3}+\frac{R}{3}\right)\cdot 12C + \left(\frac{R}{3}+\frac{R}{3}+\frac{R}{3}\right)\cdot 26C$$

$$t_{pdr} = 36\,RC$$



Logical effort :-

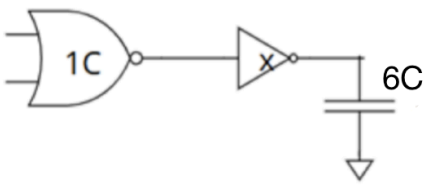
$g_A = \frac{8C}{3C} = \frac{8}{3}$

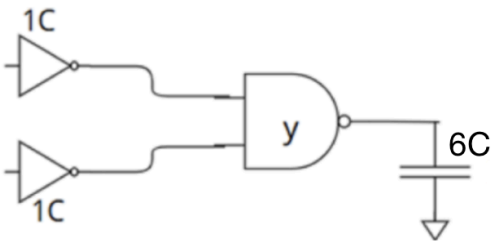
$g_B = \frac{8C}{3C} = \frac{8}{3}$

$g_C = \frac{5C}{3C} = \frac{5}{3}$

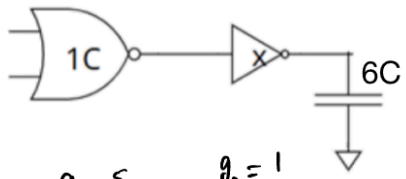
$g_D = \frac{7C}{3C} = \frac{7}{3}$

Q5) Consider the two alternative circuit implementations of a 2-input OR gate as shown in the figure below. Provide an intuitive argument to determine which design is expected to demonstrate slow performance. **(0.5 marks)** Support your reasoning with a quantitative analysis by calculating the path effort, delay **(1 mark)**, and the input capacitances x and y required to achieve this delay **(1 mark)**. Also size the corresponding transistors accordingly **(1 mark)**. **(CO2, 3.5 marks)**





Path logical effort for 1st circuit, G1 = (5/3)*1 = 5/3 and for 2nd circuit, G2 = 1*(4/3) = 4/3
Since G1>G2, intuitively it seems design 1 is expected to demonstrate slow performance.



$g_1 = \frac{5}{3}$ $\quad g_2 = 1$

$e_1 = g_1 g_2 = \frac{5}{3}$

$B = 1$

$H = \frac{6C}{1C} = 6$

$F = e_1 B H$

$F = 10$

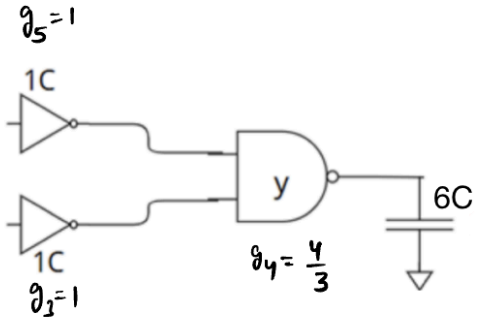
$\hat{f} = (F)^{1/N} = (10)^{1/2}$

$\hat{f} = 3.16$

$D_1 = N\hat{f} + P$

$D_1 = 2 \times 3.16 + (2+1)$

$D_1 = 9.32$



$g_5 = 1$

$g_3 = 1$ $\quad g_4 = \frac{4}{3}$

$e_2 = g_2 g_4 = \frac{4}{3}$

$B = 1$

$H = \frac{6C}{1C} = 6$

$F = e_2 B H$

$F = 8$

$\hat{f} = (F)^{1/N} = (8)^{1/2}$

$\hat{f} = 2.83$

$D_2 = N\hat{f} + P$

$D_2 = 2 \times 2.83 + (1+2)$

$D_2 = 8.66$

As we can see $D_1 > D_2$

$\hat{f} = g_2 h_2$

$3.16 = 1 \cdot \frac{6C}{x}$

$x = \frac{6}{3.16} = 1.9C$

Let inverter be upsized by k_1

$3 \cdot k_1 C = 1.9C$

$k_1 = 0.63$

for pmos $\Rightarrow 2 \times 0.63 = 1.26$

for nmos $\Rightarrow 1 \times 0.63 = 0.63$

$\hat{f} = g_4 h_4$

$2.83 = \frac{4}{3} \cdot \frac{6C}{y}$

$y = 2.83C$

Let NAND gate be upsized by k_2

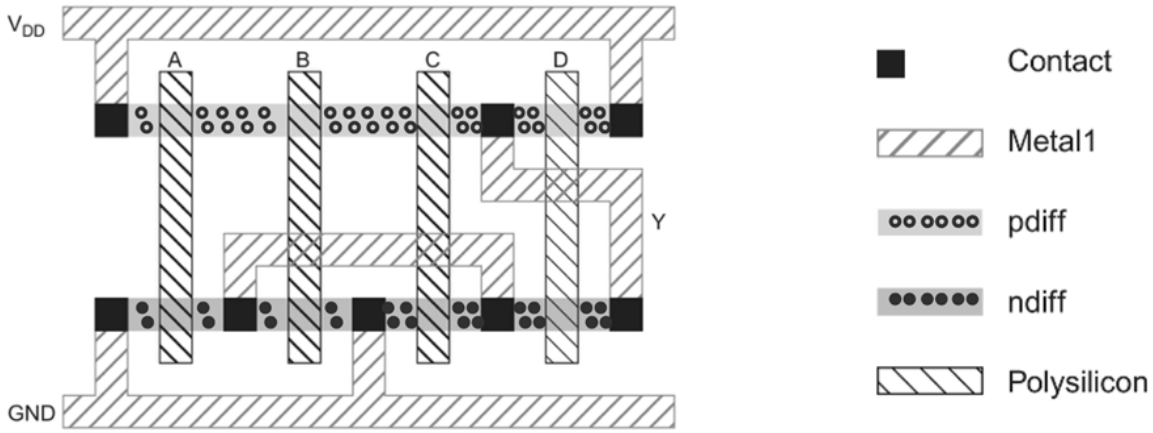
$4 \cdot k_2 C = 2.83C$

$k_2 = 0.71$

for pmos $\Rightarrow 2 \times 0.71 = 1.42$

for nmos $\Rightarrow 2 \times 0.71 = 1.42$

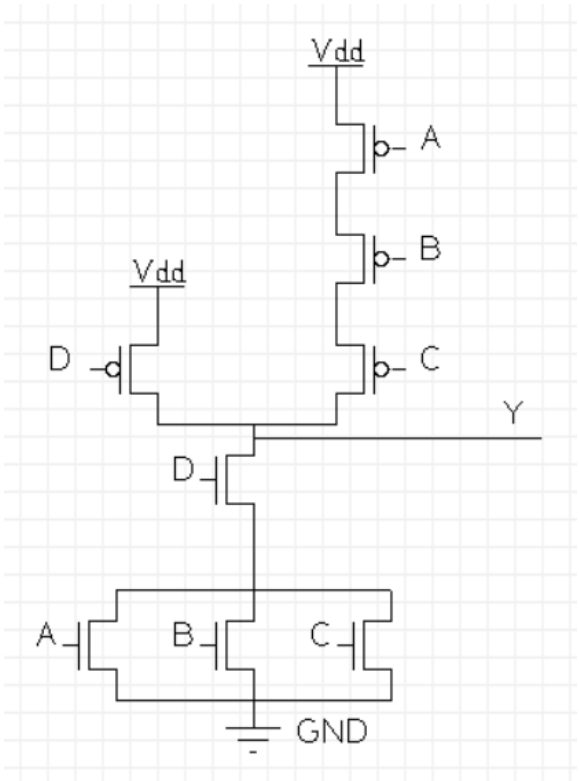
Q6) For the given layout **(CO5, 2 marks)**



a) Draw the transistor level schematic. **(1 mark)**

b) Derive the boolean expression of output Y **(1 mark)**

a)



b) Y = ((A+B+C).D)'

Q7) [Bonus] A product is designed in 90nm technology and takes up 100mm2 area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs.10. The designers use a denser version of libraries to reduce the area to 70mm2. Assuming the same Defectivity, D0, what is the new expected Yield? The product is still sold for Rs.100/-. How much profit does the company make now per product sold? **(CO1, 2 marks)**

Assume that 100 dies were manufactured per wafer.
At 56% yield, every wafer earns Rs.5600/-
At this sale price, profit is Rs.560/- (Rs. 10/- per die sold).

Yield is inversely dependent on Area.
When the Area reduces to 70mm2. Yield changes to 56/(0.7) = 80%
Total dies made now = (100/70)*100=142
Therefore, no of non-defective dies are= 142*0.8=113.6, which is equivalent to 113.
So, now 57 extra dies can be sold at Rs.100/-
Extra profit = Rs. 5700/
Total profit = Rs. 6260/ Profit per die = 6260 / 113 = Rs. 55 (approx)

So, with a 30% reduction in area, total profit jumped to almost 11 times, and profit per sold die increased to about 5 times. Therefore, the area is considered as one of the most important Figures of Merit in the VLSI industry.