VLSI Design Flow

Mid Semester Exam (27th February 2023)

Time allowed: 1 hour *Maximum Marks: 30*

1.

a. Optical Proximity Correction (OPC) is a Resolution Enhancement Techniques (RET) that pre-compensates a mask such that the features obtained on the mask is same as is desired. It add appropriate serifs, hammerheads, and mouse bites to the mask and improves the resolution of photolithography by compensating errors due to diffraction etc. It can avoid problems of rounding of corners, and line end pullback when the wavelength of light used in photolithography is greater than the feature size.

b. For performing functional coverage, a designer (or a verification engineer) needs to create a functional coverage model. This requires additional effort in determining the functional coverage of an RTL model. On the other hand, the code coverage can be determined directly by the RTL code, and does not require any extra effort from the designer.

c. In SoC design methodology, only IP integration or IP assembly is required. The internal details of IP are already available and hence no extra effort is required in creating a complex IP. Thus, SoC design methodology help reduce design effort.

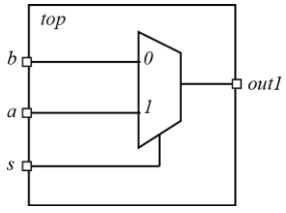
d. Event-based simulator should be used. An event-based simulator can capture events or changes in the signal within a clock cycle for combinational circuit elements. Hence, it can capture within-cycle glitches. A cycle-based simulator only computes values at clock edges. Hence, it will miss within-cycle glitches.

e. Uniquification create separate copies of the module for different instances. It is required when we want different instances of the same module to be synthesized differently.

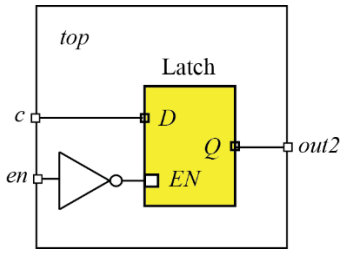
f. We can get a warning of a module being treated as black-box during elaboration when we instantiate a module in the model, while the definition of that module is missing. We can fix this problem by providing definition (or including the module or its file) that is missing. **[2+2+2+2+2+2 Marks]**

2.

a.



b.



3. Setup time = $20 + 12 - 50 = -18\,ps$
Hold time = $10 - 12 + 50 = 48\,ps$
Clock-to Q delay = $10 + 50 + 8 = 68\,ps$

4.

	Load=10 ff	Load=20 ff	Load=30 ff	Load=40 ff
Clk Slew=10ps	10	20	30	40
Clk Slew=20ps	20	30	40	50
Clk Slew=30ps	25	35	45	55
Clk Slew=40ps	28	38	48	58

	Clk Slew=10ps	Clk Slew=20ps	Clk Slew=30ps	Clk Slew=40ps
Data Slew=20ps	10	12	14	16
Data Slew=30ps	12	16	18	20
Data Slew=40ps	14	18	22	26
Data Slew=50ps	18	25	30	40

a) Path between F1 and F3.
Setup time of F3 = 16 ps
Clock to Q delay of F1 = 25 ps
Arrival Time = 25 + 100 ps = 125 ps
Required Time = 1000 – 16 ps = 984 ps
Slack = 984-125=859 ps

b) Path between F2 and F3.
Setup time of F3 = 16 ps
Clock to Q delay of F2 = 20 ps
Arrival Time = 20 + 100 ps = 120 ps
Required Time = 1000 – 16 ps = 984 ps
Slack = 984 – 120 ps = 864 ps

5.

a) The set of reachable states is {S1, S0, S2, S3}. And the characteristics functions is: a'b'c'+a'b'c+a'bc'+a'bc

b) The set of reachable states is {S4, S3}. And the characteristics functions is: ab'c'+a'bc