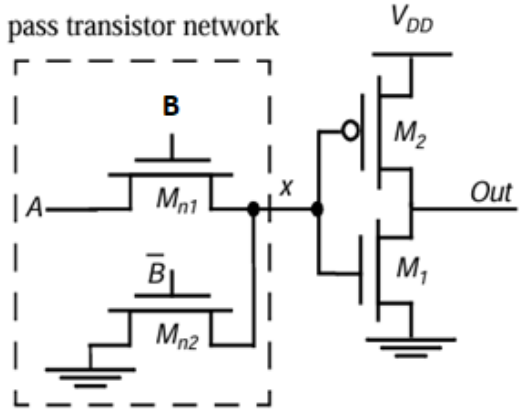
Digital VLSI Design (ECE 314/514)
End-Sem Examination
5-Dec-2023

Duration: 2 hr **MM: 30 marks/ 28 marks (for B.Tech)**

Q.1.a) Why does a FF need to satisfy setup time and hold time constraints? Explain in detail. **[1 mark]** [CO4]
b) Suppose you have designed a chip, and after fabrication, it fails. How would you determine if it is a setup failure or a hold time failure? **[1 mark]** [CO4]

Q2. Consider the circuit as shown below. Assume the inverter switches at VDD/2, neglect body effect, channel length modulation, and all parasitic capacitance throughout this problem.



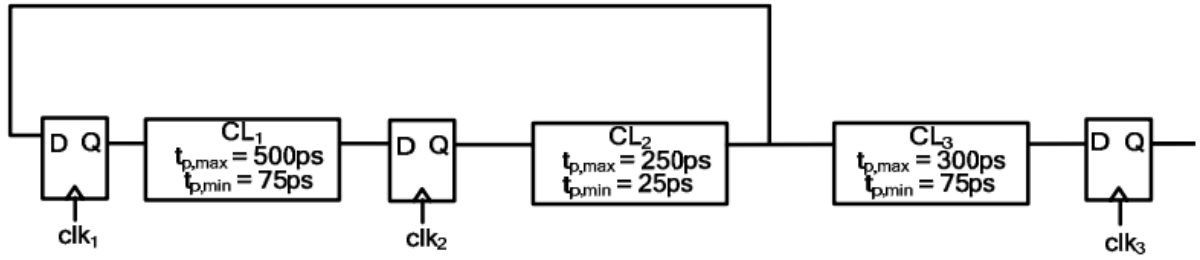
a) What is the logic function performed by this circuit? [1 mark] [CO4]
b) Explain why this circuit has non-zero static dissipation. [1 mark] [CO4]
c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain the constraints that you would consider when sizing this transistor. [2 marks] [CO4]

Q3. Answer the following questions.
a) Draw the schematic of a 2-input domino AND gate. **[1 mark]** [CO4]
b) If one engineer removed the footer nmos from the gate in part (a), how does this impact the delays compared to the original gate? **[1 mark]** [CO4]
c) Are there any failure modes? Please explain. **[1 mark]** [CO4]

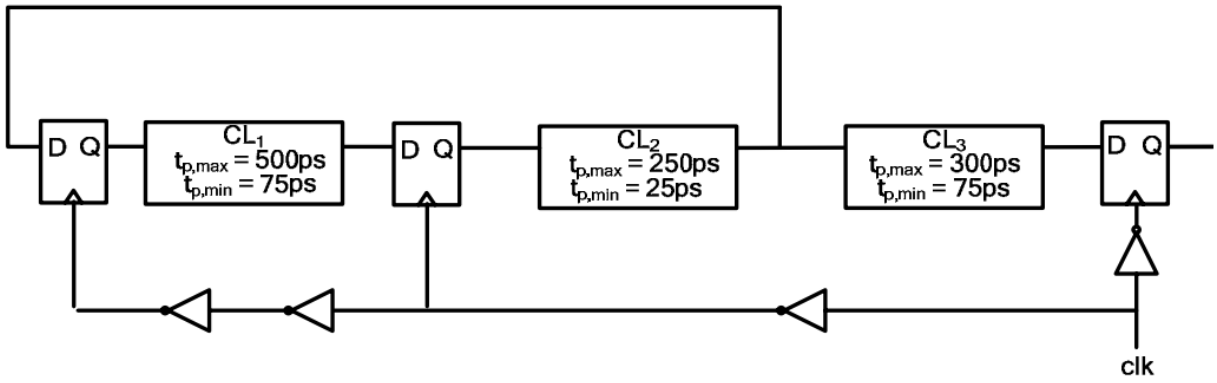
Q.4. Answer the following questions
a) What is sequencing overhead? **[1 mark]** [CO4]
b) What is adaptive sequencing? Describe any 2 adaptive sequencing methods in brief. **[3 marks]** [CO4]

Q. 5. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $\mathbf{t_{cq}}$ **= 50ps,** $\mathbf{t_{setup}}$ **= 50ps,** and $\mathbf{t_{hold}}$ **= 50ps**. You can assume that the clock has no jitter.

a) Assuming there is no skew between clk_1, clk_2, and clk_3, list all the timing constraint paths; what is the minimum clock cycle time for this pipeline? Are there any minimum delay (hold time) violations? **[3 marks]** [CO4]



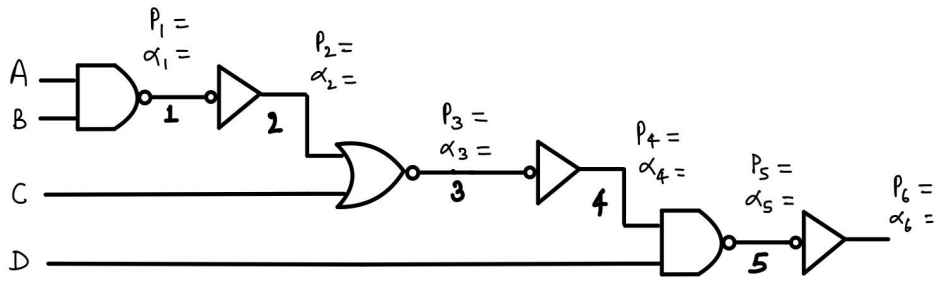
b) Now, we'll include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, what is the minimum clock cycle time? **[2 marks]** [CO4]



Q6. Answer any 4 of the following questions. If all parts are answered, then it will be considered 'bonus' **[4 x 1 marks + 2 x 1 marks bonus]** [CO5]

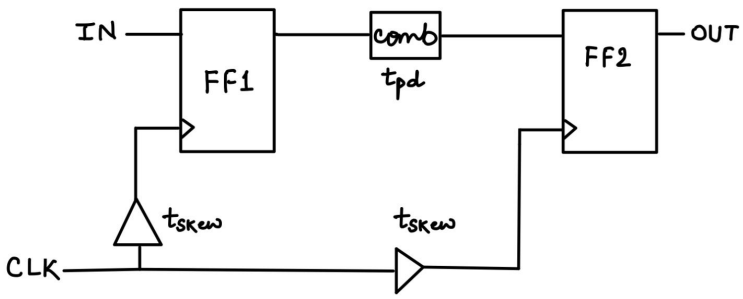
a) Why are non-volatile memories called non-volatile?
b) Give two examples of Non-Random Access Memory.
c) Which type of memory should be preferred if very high-speed access is the most important requirement?
d) Why are Flash memories denser than SRAMs?
e) Why are SRAMs better than Flash in terms of endurance?
f) Why are Design rules for layout allowed to be violated in SRAM array design?

Q7. a) Determine the activity factor at each node in the circuit, assuming the input probabilities Pa = Pb = Pc = Pd = 0.5. **[3 marks]** [CO3]



b) The circuit above (part-a) sees a total load capacitance of 10fF and is operated at 0.6V. The time period of the system clock is 2ns. Find the switching power of the circuit. **[1 mark]** [CO3]

Q8 .a) i) Calculate the maximum operational frequency of the following circuit. **[1 mark]** [CO4]



T_{pd} = 1ns
T_{hold} = 150ps
T_{setup} = 200ps
T_{cq} = 300ps
T_{skew} = 100ps

ii) Calculate the setup slack if the clock period is 2ns. **[1 mark]** [CO4]

b) If the 2nd FF is replaced with a negative edge-triggered FF, Calculate the maximum operating frequency. Assume same timing parameters. [**bonus for B.Tech students**] **[2 marks]** [CO4]