Digital VLSI Design (ECE-314/514)

End-Sem Exam

3rd December 2025 [Time: 2:30-3:30 PM]

Maximum Marks: 25 Marks | Duration: 60 minutes

Name _____ | Roll No._____

Instructions

1. This is a closed-book exam
2. Use of **calculators is permitted**. The use of mobile phones is strictly prohibited.
3. There are a total of 6 questions in the paper, and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following project-based questions in 50-100 words. **[CO1,CO2,CO3,CO4,CO5]**

a) Why is it important to distribute I/O pins across the layout rather than placing them along the same track while making layouts? Give two reasons. **[1 mark]**

b) What are the worst-case PVTs for characterising leakage of standard cells? **[1 mark]**

c) After post-layout simulations, we observe a significant degradation in delay compared to pre-layout estimates. What could be the two possible reasons for this, and what corrective actions should be taken? **[1 mark]**

d) What are the two advantages of using multi-bit latches or flip-flops? Additionally, why is it a bad idea to route the clock signal using polysilicon? Give two reasons. **[2 marks]**

e) How can setup and hold margins change post-layout, and how can these changes affect the overall design? **[2 marks]**

f) What could be two disadvantages of using an excessive number of contacts in a layout? **[1 mark]**

g) Do parasitic RCs extracted post-layout impact leakage when compared to pre-layout estimates? Justify your answer by giving two reasons. **[1 mark]**

h) Why is it recommended that I/O pins in standard cell layouts be designed to span across multiple tracks? Give two reasons. **[1mark]**

i) While designing a transmission-gate–based multiplexer, buffers are often inserted between successive transmission gate stages. What is the need for using these buffers? **[1 mark]**

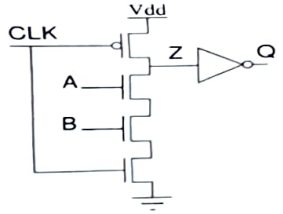
Q2) Consider a sequential circuit:

(a) When the clock frequency is increased, the circuit fails to operate correctly. What could be the reason for this behaviour, and what can be done to fix it so that the circuit works reliably? **[1.5 marks, CO4]**

(b) If the failure is independent of the clock frequency, what timing issue could be causing the failure, and how can it be fixed? **[1.5 marks, CO4]**

Q3) What is clock gating, and why is it used? **[2 marks, CO4]**

Q4) A dynamic Domino AND gate is precharged such that inputs A=B=0 and the intermediate dynamic node Z is precharged to VDD. During the evaluation phase, input A rises to '1' while B remains '0'. Ideally, the output should remain unchanged; however, it is observed that the voltage of node Z drops significantly, which can sometimes cause a logic error. **[2 marks, CO3]**



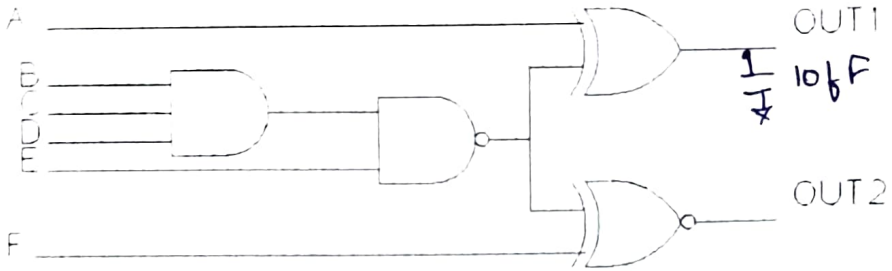
(a) What is this phenomenon called? Briefly explain why the voltage at node Z drops.

(b) What can be done to correct this?

Q5) Consider the figure below and answer the following:

(a) Calculate the activity factor of the output node OUT1 of the circuit given below. It is given that the probability of an input being high is 0.5 for all inputs. **[2 marks, CO3]**

(b) The circuit shown above sees a total load capacitance of 10fF and is operated at 1V. The time period of the system clock is 1ns. Find the switching power of the circuit. **[1 Mark, CO3]**



Q6) In the figure below, assume the following parameters of the FFs: t_{C2Q} = 150ps, t_{setup} = 50ps, and t_{hold} = 100ps. The clock has no jitter.

(a) The propagation delay (tpd) and the contamination delay (tcd) of each module are annotated. What is the minimum clock period (T) if there is no clock skew? **[2 marks,CO4]**

(b) If the skew between CK1 and CK2 is -100ps, and the skew between CK1 and CK3 is 50ps, then what is the minimum clock period? **[2 marks, CO4]**