VLSI Design Flow

Mid Semester Exam (8th March 2021)

Time allowed: 1 hour *Maximum Marks: 40*

Note:

I. ***All questions are compulsory.***
II. ***Marks are indicated in bold at the end of each question.***
III. ***Be crisp and precise in your answer so that you can complete the answers in 1 hour.***
IV. ***Use the marks allotted to each question as an indicator of how elaborate you need to answer.***
V. ***Cheating or use of unfair means will be dealt with as per institute policy.***

1. A software was profiled, and the % of time spent (on an average) in different functions are shown below.

Function name	% Time
F1	5
F2	3
F3	15
F4	5
F5	10
F6	30
F7	5
F8	25
F9	2

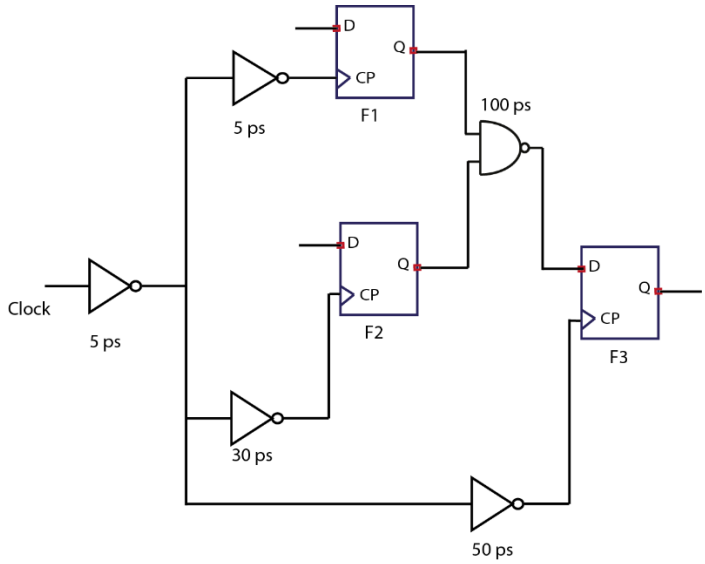
The cost of a product entirely implemented with the above software running on a general purpose microprocessor is Rs 1000/-. We can implement each function of the software using separate dedicated hardware. The runtime of any function implemented with dedicated hardware is 1/10th of that implemented in software. However, when we implement any function with dedicated hardware, the product cost increases by Rs 400/- per function, while the cost of the software remains unchanged.

a) Assume that you need to keep the product cost below Rs 2500/-. How will you perform software-hardware partitioning such that you obtain the ***minimum*** runtime meeting the cost constraint? What is the estimated cost of the system? Assume that a given application consumed 1000s when entirely implemented in software. What is the estimated runtime in your designed system? **[2+1+2 Marks]**

b) This question is independent of part (a). However, the information above part (a) is valid for this question also. Assume that a given application takes a runtime of 1000 s when entirely implemented in software. However, we need to reduce the runtime of this application below 350 s by running some functions on dedicated hardware. How will you perform software-hardware partitioning such that you obtain the ***minimum*** cost and meet the runtime constraint? What is the estimated runtime for the application in your system? What is the estimated cost of your designed system? **[2+1+2 Marks]**

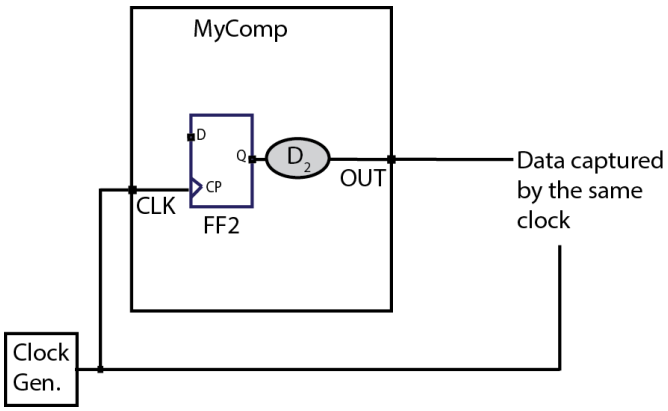
2.

(a)



A portion of a sequential synchronous circuit is shown above. The following attributes are valid for all the flip-flops F1, F2 and F3: Setup time = 30ps, Hold time = 10ps, and CP->Q Delay = 50ps. The delay of the NAND gate N1 is 100ps and the delay of inverters are shown in the figure. The frequency of the Clock is 1GHz. Ignore the delay of all the wires. Find the worst setup slack and the worst hold slack of the circuit. **Show all relevant computations.** **[4+4 Marks]**

(b)



Consider the above circuit. The period of the clock signal generated by the clock generator is 2000 ps (unit of time in library is ps). The data generated by the output port OUT of MyComp is captured externally by the same clock signal (as shown above). Additionally, the following requirements for the signal generated at the output port OUT should be satisfied:

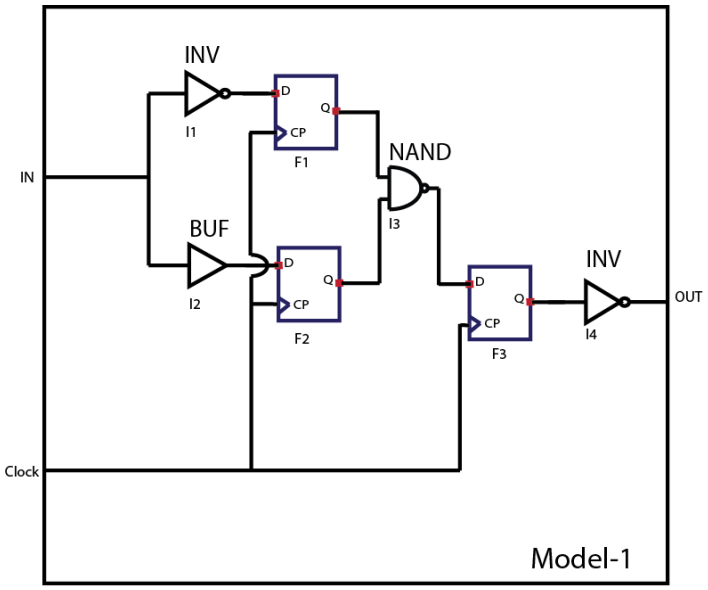
a) it should be available by 900 ps before the clock edge, and

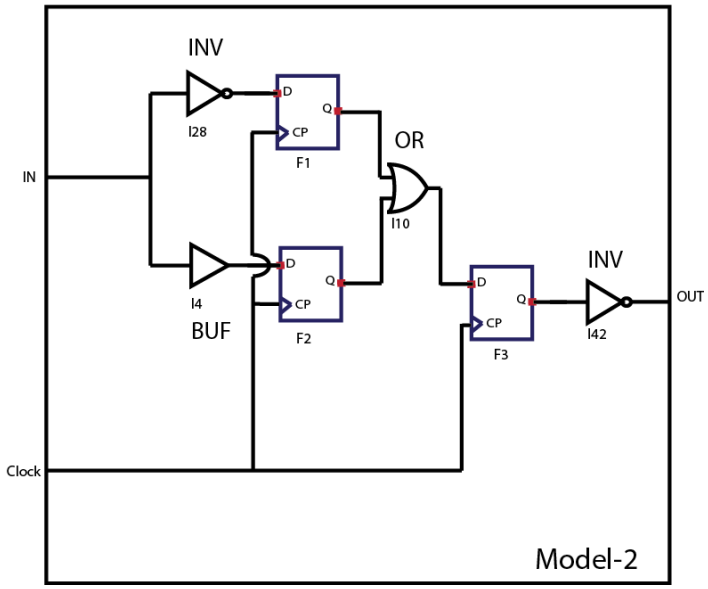
b) it should be stable for 600 ps after the clock edge.

Write all the SDC commands to model the above requirements (including that of the clock signal). **[1+2+4 Marks]**

[See the next page]

3.





Consider the netlist of Model-1 and Model-2 shown above. We perform Combinational Equivalence Checking between the above two models. The ports and registers are matched by their names.

a) Draw all the miter circuits separately that will be created for CEC for the above models. **Label the instances/ports in the miter with their corresponding names in the model [where ever possible].**
b) Which of the miter circuits drawn in (a) will fail [Put some label to miters in (a) and indicate the label here, no need to redraw]? Report all the failing patterns. Explain your answer.
c) Are the above failures reported by CEC correct (i.e. two models will give different responses) or are they false failures? Explain your answer (no marks without correct explanation).

[**4+5+6 Marks]**