VLSI Design Flow

End Semester Exam (2nd May 2021)

Time allowed: 70 minutes *Maximum Marks: 45*

Note:

I. ***All questions are compulsory.***
II. ***Marks are indicated in bold at the end of each question.***
III. ***Be crisp and precise in your answer so that you can complete the answers in the given time.***
IV. ***Use the marks allotted to each question as an indicator of how elaborate you need to answer.***
V. ***Cheating or use of unfair means will be dealt with as per institute policy.***

1. For some process, the yield is given by the following equation:

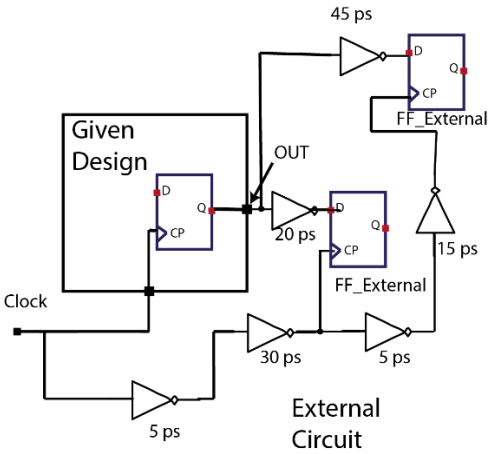
$$Yield = (1 + Ad/\alpha)^{-\alpha} \times 100\%$$

where A is the die area, d is the defect density, and α is the clustering parameter. The wafer diameter is 300 mm, and the die size is 25 mm^2. Assume that the cost of fabricating a wafer is \$100 and there is no wastage of material in creating dies out of the wafer. Assume defect density is 0.5 defect/cm^2 and the clustering parameter is 0.5.

(a) Estimate the yield and the cost per die. **[3+3 Marks]**

(b) Due to yield learning, defect density decreases to 0.1 defect/cm2. Estimate the new yield and the cost per die. **[2+2 Marks]**

2.



You are the designer of "Given Design". You need to develop a constraint file (SDC file) for the module "Given Design" (as shown above). Assume that, all relevant external circuit connected to "Given Design" is given to you (and shown above). The delay of inverters are shown in the figure itself. Take setup time of all the external flip-flops as 22 ps and that in the "Given Design" as 26 ps. Take the clock-to-q delay of all the external flip-flops as 39 ps and that in the "Given Design" as 47 ps.

You need to write the SDC command "set_output_delay" for the port OUT for **late analysis** (to meet setup-checks in the external circuit). What should be the value of output-delay that must be set at the output port OUT for **the late analysis?** Show relevant calculations for all paths. Write the SDC command "set_output_delay" for the late analysis [Take the name of clock in SDC as CLK]. Ignore early analysis and wire delays in this question. **[10 Marks]**

3. A netlist of a design is as shown below:

```
module top(A, B, C, D, E, Z1, Z2);
 input A, B, C, D, E;
 output Z1, Z2;

 nor I1(n1, A, B);
 and I2(Z1, n1, n2);
 nand I3(n2, B, C, D);
 not I4(n3, D);
 nor I5(n4, n3, E);
 and I6(Z2, n2, n4);

endmodule
```

Draw the schematic of the above netlist
Assume that the output pin of all the gates is represented as Y. Assume single stuck-at fault model in this question. Using path sensitization method, find a test vector that simultaneously detects both SA-0 at the pin I1/Y and SA-0 at the pin I3/Y. **[2+8 Marks]**

4. Assume that there are three nets in a design: N1, N2 and N3. The net N1 is connected to three cells C1, C2, and C3. The net N2 is connected to two cells C4 and C5. The net N3 is connected to five cells C6, C7, C8, C9, and C10. A placement tool has identified the following locations of cells:

C1(0,0), C2(10,4), C3(2,6),
C4(0,10), C5(0,20),
C6(0,30), C7(0,35), C8(20,35), C9(35,35), and C10(70,75).

(a) Compute the total WL of the design, based on half-perimeter wire length approximation. The unit of length is micron. **[5 Marks]**

(b) A placement tool is using a simulated annealing algorithm to find the optimum solution. The acceptance probability of the new solution is given as $e^{-(\Delta E/T)}$ when $\Delta E > 0$. Here ΔE is the increase in the total wire length due to the new solution and T = 40 micron. The placement engine perturbs the above solution by changing the location of C10 (all other cells are at the same location as mentioned above). Find ΔE and the acceptance probability if the new location of C10 is as follows:

i) C10(70,45) **[3 + 2 Marks]**
ii) C10(90,95) **[3 + 2 Marks]**