DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

MONSOON Semester | ECE 315/ ECE515: Analog CMOS Circuit Design | 2023 – 2024

Time: 60 minutes. **Quiz -2** **M.M.: 20**

Instructions: All questions carry sufficient information. **No further information will be provided during the exam.** Please answer all parts of the same question together at the same place, not here and there.

1. For the circuit in Fig. 1, $I_{in} = 100$ μA, $R_s = 1$ kΩ. Assume each transistor has W = 10 μm, L = 0.2 μm, body effect $g_{mb} = 0.2g_m$, $\mu C_{ox} = 110$ μA/V^2 and $\lambda = 0.15$ μm/V. Calculate R_{out}. **(5)**

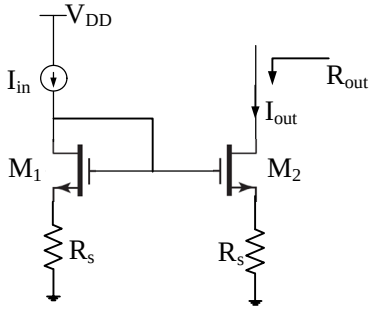

Fig. 1

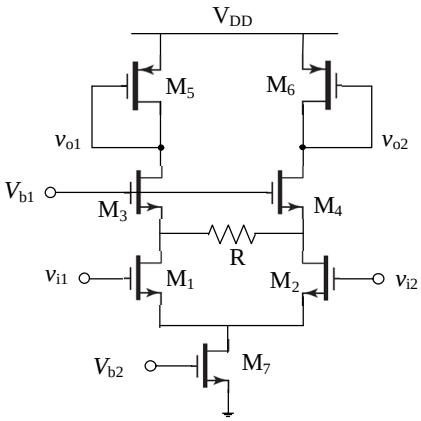

Fig. 2

2. Calculate the small signal differential gain of the circuit in Fig. 2. Assume Vb1 and Vb2 are DC bias voltages, $\lambda \neq 0$, $\gamma = 0$ and $g_m r_o >> 1$ for all MOS devices. Also, assume there is symmetry in the circuit. **(5)**

3. (a) For which single stage CMOS amplifier does Miller's approximation decrease the input capacitance when frequency response is considered?
(b) Why do we need negative feedback to amplifier circuits? Give only one reason. **(1+1+3)**
(c) Find the loop-gain of the circuit shown in Fig. 3.

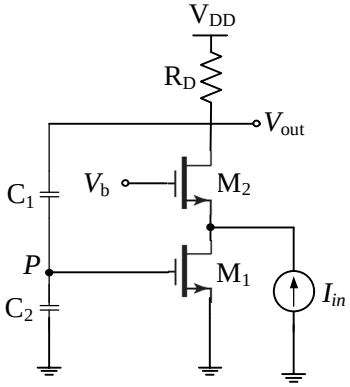

Fig. 3

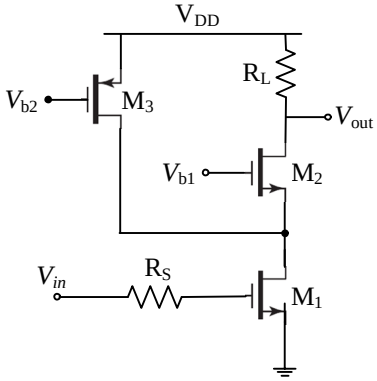

Fig. 4

4. Let us assume that the circuit in Fig. 4 is given for frequency response analysis.
(a) Identify the capacitors, which experience Miller effect, if there is any.
(b) Identify the poles by inspection. Assume $\lambda = 0$, $\gamma = 0$ for all the MOS devices. **(2+3)**