DVD Monsoon 2025: Weekly Quiz 6

Total points 10/10

Instructions

- The test will be live from **4:00 PM to 7:00 PM**.
- You must submit your response **before 7:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

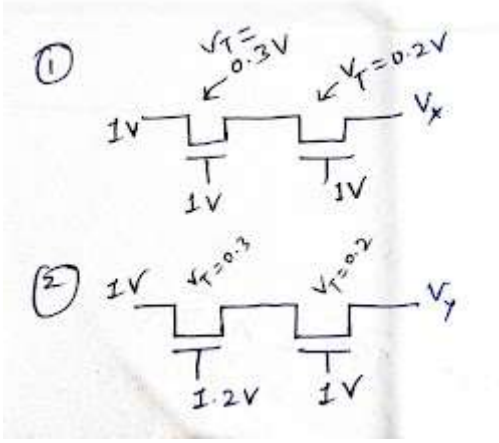
✓ Consider a PTL network using NMOS transistors. Which of the following statements are true? 1/1

- [x] NMOS transistors are used to transmit inputs, while buffers are employed to restore and generate the output. ✓
- [x] Pass transistor logic does not provide full voltage swing at the output. ✓
- [x] Level restoring transistor is used to achieve full voltage swing at the output. ✓
- [ ] When only NMOS are used, there is no static power consumption.

Feedback

In PTL, NMOS transistors are used to transmit input signals, while buffers at the output help restore full voltage levels. PTL reduces transistor count compared to conventional CMOS logic. In PTL, there is a threshold voltage drop and therefore full voltage swing in not achieved. To get a full voltage swing at the output, level restiring trasistor is used. NMOS-only PTL circuits still exhibit static power consumption due to leakage.

✓ Which one of the following is the correct value for output Vx and Vy? 2/2



- [x] Vx = 0.7V, Vy = 0.8V ✓
- [ ] Vx = 0.8V, Vy = 0.8V
- [ ] Vx = 0.5V, Vy = 0.5V
- [ ] Vx = 0.8V, Vy = 0.7V

✓ Select the correct statement regarding skewed gates. 1/1

- [ ] The non-critical MOS transistor is downsized; with skewing, the favoured transition has lower noise immunity, and the logical effort for that side decreases.
- [x] The non-critical MOS transistor is downsized; with skewing, the favoured transition gains better noise immunity, and the logical effort for that side decreases. ✓
- [ ] The non-critical MOS transistor is upsized; with skewing, the favoured transition has higher noise immunity, and the logical effort for that side increases.
- [ ] The non-critical MOS transistor is upsized; with skewing, the favoured transition gains better noise immunity, and the logical effort for that side decreases.

Feedback

In skewed gates, the non-critical MOS transistor is downsized to favor one transition. This improves the noise immunity of the favoured transition while reducing its logical effort, leading to faster switching for that side but it leads to a slower response and reduced noise margin for the non-favoured transition.

✓ Which of the following statements correctly describe the characteristics of pseudo-NMOS logic? 1/1

- [x] It offers smaller area and reduced load compared to CMOS logic. ✓
- [x] It exhibits static power dissipation due to the always-on pull-up transistor. ✓
- [ ] It provides high noise margins similar to CMOS logic.
- [x] It is suitable for area-efficient designs where moderate power loss is acceptable. ✓
- [x] A larger pull-up device improves performance but increase static power dissipation. ✓
- [ ] It is more robust than static CMOS logic.

Feedback

Pseudo-NMOS logic uses a permanently ON PMOS transistor as the pull-up device, which reduces area and load capacitance but there is continuous current flow when the pull-down network is active, leading to static power dissipation. Despite this drawback, pseudo-NMOS is often preferred in area-efficient designs where some power loss is acceptable.
A larger pull-up device improves performance by providing faster charging of the output node, but it also increases power dissipation.
It also degrades robustness when compared to static CMOS as the circuit can fail in cross-corner analysis.

✓ Which of the following statements are correct for static CMOS circuits? 1/1

- [x] The output is either connected to VDD or GND at all times. ✓
- [ ] There is huge short circuit power consumption.
- [x] There is no continuous biasing current. ✓
- [x] It has good noise margin. ✓

Feedback

Static CMOS circuits are designed such that the output is always connected to either VDD or GND through complementary transistors, resulting in no direct path between VDD and GND in steady state, eliminating no continuous biasing current. They also exhibit good noise margins due to full voltage swing levels.

✓ Which of the following statement is/are true regarding DCVSL logic? 1/1

- [x] It avoids the use of an always-on PMOS transistor, thereby reducing static leakage power. ✓
- [x] It is suitable for applications where both complementary outputs are required. ✓
- [ ] It suffers from degraded noise immunity due to its differential structure.
- [ ] It does not provide a full logic swing from VDD and GND.
- [x] It occupies more area compared to pseudo-NMOS logic due to the use of dual pull-down networks. ✓

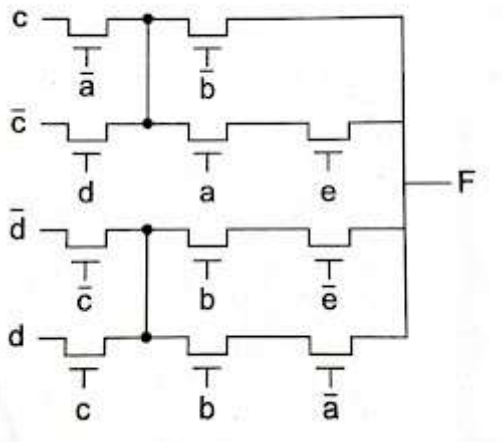
Feedback

DCVSL is more efficient than pseudo-NMOS because it avoids the always-on PMOS pull-up leading to improvements in the noise margin and significantly reducing static power. Its differential nature makes it suitable for complementary outputs and provides a full rail-to-rail swing.
The key trade-off is that DCVSL occupies more area than pseudo-NMOS because it requires dual, complementary pull-down networks.

Name *

Abhinav Maurya

✓ Which one of the following is the correct boolean expression for the below PTL circuit. 2/2



- [ ] F = (a'c +dc').(ae+b')+(cd'+c'd).(be'+a'b)....
- [x] F = (a'c +dc').(ae+b')+(c'd'+cd).(be'+a'b) ✓
- [ ] F = (ac' +d'c).(ae+b')+(c'd'+cd).(be'+a'b)
- [ ] F = (a'c +dc').(ae+b')+(c'd'+cd).(b'e+ab')

Feedback

https://drive.google.com/f...

✓ In a CMOS logic network, the designer observes that the pull-down delay of a NAND3 gate is dominated by one input path with high signal activity. Which of the following can be done to improve the design? 1/1

- [x] Inputs with higher switching activity should be connected to transistors closer to the output. ✓
- [ ] Inputs with lower switching activity should be placed closer to the output to reduce dynamic power.
- [ ] Reordering inputs changes the logical function of the circuit.
- [x] Reordering inputs can help balance delay and power. ✓

Feedback

Input reordering is atechnique used to improve delay and power in CMOS logic gates without changing their logical function.
In a series network such as a NAND gate, placing the input with higher switching activity closer to the output helps reduce the effective resistance leading to improvement in speed.