DVD Monsoon 2025:Quiz-8

Total points 9/10

Quiz Instruction

- The test will be live from **4:00 PM to 7:00 PM**.
- You must submit your response **before 7:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

Untitled Section 9 of 10 points

✓ **During flip-flop setup time characterization, it is observed that as the data transition is moved closer to the active clock edge, the Clock-to-Q delay (t(CQ)) increases significantly.** 1/1

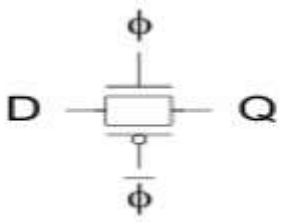
Which of the following are the primary physical reasons for this increase?

- [ ] The output load seen by the flop increases when data toggles near the clock edge.
- [ ] Setup margin affects only functional correctness; tclk→Q is independent of data arrival time.
- [x] The master latch fails to fully resolve resolve its internal node voltage before the clock transition,resulting in a weak or partially developed logic level. ✓
- [ ] The propagation delay of the combinational logic between master and slave latches increases due to added parasitic capacitances.
- [x] The internal nodes of the flip-flop enter a metastable region where regeneration takes longer to resolve to a valid 0 or 1. ✓

Feedback

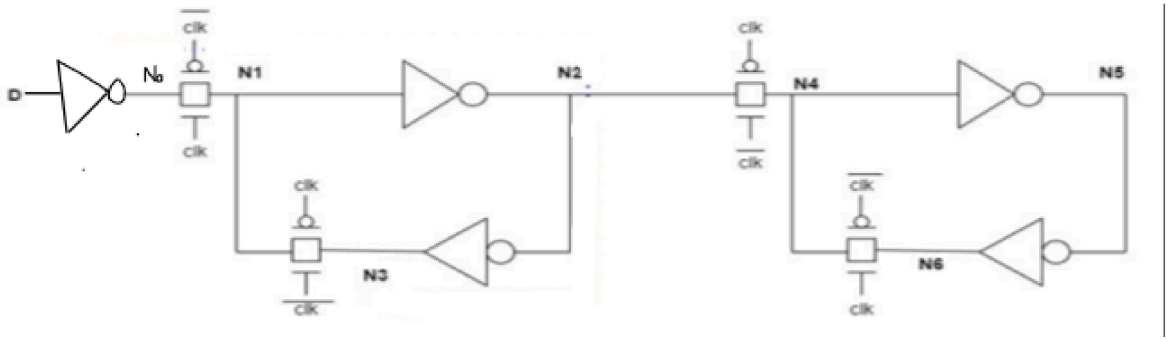
When data changes too close to the clock, the master latch's sampling node doesn't settle to a stable voltage before the clock edge. This causes delayed or weak transition to the slave.

✓ **What are the problems faced by the given latch design?** 1/1



- [ ] Vt drop
- [x] Output noise sensitivity ✓
- [x] Diffusion input ✓
- [x] Backdriving ✓

✓ In the attached flip-flop diagram, where exactly are **setup** and **hold** times defined? 1/1



- [ ] The hold time is defined at N3, Hold time violation arises because of the delay between the generation of CLK and CLKbar .
- [ ] Setup time is defined at N1
- [x] Setup time is defined at N2 ✓
- [x] The hold time is defined at No, Hold time violation arises because of the delay between the generation of CLK and CLKbar . ✓

Name *

Abhinav Maurya

✓ **Choose the correct options:** 1/1

- [x] The sampling edge for a positive level sensitive latch is falling edge of the clock ✓
- [ ] The sampling edge for a negative edge triggered flip flop is rising edge of the clock
- [x] The sampling edge for a positive edge triggered flip flop is rising edge of the clock ✓
- [ ] The sampling edge for a negative level sensitive latch is falling edge of the clock

✓ **Power-up non-determinism due to latch contention** 1/1

An FSM behaves randomly at power-on. Its state element is a level-sensitive latch implemented as either:

Fig.1: transmission gate on the input; feedback is a normal inverter.

Fig.2: transmission gate on the input; feedback is a tri-state inverter.

Which implementation is most likely causing the non-deterministic behavior?

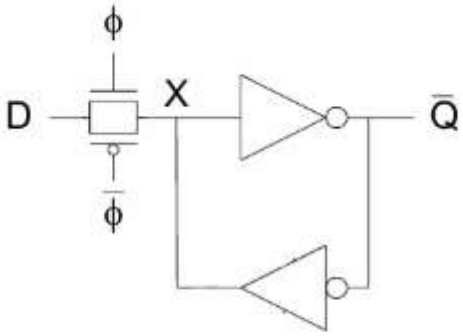


FIG.1

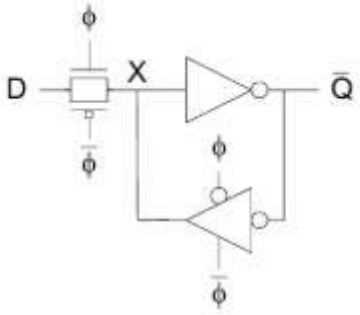


FIG.2

- [x] FIG.1 ✓
- [ ] FIG.2
- [ ] Using any of them does not make a difference
- [ ] None of the above

Feedback

In advanced nodes, mismatch can make the always-on feedback inverter stronger than the pass path, so when the TG is ON the inverter fights the input (contention/ratioed behavior), leading to random power-up state. The tri-stated keeper in Fig.2 avoids contention during transparency.

✓ **What are the Corners at which the sign-off margins in STA will be minimum? Please choose the correct option** 1/1

- [ ] Hold time-> Slow PMOS and Slow NMOS
- [x] Hold time-> Fast PMOS and Fast NMOS ✓
- [ ] Setup time-> Fast PMOS and Fast NMOS
- [x] Setup time -> Slow PMOS and Slow NMOS ✓

Feedback

Hold is a min-delay problem → worst at FF, Vmax, Tmin (fast devices, shortest paths, smallest clk-to-Q).
Setup is a max-delay problem → worst at SS, Vmin, Tmax (slow devices, longest paths).

Roll No. *

2023024

✓ **A 100-MHz design is repartitioned into four flip-flop pipeline stages. Considering non-zero sequencing overhead , what is the most realistic new maximum clock frequency?** 1/1

- [ ] 400 MHz
- [x] Between 100 MHz and 400 MHz ✓
- [ ] Above 400 MHz
- [ ] Below 100 MHz

Feedback

The correct choice is B (Between 100 MHz and 400 MHz).
When you pipeline into 4 stages, the ideal 4× speedup is limited by sequencing overhead—the extra time per stage due to the flip-flops and clocking: Tcq+ Tsetup+ clock skew/jitter.Since the overhead is > 0,
Fmax<400 MHz; with reasonably balanced stages it still exceeds 100 MHz.

✗ **In a sequential circuit, the contamination delay of the combinational logic between 2 flip-flops is very small. Which of the following statements is true?** 0/1

- [x] The circuit will operate faster, since smaller delay always improves performance ✗
- [x] The circuit may face a hold violation because of very less contamination delay ✓
- [ ] The setup time requirement will be violated
- [ ] The clock period must be increased to avoid hold violations

Correct answer

- [x] The circuit may face a hold violation because of very less contamination delay

Feedback

Reason: Answer: B
Why:
• Tiny contamination delay ⇒ data can arrive too early at the capture flop, violating the hold requirement.

Why not the other options:
• A: Smaller min delay doesn't "speed up" the circuit; performance (Fmax) depends on max delay, not min.
• C: Setup violations relate to max delay (long paths), not small min delay.
• D: Hold is independent of clock period; lengthening T doesn't fix hold—adding data-path delay (or skew) does.

✓ **A D flip-flop is characterized twice using different setup time criteria:** 2/2

Case 1: Setup time defined when Clock-to-Q delay increases by 5%

Case 2: Setup time defined when Clock-to-Q delay increases by 2%

Case 3: Setup time defined when Clock-to-Q delay increases by 10%

Assume all other parameters (cell architecture, process, voltage, and temperature) remain identical.

Which of the following statements are true?

- [x] The setup time value extracted in Case 2 will be greater than in Case 1. ✓
- [x] The STA slack for paths using Case 2 libraries will reduce compared to Case 1. ✓
- [x] Case 2 libraries inherently include more pessimism, so smaller additional STA margins are needed. ✓
- [ ] Case 1 libraries inherently include more pessimism, so smaller STA margins are needed
- [x] Characterizing setup at a 10% Tcq increase trades reliability for performance ✓

Feedback

A - True

Using a 2% threshold means data must settle farther from the clock edge larger setup time.

B True

Larger setup time increases total data path delay term (tCQ + tpd + tsetup) less slack.
C-True

Since setup is defined more conservatively, library itself carries extra safety less additional STA margin (like OCV derate) needed.

E- False
Extracted Tsetup becomes smaller, data can be closer to the clock and still be considered safe. But you are sitting closer to the metastability onset, small PVT, noise crosstalk or other variations can push the flip-flops into failure