Digital VLSI Design (ECE314/ECE514)
Mid Semester Exam (8th October 2024)

Duration : 1 hour   Maximum Marks : 30
**

Name   :
Roll Number :

Instructions:

1. **This question paper is of 30 marks in total.**
2. **Students registered for the ECE314 course are required to attempt questions amounting to 25 marks. Any additional questions attempted beyond 25 marks will be treated as bonus.**
3. **Students registered for the ECE514 course must attempt the entire paper of 30 marks.**

1. Answer the following questions: **[6 marks]**
   a. During fabrication, both high K and low K dielectric oxides are used. Where is it desired to use which dielectric and why? [CO1]   **[2 marks]**

   b. A mobile processor core is to be designed. Battery life is a key concern. So the dynamic power has to be kept low, but users also demand high performance for gaming and video streaming. How would you balance these two conflicting priorities? [CO3]   **[1 mark]**

   c. What is done to prevent latch-up? [CO1]   **[1 mark]**

   d. In dynamic voltage frequency scaling, for operating in high performance, do we first increase the voltage and then increase the frequency or we first increase the frequency and then increase the voltage ? Support your answer with reasoning. [CO3]   **[2 marks]**

2. In the below figure, given is a stick diagram of a complex logic gate. Answer the following questions with respect to this stick diagram.[CO2]   [8 marks]
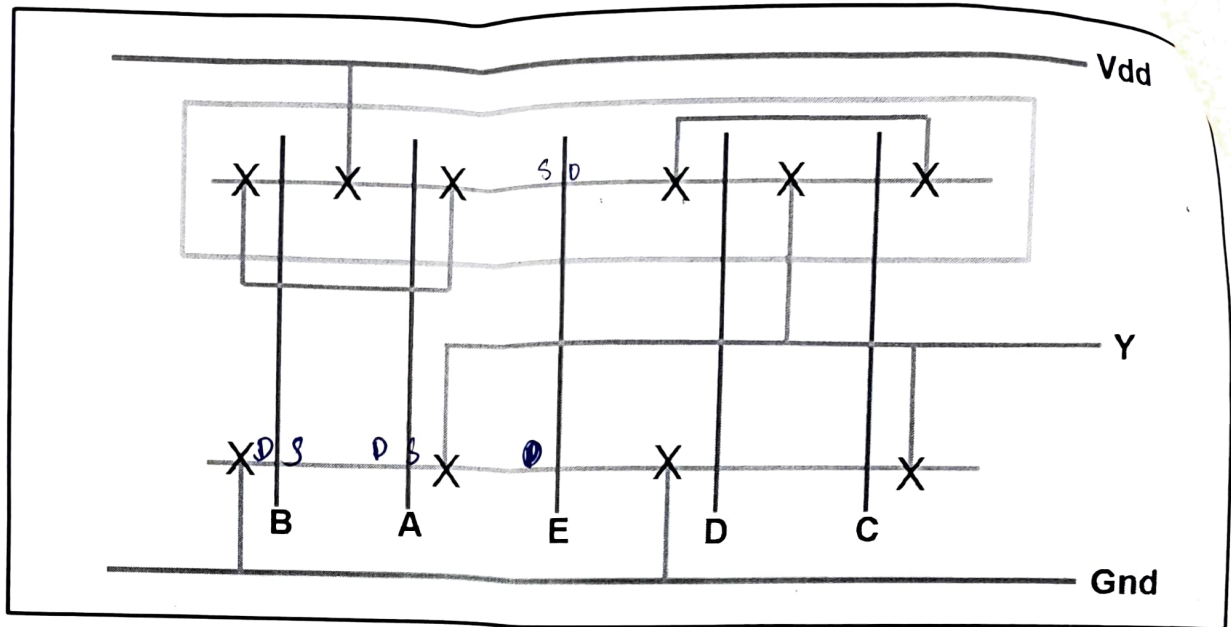
a. Write the boolean expression for this stick diagram.   **[1 mark]**
b. Draw CMOS schematic for the above derived boolean expression and size the transistors with respect to unit inverter.   **[2 marks]**
c. Strength of this complex logic gate is increased to 3 times the strength of the unit inverter. What will be the logical effort with respect to input B and input E.   **[1 mark]**
d. Based on the schematic drawn in part b, what will be the input stimuli to calculate rise and fall propagation and contamination delay ? Clearly state any assumptions.   **[4 marks]**

3. For a CMOS process which of the following might be less than target, more than target or remains at target in different process lots: [CO2]   **[3 marks]**

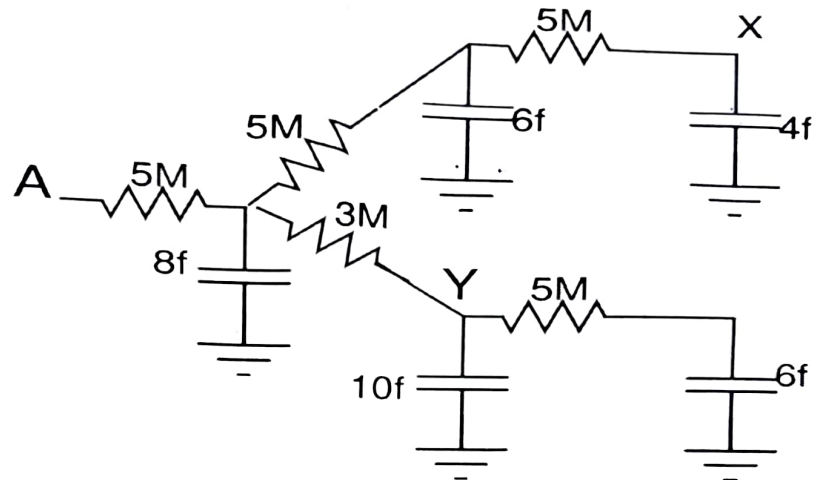| Corner/Parameter	tox	Width	Length
FF			
SS			
TT			
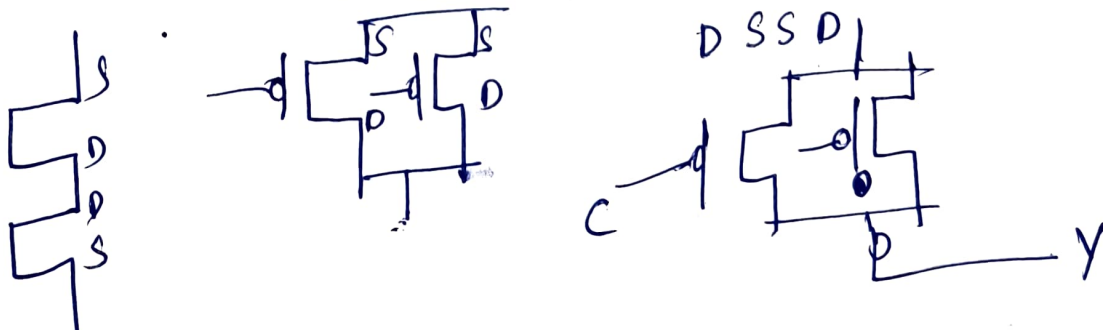
4. Calculate the Elmore Delay with respect to point A in the given circuit for: [CO1,CO2]
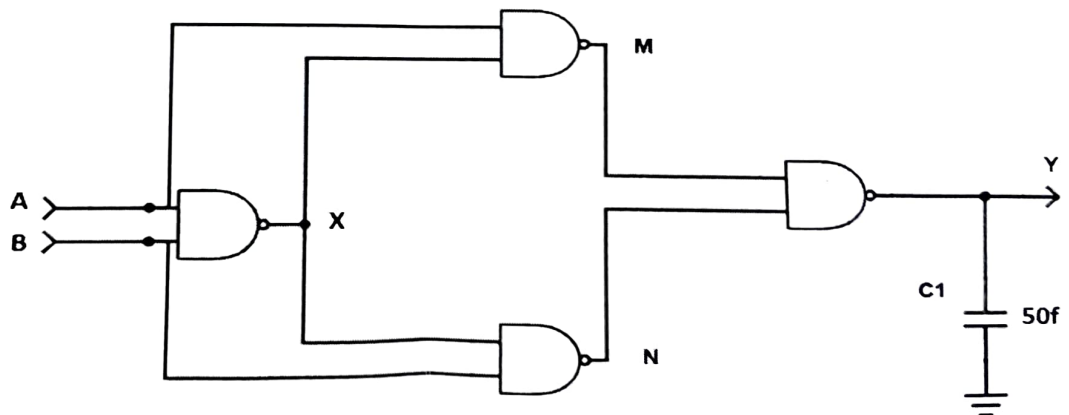   a. Point X
   b. Point Y

   [2 marks]
   [2 marks]

5. Given below is a NAND gate implementation of XOR gate. Answer the following questions. [CO3]

   [4 marks]

   a. Given that occurrence of logic 0 and logic 1 at input A and B is equiprobable, then what is the activity factor at 'Y' node. [2 marks]

   b. If the circuit is operated at VDD = 1.2V and clock frequency of 1GHz then, what is the dynamic power dissipation at the 'Y' node ? [2 marks]

6. A chip is produced using 90nm technology and occupies 100mm² of area with a yield of 50%. Each chip is sold for Rs. 200/- at a profit of Rs. 25/- per die. Now the company decided to design the same product in 65nm technology node, reducing the area by 20%. Answer the following questions. [CO1]   **[2 marks]**

   a. What will be the new expected yield ?   **[1 mark]**
   b. Company decided to sell the product at the same price. What will be the new profit per die?   **[1 mark]**

7. In the gate level schematic given below, find the normalized path delay from input A to Z via I1, I2, I3. Also find the values of drive strengths X and Y of gates I2 and I3 respectively. [CO2]   **[3 Marks]**