VLSI Design Flow

Mid Semester Exam (27th September 2025)

Time allowed: 1 hour *Maximum Marks: 30*

Note:

I. ***There are 5 questions. All questions are compulsory.***
II. ***Marks are indicated in bold at the end of each question.***
III. ***Be crisp and precise in your answer so that you can complete the answers in 1 hour.***
IV. ***Cheating or use of unfair means will be dealt with as per institute policy.***

1.

a. With respect to photolithography, answer the following?
   i. Name the material that changes its property when exposed to light and is applied to the wafer to capture the pattern on the mask.
   ii. Name the task that removes material from the layer that needs to be patterned after exposure and development. **[0.5X2=1 Mark]**

b. On a silicon wafer, 400 pieces of a given die are fabricated. The yield of fabrication is 75%. How many silicon wafers need to be processed by the foundry if it needs to deliver 3,00,000 good dies to a customer? **[2 Marks]**

c. With respect to resolution enhancement techniques, answer the following:
   i. Name the technique that modifies the pattern in the given layout by adding hammerheads, serifs, etc., such that effects of diffraction can be reduced.
   ii. Name the technique that decomposes closely-spaced features to multiple layouts such that they can be exposed and patterned separately.

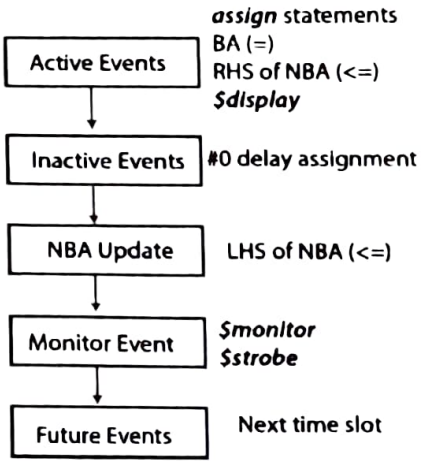
[0.5X2=1 Mark]

d. Name the VLSI design flow task that performs the following activity (just give the names of each task, no description needed):
   i. Converts an algorithm written in high-level language (such as C, C++) to RTL
   ii. Divides the part of an algorithm that will be implemented using dedicated hardware and the part of that algorithm that runs as software on a general-purpose processor.
   iii. Converts a generic netlist to a netlist implemented using standard cells present in the given technology library
   iv. Determines the power delivery network for a design on the layout
   v. Determines the layout of data path signal nets on the layout during physical design
   vi. Makes controlled changes to a design after following the due engineering process at the last moment before signoff. **[0.5X6=3 Marks]**

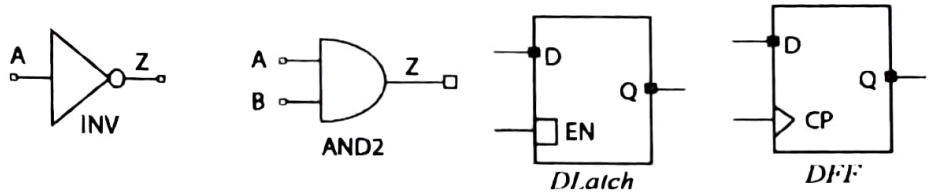
e. What will the simulation result be for the Verilog code shown on the next page? The stratified Verilog event queue is shown for your convenience. Write only the expected output. No explanation is needed. **[2 Marks]**

Recheck

```
module top();
  reg a, b;

  initial begin
    $monitor("a=%b b=%b", a, b);
  end

  initial begin
    a = 0;
    b <= 1;
  end

endmodule
```



2. Assume that a library consists of an inverter, a two-input AND gate, a D Latch and a D flip-flop with the respective cell names being INV, AND2, DLatch, and DFF, as shown in the figure below:



Draw the schematic of the expected synthesized netlist for each module shown below. Label the circuit elements appropriately because labels carry marks.

a)

```
module top(a, b, clk, out);
input a, b, clk; output out;
reg q1, q2, out;

always @ (posedge clk) q1 <= a;
always @ (posedge clk) q2 <= b;
always @ (posedge clk) out <= q1 & q2;
endmodule
```

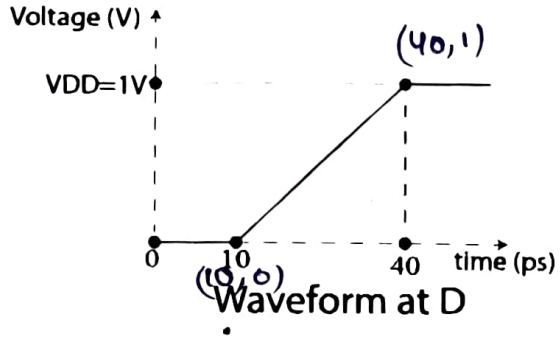
[4 Marks]

b)

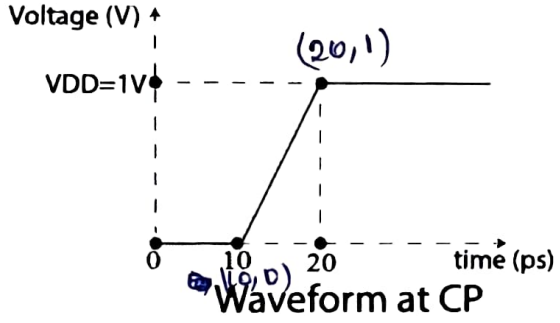
```
module top(a, b, sig, out);
input a, b, sig; output out;
reg t;

always @ *
begin
  if (sig) t <= a;
end
always @ *
 out = t & b;

endmodule
```

[3 Marks]

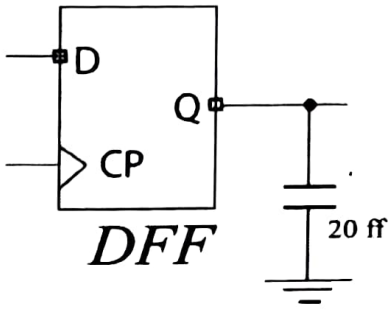
3. Consider a flip-flop shown in the following figure. It receives signals at the D and CP (clock) pins with waveforms, as shown in the figure. It drives a load of 20 ff at the output. The supply voltage is 1 V.



Waveform at D



Waveform at CP



The library is characterized using a slew threshold of 10% to 90%. The setup-time 2D table for DFF in the library is shown below.

D-pin slew → CP-pin slew ↓	2 ps	4 ps	8 ps	16 ps	24 ps
2 ps	5	10	16	20	28
4 ps	6	12	18	24	36
8 ps	9	15	27	39	45
16 ps	13	26	47	63	80

The clock-to-Q delay 2D table for DFF in the library is shown below.

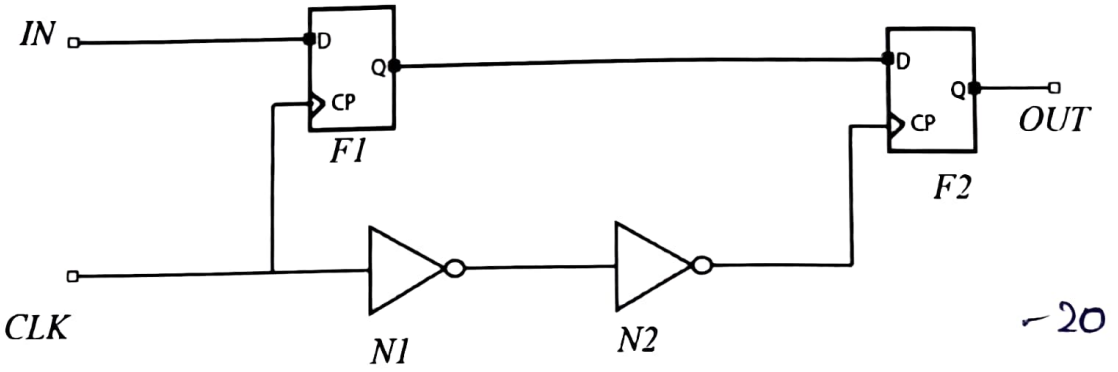
CP-pin slew → Load ↓	2 ps	4 ps	8 ps	16 ps	32 ps
10 ff	10	20	28	40	52
20 ff	14	26	35	70	100
30 ff	22	44	68	86	110
40 ff	32	48	76	94	136

Compute the following:

a. Setup time of the flip-flop
b. Clock-to-Q delay of the flip-flop

[3+2 Marks]

4. Consider the synchronous circuit shown below.

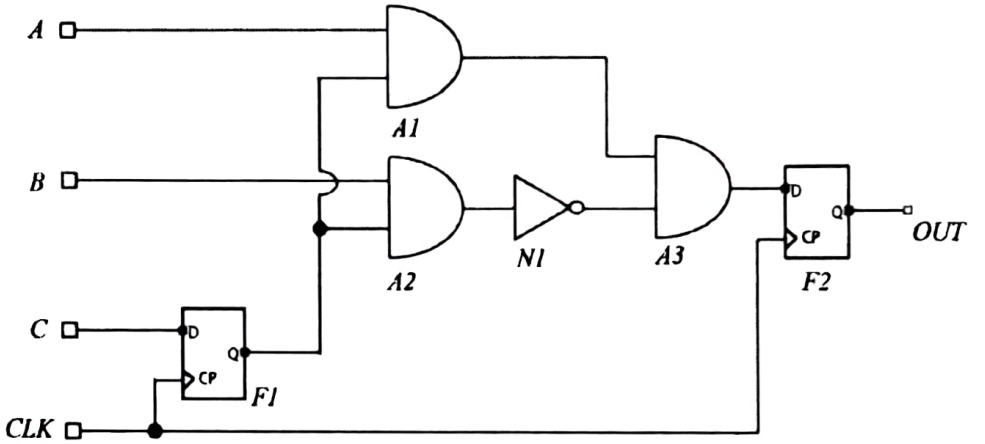


-20

Assume that the clock period is 1000 ps. Assume the wire delay is zero.
Assume that for both flip-flops: setup time = 40 ps, hold time = 10 ps, clock to Q delay = 30 ps
Assume that the delay of each inverter is 20 ps.
Calculate the hold or early slack of the path in which F2 captures data launched by the flip-flop F1 (show calculation of required time, arrival time, and slack since each quantity carries marks).

[3 Marks]

5. Consider the synchronous circuit shown below.



Assume that the clock period is 1000 ps. Assume that the arrival time of the clock signal at the clock pin of all the flip-flops is 0 ps. Assume the wire delay is zero.
Assume that:
For the flip-flop F1: setup time = 30 ps, hold time = 20 ps, clock to Q delay = 40 ps
For the flip-flop F2: setup time = 35 ps, hold time = 25 ps, clock to Q delay = 45 ps
For the inverter N1: delay = 50 ps
For each AND gate: delay = 100 ps
Determine the following:

a. The worst-case setup or late slack for the path in which F2 captures data launched by F1 (show calculation of required time, arrival time, and slack since each quantity carries marks). 675 **[3 Marks]**

b. The worst-case hold or early slack for the path in which F2 captures data launched by F1 (show calculation of required time, arrival time, and slack since each quantity carries marks). 215 **[3 Marks]**