Digital VLSI Design (ECE-314/514)

End-Sem Exam Rubrics

3rd December 2025 [Time: 2:30-3:30 PM]

Maximum Marks: 30 Marks Duration: 60 minutes

Name _____ Roll No._____

Instructions

1. This is a closed-book exam
2. Use of **calculators is permitted**. The use of mobile phones is strictly prohibited.
3. There are a total of 6 questions in the paper, and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following project-based questions in 50-100 words. **[CO1,CO2,CO3,CO4,CO5]**

a) Why is it important to distribute I/O pins across the layout rather than placing them along the same track while making layouts? Give two reasons. **[1 mark]**

A. It is important to distribute I/O pins across the layout instead of placing them along the same track to ensure efficient and congestion-free routing. When multiple I/O pins are aligned on a single track, several issues can arise:

1. **Routing Congestion:** Concentrating pins in one region forces many nets to pass through the same narrow area, creating local congestion and increasing the risk of routing failures.
2. **Excessive Use of Upper Metal Layers:** To bypass the congested region, routers may be forced to use higher metal layers unnecessarily, increasing design complexity and blocking higher metal tracks.
3. **Increased Parasitics:** Longer and more complex routing paths can introduce additional resistance and capacitance, affecting signal integrity and potentially degrading timing performance.
4. **Improved Placement Flexibility:** Scattered I/O pins reduce detours and enable more optimal routing paths.

By distributing I/O pins around the periphery or appropriate layout regions, we support smoother routing, improved performance, reduced congestion, and a more robust and manufacturable design.

b) What are the worst-case PVTs for characterising leakage of standard cells? **[1 mark]**

A. The worst-case PVT conditions for characterising leakage in standard cells are:

Process: FF (Fast–Fast)

Voltage: High

Temperature: High

Justification:

1. **Fast–Fast (FF) Process Corner:**
   In the FF corner, transistors exhibit lower threshold voltages (Vt). A lower Vt significantly

increases subthreshold leakage since leakage current grows exponentially as Vt decreases. Thus, FF devices leak more compared to typical or slow devices.

2. **High Supply Voltage:**
   Higher supply voltage increases the electric field across the device, enhancing subthreshold, gate, and junction leakage components. Even when the transistor is off, a higher voltage difference promotes more charge carrier activity, increasing leakage current.
3. **High Temperature:**
   Leakage mechanisms such as subthreshold leakage and junction leakage rise sharply with temperature. Higher temperature increases intrinsic carrier concentration and provides carriers with more thermal energy, causing exponentially higher leakage currents.

c) After post-layout simulations, we observe a significant degradation in delay compared to pre-layout estimates. What could be the two possible reasons for this and what corrective actions should be taken?

[1 mark]

A. A significant increase in delay during post-layout simulations typically arises from layout-induced parasitics that were not present or not fully accounted for during pre-layout analysis. Key reasons include:

1. **Excessive Parasitic Capacitance:** Large metal-to-metal overlap, long interconnects, or closely spaced routing can introduce high coupling capacitances. Increased capacitance directly increases RC delay on nets.
2. **Insufficient Diffusion (Active) Sharing:** Lack of source/drain diffusion sharing between transistors increases the number of diffusion regions, leading to higher junction capacitances and larger parasitics.
3. **Use of Poly Routing:** Polysilicon has significantly higher resistance compared to metal layers. Any signal routed in poly experiences high RC delay, degrading timing.
4. **Unoptimized Transistor Placement:** Longer gate connections, poorly aligned devices, or unnecessary spacing can increase wire length and add delay.
5. **Suboptimal Cell or Layout Structure:** Irregular device sizing, asymmetric structures or routing can worsen performance.

To mitigate the delay degradation, the following steps should be taken:

1. **Optimize Layout to Reduce Parasitics:** Minimize metal overlaps, avoid unnecessary coupling, and use higher metal layers for long or critical nets.
2. **Improve Diffusion Sharing:** Merge adjacent transistors where logical connectivity allows, reducing junction capacitance and improving speed.
3. **Avoid Poly Routing:** Restrict poly usage to transistor gates only; route signals using low-resistance metal layers.
4. **Re-evaluate Device Placement and Sizing:** Adjust device orientation, spacing, or sizing to achieve more compact and symmetric layouts.

d) What are the two advantages of using multi-bit latches or flip-flops? Additionally, why is it a bad idea to route the clock signal using polysilicon? Give two reasons. **[2 marks]**

A. Advantages of using Multi-bit latches or flip-flops is they reduce the load on the clock network and improve overall power and area efficiency:

1. **Reduced Clock Capacitance:** Multi-bit flops share common internal clock buffers and clock drivers. This significantly reduces the total clock pin capacitance compared to using several single-bit flops, lowering clock power.
2. **Lower Dynamic Power Consumption:** Since dynamic power is proportional to capacitive load, reducing clock capacitance leads directly to reduced dynamic power on the clock tree.
3. **Fewer Clock Buffers Required:** A smaller effective clock load means fewer buffers are needed in the clock tree, improving power and sometimes clock skew margins.
4. **Area Efficiency:** Multi-bit cells often occupy less area than equivalent sets of single-bit cells due to shared diffusion, clock drivers, and layout compaction.
5. **Reduced Routing Congestion:** With fewer individual clock pins and a more compact footprint, routing complexity is reduced, especially in dense regions.

Routing the clock signal with polysilicon should be strictly avoided due to its detrimental impact on performance:

1. **High Resistance:** Polysilicon has much higher resistance compared to metal layers. Routing clock through poly introduces large RC delays, severely degrading clock edge quality and timing.
2. **Increased Capacitance:** Poly routing increases coupling and parasitic capacitance, further worsening RC delay and leading to slower clock transitions.
3. **Higher Power Consumption:** Due to higher capacitive load and slower transitions, the clock network may consume more power to drive the same load.
4. **Greater Susceptibility to Noise and Variations:** High-R poly lines are more sensitive to process variations and noise, making clock distribution less robust.

Thus, we end up losing the advantages of using multi-bit latches or flip-flops if we route the clock with polysilicon.

e) How can setup and hold margins change post-layout, and how can these changes affect the overall design? **[2 marks]**

A. Setup and hold margins can change significantly post-layout because the actual routed design introduces real interconnect parasitic resistances, capacitances, and coupling that are not present in pre-layout timing estimates. These parasitics alter the real signal propagation delays and clock arrival times, leading to updates in both setup and hold margins.

Setup and Hold Margins Change Post-Layout due to:

1. **Interconnect Delays Increase or Decrease:** Routing introduces wire resistance and capacitance, which may slow down or, in some cases, speed up signal paths. This directly affects data arrival times at registers.

2. **Coupling and Crosstalk Effects:** Neighboring switching nets induce coupling capacitances that can either accelerate or delay transitions, modifying setup/hold margins.
3. **Clock Skew Changes After CTS:** Real clock tree synthesis introduces skew between launch and capture registers, which can improve or degrade setup and hold slack.

Impact on the Design:

1. **Previously Failing Paths May Be Fixed:** If routing shortens path delays or skew becomes favorable, setup or hold violations present in pre-layout may disappear.
2. **New Violations May Be Introduced:** Increased RC parasitics, poor routing, or adverse skew may create fresh setup or hold violations that were not visible before layout.
3. **Potential Timing Closure Challenges:** Significant slack degradation may require inserting buffers, resizing cells, re-routing paths, or adjusting the clock network.
4. **Risk to Functionality and Silicon Reliability:** Unresolved setup violations can cause incorrect data capture, while hold violations can lead to metastability, both resulting in malfunctioning silicon.

f) What could be two disadvantages of using an excessive number of contacts in a layout? **[1 mark]**

A. Using too many contacts in a layout is generally discouraged because it introduces several drawbacks that can negatively impact performance, area, and manufacturability:

1. **Increased Parasitic Capacitance:** Each contact contributes parasitic capacitance to the connected node. Excess contacts therefore increase total capacitance, leading to higher RC delays and degraded timing.
2. **Higher Power Consumption:** Greater capacitance results in increased dynamic power consumption since dynamic power is proportional to capacitive load.
3. **Larger Area Usage:** Contacts occupy physical space. Using more contacts than necessary can enlarge the layout footprint and reduce layout density.
4. **Routing Blockage:** Excess contacts create obstacles for metal routing, potentially increasing congestion and forcing detours that increase wire length and parasitics.

In practice, contacts should be used optimally enough to ensure good connectivity and current handling, but not so many that they introduce unnecessary parasitics or layout complications.

g) Do parasitic RCs extracted post-layout impact leakage when compared to pre-layout estimates? Justify your answer by giving two reasons. **[1 mark]**

A. **No**, Parasitic resistances (R) and capacitances (C) extracted after layout don't impact leakage. They primarily affect dynamic behavior, such as signal propagation delay, transition times, and power consumed during switching. Leakage power, however, is dominated by device-level characteristics, not interconnect parasitics.

Reasons parasitic RCs do not affect leakage:

1. **Leakage is a device property, not a routing property:** Leakage current, subthreshold leakage, gate leakage, junction leakage is determined by transistor parameters such as threshold voltage

(Vt), channel length, oxide thickness, and temperature. Interconnect RCs do not alter these device characteristics.

2. **RCs only influence dynamic, not static power:** Capacitance affects dynamic power ($P = C \cdot V^2 \cdot f$). Resistance affects signal delays (RC timing). Neither contributes to static current flow when the circuit is not switching.
3. **Leakage depends on node voltages, not wire parasitics:** Leakage is driven by the steady-state voltage across a transistor when it is off. Parasitic RCs do not significantly change these DC node voltages.

h) Why is it recommended that I/O pins in standard cell layouts be designed to span across multiple tracks? Give two reasons. **[1mark]**

A. It is recommended that I/O pins span across two M3 tracks in standard cell layouts to improve routing flexibility and ensure better connectivity during top-level routing. By covering two adjacent M3 tracks, the router has multiple access points to enter the pin, making it easier to route signals efficiently without congestion. This approach provides:

1. **Greater Routing Flexibility:** Having two accessible M3 tracks allows the router to approach the pin from different directions, reducing routing detours.
2. **Lower Risk of Pin Access Failures:** If one track becomes blocked due to neighbouring routing or congestion, the alternate track still provides access.
3. **Improved Routability in Dense Regions:** Multi-track access points help avoid routing bottlenecks within highly congested standard cell rows.

Overall, ensuring I/O pins span two M3 tracks supports more robust routing, reduces congestion, and improves timing closure at the chip level.

i) While designing a transmission-gate–based multiplexer, buffers are often inserted between successive transmission gate stages. What is the need for using these buffers? **[1 mark]**

A. As a signal passes through multiple transmission gates, it suffers voltage degradation and increased delay due to the finite resistance and parasitic capacitances of each transmission gate. Buffers are placed between transmission-gate chains to restore signal strength, restore noise margins, and provide full voltage swing.

Q2) Consider a sequential circuit:

(a) When the clock frequency is increased, the circuit fails to operate correctly. What could be the reason for this behaviour, and what can be done to fix it so that the circuit works reliably? **[1.5 marks, CO4]**

(b) If the failure is independent of the clock frequency, what timing issue could be causing the failure, and how can it be fixed? **[1.5 marks, CO4]**

A. (a) The circuit fails because the setup time requirement is violated. As the clock period decreases, data no longer reaches the destination flip-flop before the next clock edge.

To fix this, the critical path delay must be reduced. This can be done by optimizing or resizing logic on the critical path, adding pipeline stages so that setup timing is met.

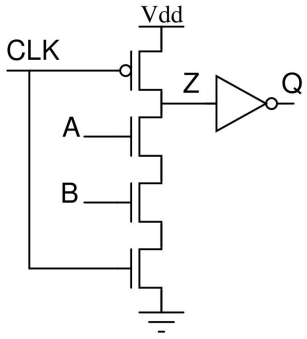
(b) If the failure does not depend on the clock frequency, the cause is a hold-time violation. Hold violations occur when data propagates too quickly to the next flip-flop, violating the hold requirement. To fix it, the minimum delay of the path must be increased by adding delay buffers, using slower combinational elements, or adjusting clock skew to ensure that the capturing flip-flop sees a stable input for the required hold time.

Q3) What is clock gating and why is it used? **[2 marks, CO4]**

(a) Clock gating is a low-power design technique in which the clock signal to a flip-flop, register, or functional block is selectively turned off when that part of the circuit is not required to operate. This is done using gating logic (such as AND/OR gates or integrated clock-gating cells) that enables or disables the clock based on control signals.

Clock gating is used to reduce dynamic power consumption, since the clock network switches every cycle and is one of the largest sources of power in digital circuits. By preventing unnecessary clock transitions, clock gating decreases switching activity, lowers overall power usage, and improves energy efficiency without affecting functional correctness.

Q4) A dynamic Domino AND gate is precharged such that inputs A=B=0 and the intermediate dynamic node Z is precharged to VDD. During the evaluation phase, input A rises to '1' while B remains '0'. Ideally, the output should remain unchanged; however, it is observed that the voltage of node Z drops significantly, which can sometimes cause a logic error. **[2 marks, CO3]**

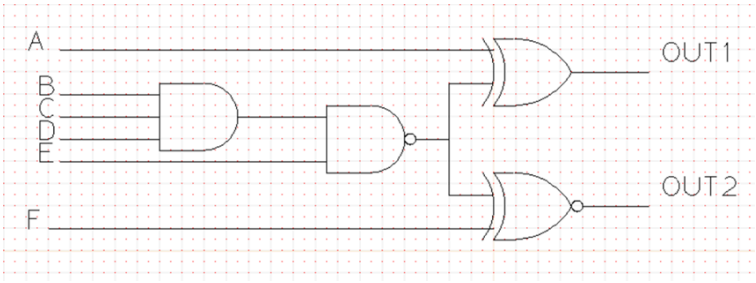


(a) What is this phenomenon called? Briefly explain why the voltage at node Z drops.
(b) What can be done to correct this?
(a) Phenomenon: Charge Sharing.
When input A rises, the transistor connected to A turns ON, connecting the precharged dynamic node Z to the internal diffusion capacitance between the two series NMOS transistors. Charge from Z spreads to this internal node, lowering the voltage at Z.
(b) Adding a keeper transistor to refresh the dynamic node and maintain its logic.

Q5)Consider the figure below and answer the following:

(a) Calculate the activity factor of the output node OUT1 of the circuit given below. It is given that the probability of an input being high is 0.5 for all inputs. **[2 marks, CO3]**

(b) The circuit shown above sees a total load capacitance of 10fF and is operated at 1V. The time period of the system clock is 1ns. Find the switching power of the circuit. **[1 Mark,CO3]**



(a)Let X be the output of the 3-input AND gate (inputs B, C, D):

$$P(X=1) = P(B) \cdot P(C) \cdot P(D) = 0.5 \cdot 0.5 \cdot 0.5 = 0.125$$

Let Y be the output of the NAND gate (inputs X, E):

$$P(Y=0) = P(X=1) \cdot P(E=1) = 0.125 \cdot 0.5 = 0.0625$$

$$P(Y=1) = 1 - P(Y=0) = 1 - 0.0625 = 0.9375$$

Output Node OUT1 (XOR Gate)

The inputs to the XOR gate are A and Y .

$$P(\text{OUT1}=1) = P(A=1)P(Y=0) + P(A=0)P(Y=1)$$

$$P(\text{OUT1}=1) = (0.5 \cdot 0.0625) + (0.5 \cdot 0.9375)$$

$$P(\text{OUT1}=1) = 0.5 \cdot (0.0625 + 0.9375) = 0.5 \cdot 1 = 0.5$$

Since $P(\text{OUT1}=1) = 0.5$, then $P(\text{OUT1}=0) = 0.5$.

Calculate Activity Factor (α)

$$\alpha = P(\text{node}=0) \cdot P(\text{node}=1)$$

$$\alpha_{\text{OUT1}} = 0.5 \cdot 0.5 = 0.25$$

(b) $Pswitching = \alpha \cdot Cload \cdot V2 \cdot f$

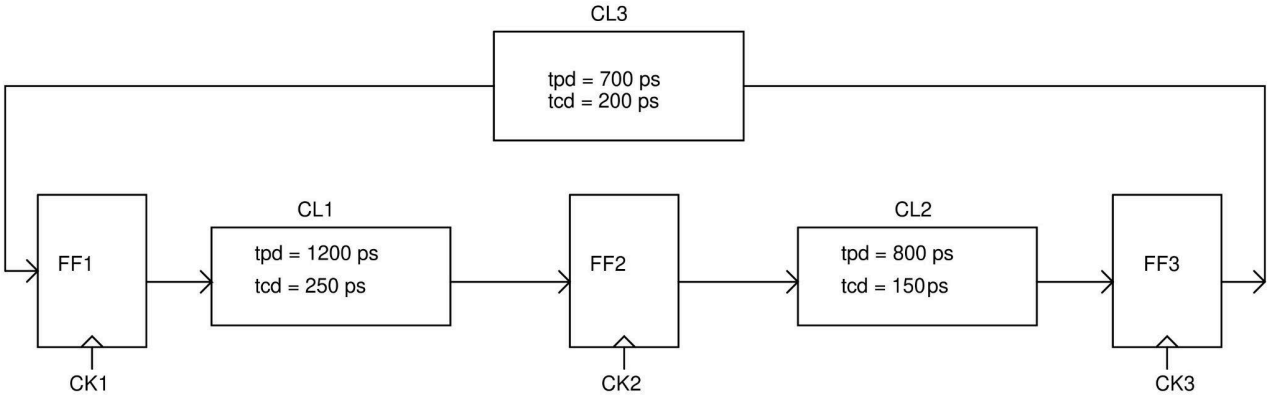
$P_{switching} = 0.25 \cdot (10 \times 10^{-15}) \cdot (1)^2 \cdot (1 \times 10^9)$

$Pswitching = 2.5 \times 10{-}6\ \text{W}$

Q6) In the figure below, assume the following parameters of the FFs: tC2Q = 150ps, tsetup = 50ps, and thold = 100ps. The clock has no jitter.

(a) The propagation delay (tpd) and the contamination delay (tcd) of each module are annotated. What is the minimum clock period (T) if there is no clock skew? **[2 marks,CO4]**

(b) If the skew between CK1 and CK2 is -100ps, and the skew between CK1 and CK3 is 50ps, then what is the minimum clock period? **[2 marks, CO4]**



Ans.

(a) $T_{max} > t_{c2q} + \max(t_{pd} \text{ of } CL_1, t_{pd} \text{ of } CL_2, t_{pd} \text{ of } CL_3) + t_{setup}$

$= 150 + t_{pd} \text{ of } CL_1 + 50$

$= 150 + 1200 + 50$

$T_{max} = 1400\text{ps}$

(b) Stage 1 (FF_1, CL_1, FF_2) is the critical path.

$T_{max} > t_{c2q} + \max(t_{pd} \text{ of } CL_1, CL_2, CL_3) + t_{setup} - t_{skew}$

$T_{max} > 150 + 1200 + 50 - (-100)$

$T_{max} > 1500\text{ps}$

Minimum clock period = 1500 ps