Digital VLSI Design (ECE-314/514)

Mid-Sem Exam | **Set-C**

22nd September 2025 [Time: 3:00-4:00 PM]

Maximum Marks: 25 Marks | Duration: 60 minutes

Name _____ | Roll No. _____

Instructions

1. This is a closed-book exam
2. Use of **calculators is permitted**. Use of mobile phones is strictly not allowed.
3. There are multiple sets of question papers. **Write your set on your answer sheet.**
3. There are a total of 7 questions in the paper, and some of these questions have sub-parts.
4. Marks of each question (and sub-part) are written in front of each question.
5. Write all assumptions, if any, clearly. Only reasonable assumptions will be considered if any ambiguity is found in the question.

Q1) Answer the following questions. **(CO1, 8 marks)**

a) What is the phenomenon in which CMOS chips tend to develop a low resistance path between VDD and GND, causing catastrophic meltdown? Describe briefly this phenomenon - how and when this phenomenon is triggered? How can this be prevented? **(2 marks)**

b) Why is Tungsten (W) preferred over Copper (Cu) for making contacts in CMOS technology? **(1 mark)**

c) Explain the effect of the β ratio on noise margins and propagation delays in a CMOS inverter. **(2 marks)**

d) Draw the C–V characteristics plot of a PMOS transistor with proper labelling. If positive charges are implanted in the oxide layer, redraw the curve showing in which direction it shifts? **(2 marks)**

e) Explain the effect of a change in temperature on subthreshold current and ON current. **(1 mark)**

Q2) Complete the table below with the worst-case PVT conditions for different FOMs. **(CO1, 1.5 marks)**

Figure of Merit (FoM)	Process	Voltage	Temperature
Power		High	
Leakage			High
Contamination Delay	FF		

Q3) Nikhil is a design engineer at company X. While performing the verification process of a digital circuit at low voltage and high temperature, the delay specifications are met. He expects the specification to be met at low voltage and low temperature, but it fails. Explain the reason behind this? **(CO3, 1 mark)**

Q4) For the Boolean expression Y = ((A+B).C+D)', draw its Static CMOS logic schematic, size the transistors with respect to a unit inverter **(CO1, 1 mark)** and draw the stick diagram **(CO1, 2 marks),** considering as much sharing of S/D as possible and do the following: **(9 marks)**

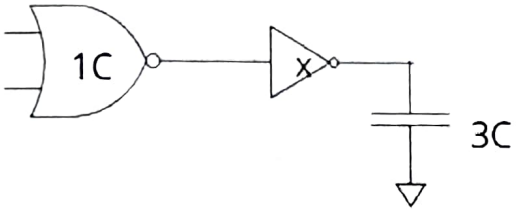
a) Indicate the capacitances at each node in the schematic while also considering an additional load of 12C at the output. **(CO1, 1 mark)**

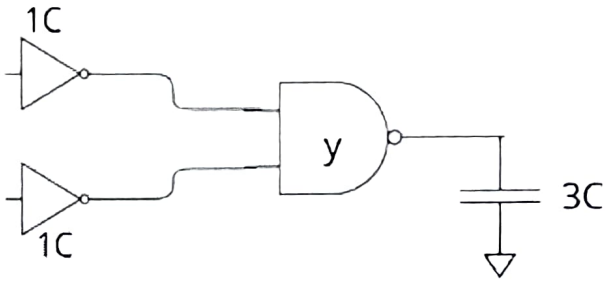
b) Calculate the Contamination Rise/Fall Delay using Elmore Delay. **(CO2, 2 marks)**

c) Calculate the Propagation Rise/Fall Delay using Elmore Delay. **(CO3, 2 marks)**

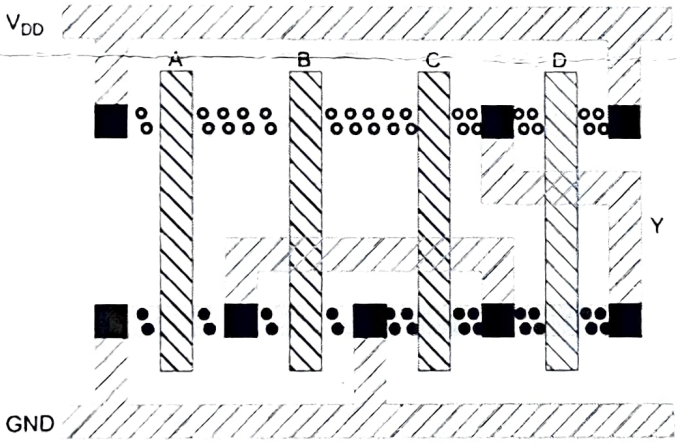
d) Calculate the logical effort of each input. **(CO3, 1 mark)**

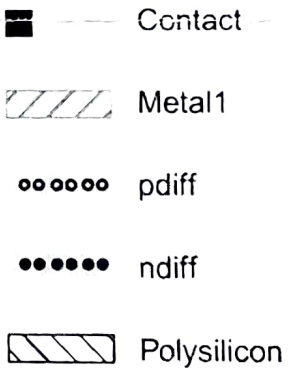
Q5) Consider the two alternative circuit implementations of a 2-input OR gate as shown in the figure below. Provide an intuitive argument to determine which design is expected to demonstrate slow performance. **(0.5 marks)** Support your reasoning with a quantitative analysis by calculating the path effort, delay **(1 mark)**, and the input capacitances x and y required to achieve this delay **(1 mark)**. Also size the corresponding transistors accordingly **(1 mark)**. **(CO2, 3.5 marks)**





Q6) For the given layout **(CO5, 2 marks)**





a) Draw the transistor-level schematic. **(1 mark)**

b) Derive the Boolean expression of output Y **(1 mark)**

Q7) [Bonus] A product is designed in 90nm technology and takes up 100 mm² area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs. 10/-. The designers use a denser version of libraries to reduce the area to 80 mm². What is the new expected Yield? The product is still sold for Rs. 100/-. How much profit does the company make now per product sold? **(CO1, 2 marks)**