

VDF Mid-Semester Exam Solutions 2020

1. i. Following are the values of Y, Z and W:

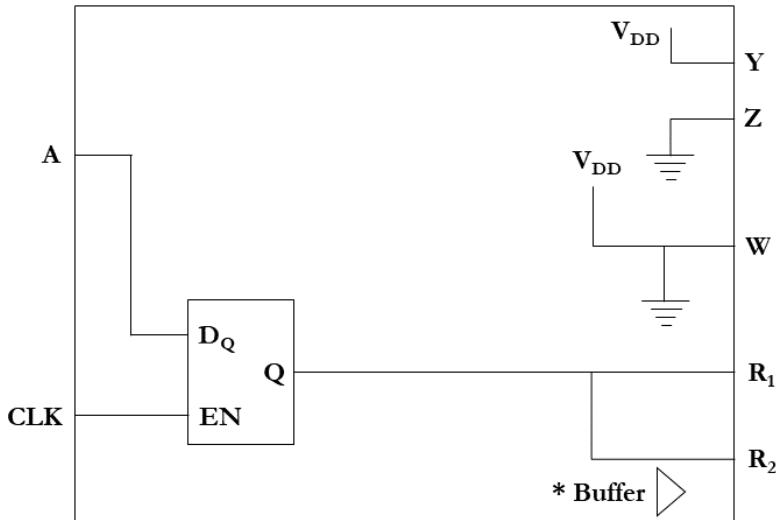
$$Y = 1'bx$$

$$Z = 1'bx$$

$$W = 1'bx$$

0.5 marks for each correct answer

- ii. Drawn below is the schematic of the expected netlist:



- W can either be connected to ground or power supply
- A buffer can also be added as denoted.

1 marks for each output

For Y and Z, if you use OR/AND gates then 0.5 marks.

- iii. **Four valued logic** is one in which there are 4 possible states, namely- 0, 1, X and Z. The values of Y, Z and W are written below:

$$Y = 1,$$

$$Z = 0,$$

$$W = 0 / 1$$

0.5 marks for each correct answer

- iv. As the sensitivity list does not contain A, when clock is positive, when the value of A changes, it won't get assigned to R2. This does not happen in synthesis. Thus, a mismatch!

2 marks for each correct

2. a i. $X = Y$ (for metastability) **1 mark**

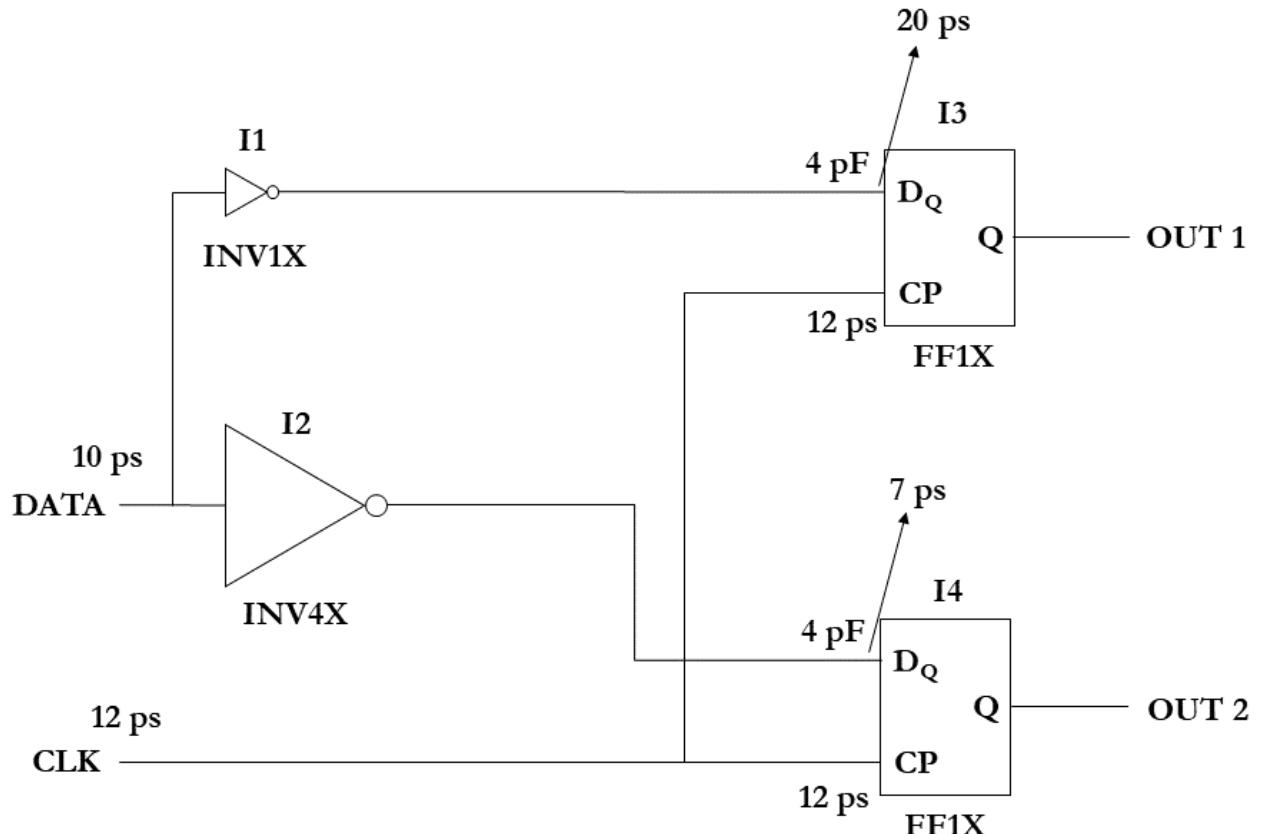
$$\text{Thus, } X = 12 - 20X \text{ **1 mark**$$

$$X = 0.5714V \text{ **1 mark**}$$

ii. V_{IN} becomes $0.5714 - 0.001 = 0.5704$ V, thus moving away from metastable region. Value of V_{OUT} becomes 2V

iii. V_{OUT} becomes 0V

b. Referring to the tables, the transition times can be listed as shown in the figure. For I4, use interpolation to determine the hold time, as the value corresponding to 7ps is not mentioned.



Transition at I3/D=20 **1 Mark**

Transition at I3/CP=12

Hold value at I3=15 ps **1 mark**

Transition at I4/D=7 **1 mark**

Transition at I4/CP=12

Hold value at I₄=8.6 **2 marks**

Question 3a.

$$A \cdot d = 0.25 \text{ cm}^2 \cdot 0.5 = 0.125 \quad \text{(1 mark)}$$

$$\begin{aligned} \text{Yield} &= (1 + Ad/\alpha)^{-\alpha} \times 100\% \\ &= (1 + 0.25 \cdot 0.5 / 0.5)^{-0.5} \times 100\% \quad \text{(1 mark)} \\ &= 89.44\% \quad \text{(1 mark)} \end{aligned}$$

$$\text{Area of wafer} = \pi r^2 = \pi \times 15 \times 15 = 706.85 \text{ cm}^2$$

$$\text{Area of die} = 0.25 \text{ cm}^2$$

$$\text{Number of dies fabricated} = 706.85 / 0.25 = 2827 \quad \text{(1 mark)}$$

$$\text{Number of good dies} = 2827 \times 89.44\% = 2528 \quad \text{(1 mark)}$$

$$\text{Cost per die} = \$100 / 2528 = 3.96 \text{ cents} \quad \text{(1 mark)}$$

Question 3b.

1. Protection of mask from chemical and mechanical damage

OR

2. It keeps dust particles away from the surface such that even when dust is on the pellicle, it will be out of focus from the projection system and there will be no impact of dust falling from the mask. **(1 mark)**

Question 3c.

Area increases yield decreases **(1 mark)**

Reason: a single defect on large area die implies more proportion of the wafer will be affected hence yield decreases. Whereas a single defect on small area dies implies that less proportion of the wafer will be affected. **(1 mark)**

Question 3d.

Any two

1. OPC (optical proximity correction)
2. Multi-patterning/ double patterning
3. Phase shift mask
4. Immersion lithography

(0.5 mark for each technique - Total 1 mark)

Question 3e.

B is more likely to be defective **(1 mark)**

Reason: defects typically appear in clusters. Therefore, there is a greater probability of having a defective die near a die that is already found to be defective. **(1 mark)**

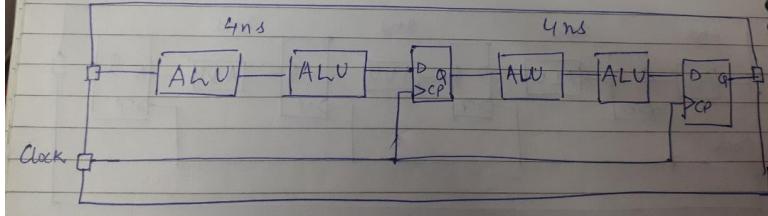
Question 4a.

$$f = 1/8ns \quad \text{(1 mark)}$$

$$= 125\text{MHz} \quad \text{(1 mark)}$$

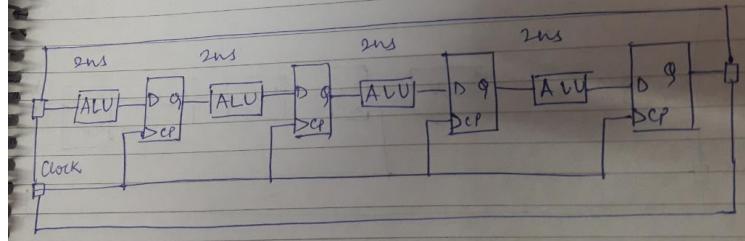
Question 4b.

(i) Max operable freq = 2 times
 $= \frac{1}{8\text{ns}} \times 2$



(2 marks)

(ii) Max. operable freq = 4 times
 $= \frac{1}{8\text{ns}} \times 4$



(2 marks)

Question 4c.

Any two

1. Area increases
2. Power increases
3. Latency increases

(1 mark each - total 2 marks)

Kavish Vishwakarma

VLSI Design Flow

Mid Semester Exam (15th February 2020)

Time allowed: 1 hour

Maximum Marks: 40

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Use of any communication device is prohibited during examination.
- VI. Cheating or use of unfair means will be dealt with as per institute policy.

1. As per Verilog IEEE Std 1364-2001 (from Verilog URM), the definitions of binary AND (&) and OR (||) operators are as follows:

Table 19—Bit-wise binary and operator

δ	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

Table 20—Bit-wise binary or operator

1	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

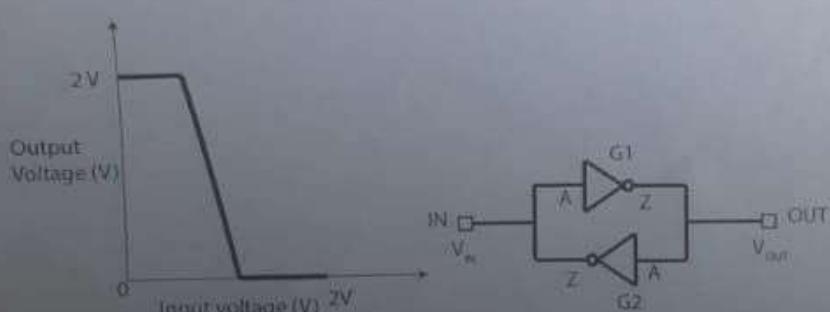
A Verilog design is as follows:

```
module top(A, clk, R1, R2, W, Y, Z);
    input A, clk;
    output R1, R2, W, Y, Z;
    reg R1, R2;

    assign Y = ~A|A;
    assign Z = ~A&A;
    assign W = 1'bx;
    always @ (clk or A)
        if (clk)
            R1 <= A;
    always @ (clk)
        if (clk)
            R2 <= A;
endmodule
```

- (a) Assume that the value of A is 1'bx. What will be the value of Y, Z and W if the above code is simulated using four-valued logic? (1)
- (b) Draw the schematic of the expected netlist for the above Verilog code when synthesized. (2)
- (c) Assume that the value of A is 1'bx. What will be the value of Y, Z and W if the above expected netlist is simulated using four-valued logic? (1)
- (d) If the underlined block of code is synthesized as a latch, then there can be a synthesis-simulation mismatch. Explain why. (2) (1.5+5+1.5+2 Marks)

2.



3. An approximate transfer characteristic of a CMOS inverter is shown above. Assume that the supply voltage is 2V. Assume that in the transition region the output voltage (V) is

$\gamma = 12 - 20X$, where X is the input voltage in volts. In other regions, the inverter characteristics are ideal.

Using the above inverter, a primitive memory element is built by cross-coupling as shown on the previous page.

(3)

- Find the metastable voltage (V_{MS}) for the cross-coupled inverter.
- Assume that the cross-coupled inverter was initially in the metastable state. If due to thermal noise, V_{IN} decreases by 1 mV, then what will be the stable voltage V_{out} ?
- Assume that the cross-coupled inverter was initially in the metastable state. If due to thermal noise, V_{IN} increases by 1 mV, then what will be the stable voltage V_{out} ? (3+1+1 Marks)

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$\frac{27}{2} = \frac{11}{2e}$

BS

- b. Assume that for the library cells INV1X, INV4X and FF1X, the NLDM tables specified in a technology library is as follows:

Output transition in ps for INV1X:

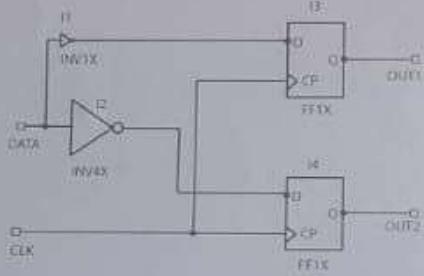
Load -> Input Transition V	2 pF	4 pF	8 pF	16 pF
10 ps	10	20	30	40
20 ps	20	30	40	50
40 ps	30	40	50	60
80 ps	40	50	60	70

Output transition in ps for INV4X:

Load -> Input Transition V	2 pF	4 pF	8 pF	16 pF
10 ps	5	7	8	10
20 ps	10	20	30	40
40 ps	20	30	40	50
80 ps	30	40	50	60

Hold Time in ps for FF1X:

Clock Pin Transition -> Data Pin Transition V	5 ps	10 ps	12 ps	15 ps
5 ps	5	6	7	8
10 ps	9	10	11	12
20 ps	13	14	15	16
40 ps	17	18	19	20



Consider the design as shown above. The instances I1, I2, I3 and I4 are of library cells INV1X, INV4X, FF1X and FFF1X, respectively.

Assume that all the wires are ideal (with negligible resistance and capacitance). The load capacitance of D pin is 4 pF. The input transition at the port DATA is 10 ps and the port CLK is 12 ps.

Find the hold time of flip-flops I3 and I4. Show all the steps. Just writing answer will not fetch any marks.

(2+3 Marks)

3.

- a. The yield is given by the following equation;

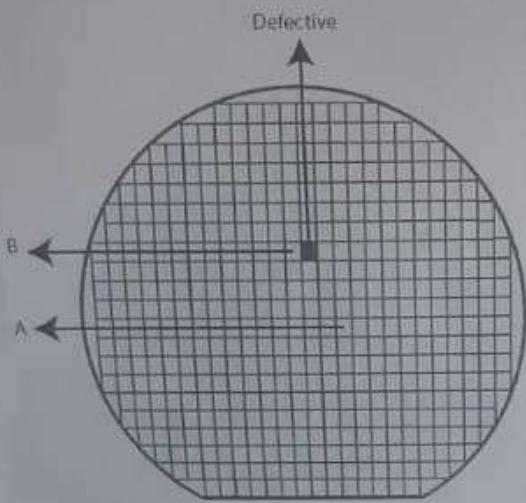
$$Yield = (1 + Ad/\alpha)^{-\alpha} \times 100\%$$

where A is the area of the die, d is the defect density and α is the clustering parameter. The diameter of the wafer is 300 mm and the die size is 25 mm². Assume that the cost of fabricating a wafer is \$100 and there is no wastage of material in creating dies out of wafer. Assume defect density is 0.5 defect/cm² and clustering parameter is 0.5. Estimate the yield and the cost per die

(3+3 Marks)

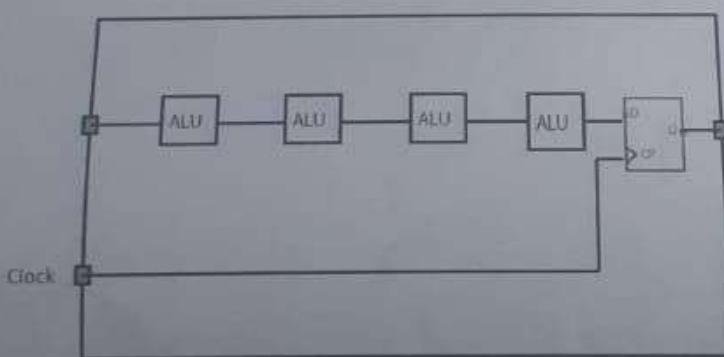
- b. What is the purpose of a pellicle on a mask? (1 Mark)
 c. If the area of a die increases then how is the yield expected to change (i.e. yield will increase or decrease)? Give reason for your answer. (2 Marks)
 d. Name any two resolution enhancement techniques. (1 Mark)

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A defect is found on a die on a wafer, as shown above. Consider two dies A and B, as shown above. Which of the two dies is more likely to be defective. Give reasons for your answer. (2 Marks)

4. Consider the following synchronous circuit. It receives data from another circuit that uses the same clock.



- a. Estimate the maximum operable frequency of the circuit. Make the following assumptions:
- All ALUs have delay of 2 ns
 - All nets are ideal and have delays of 0 ns
 - All flip-flops are ideal. Setup Time of flip-flop is 0 ps
 - All clocks are ideal

- v. Input Delay of Data Path is 0 ns. (2 Marks)
- b. A designer decided to improve the maximum operable frequency of the circuit by introducing some flip-flops (as many as required) in the data-path of the circuit. Modify and redraw the circuit shown on the previous page such that the maximum operable frequency is two times that computed in (a).
- Modify and redraw the circuit shown on the previous page such that the maximum operable frequency is four times that computed in (a). (2+2 Marks)
- c. Name two disadvantages of modified circuits with respect to the original circuit shown on the previous page. (2 Marks)

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VLSI Design Flow

Mid Semester Exam (8th March 2021)

Time allowed: 1 hour

Maximum Marks: 40

1.

a)

Let N functions be implemented in hardware.

$$\text{Total cost} = 1000 + N \cdot 400$$

To meet cost constraint

$$1000 + N \cdot 400 < 2500$$

$$N < 3.75$$

Maximum N=3

The three functions that take maximum percentage of time are moved to dedicated hardware are: F6, F8 and F3. **2 Marks**

$$\text{Cost} = 1000 + 3 \cdot 400 = \text{Rs } 2200/- \quad \text{1 Mark}$$

$$\text{Runtime of functions implemented in software} = 0.30 \cdot 1000 = 300 \text{ s}$$

$$\text{Runtime of functions implemented using dedicated hardware} = (1/10) \cdot 0.70 \cdot 1000 = 70 \text{ s}$$

$$\text{Total runtime} = 300 + 70 = 370 \text{ s.} \quad \text{2 Marks}$$

b) Since runtime with 3 functions moved to dedicated hardware is 370 s (more than target of below 350), we need to move more function to dedicated hardware.

Let us move 4th top function F5 to dedicated hardware that consumes 10% of total runtime.

$$\text{Total runtime} = 0.20 \cdot 1000 + (1/10) \cdot 0.80 \cdot 1000 = 200 + 80 = 280 \text{ s.}$$

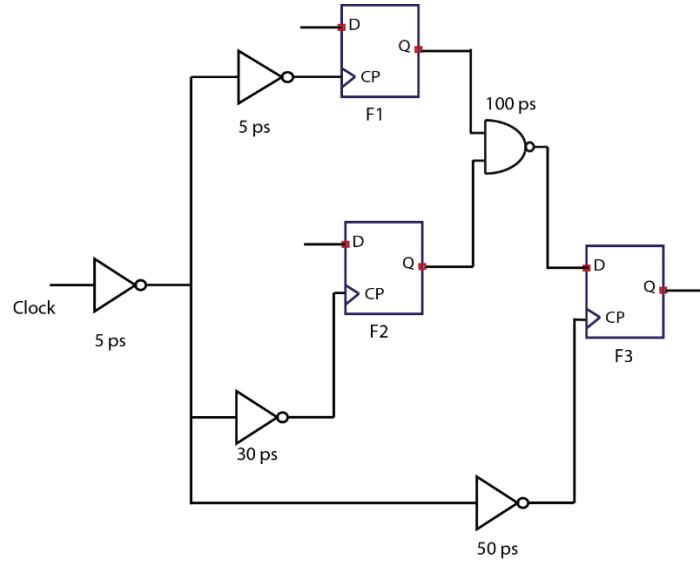
So we need to move F6, F8, F3, and F5 to dedicated hardware. **2 Marks**

$$\text{Runtime} = 280 \text{ s} \quad \text{1 Mark}$$

$$\text{Cost} = 1000 + 4 \cdot 400 = \text{Rs. } 2600/- \quad \text{2 Marks}$$

2.

(a)



Clock-frequency = 1 GHz

Time period = $10^{-9}s = 1000 \text{ ps}$

Setup analysis

Path from F1 to F3:

Setup Slack: $(1000+5+50)-(5+5+50+100+30)=865 \text{ ps}$ **1.5 Marks**

Path from F2 to F3:

Setup Slack: $(1000+5+50)-(5+30+50+100+30)=840 \text{ ps}$ **1.5 Marks**

Therefore, the worst setup slack is 840 ps (F2 to F3) **1 Mark**

Hold analysis

Path from F1 to F3:

Hold Slack: $(5+5+50+100)-(5+50+10)=95 \text{ ps}$ **1.5 Marks**

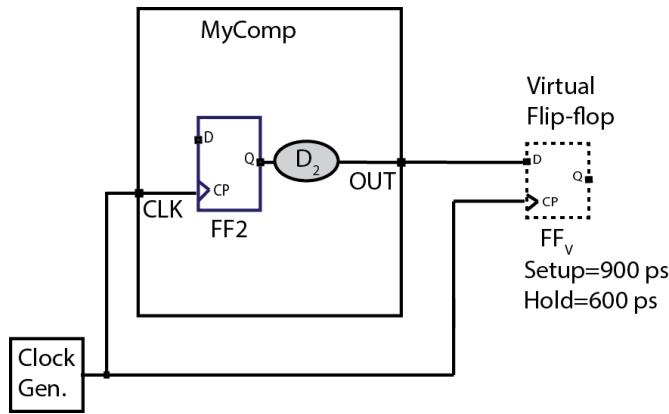
Path from F2 to F3:

Hold Slack: $(5+30+50+100)-(5+50+10)=120 \text{ ps}$ **1.5 Marks**

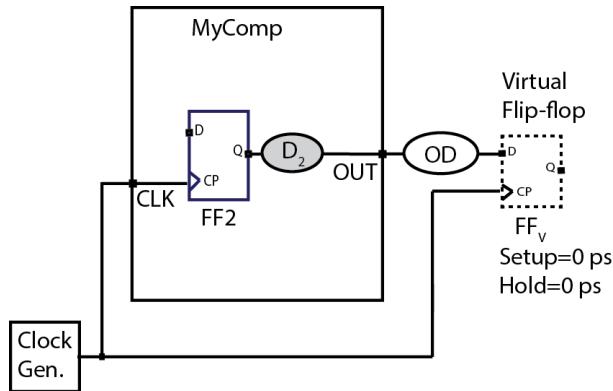
Therefore, the worst hold slack is 95 ps (F1 to F3) **1 Mark**

(b)

The requirement is similar if we consider a flip-flop at the output port with a setup and hold times of 900 ps and 600 ps, as follows:



This situation needs to be modelled using SDC set_output_delay which works as follows:



The above two figures should yield the same constraint or requirement.

To make them same, we need to find adjust the delay of the element OD for the maximum case (setup) and the minimum case (hold).

For setup analysis:

From first figure:

$$T_{FF} + T_{D2,max} + 900 < T_{period}$$

From second figure:

$$T_{FF} + T_{D2,max} + T_{OD,max} < T_{period}$$

Therefore: $T_{OD,max} = 900$ ps 1 Marks

For hold analysis:

From first figure:

$$T_{FF} + T_{D2,min} > 600$$

$$T_{FF} + T_{D2,min} - 600 > 0$$

From second figure:

$$T_{FF} + T_{D2,min} + T_{OD,min} > 0$$

Therefore: $T_{OD,min} = -600$ (Note the negative sign). 3 Marks

We need to find the value of delay

The SDCs are:

create_clock -name SYS CLOCK -period 2000 [get ports CLK] 1 Mark

set output delay 900 -max -clock [get clocks SYS CLK] [get ports OUT]

set output delay -600 -min -clock [get clocks SYS CLK] [get ports OUT]

2 Marks

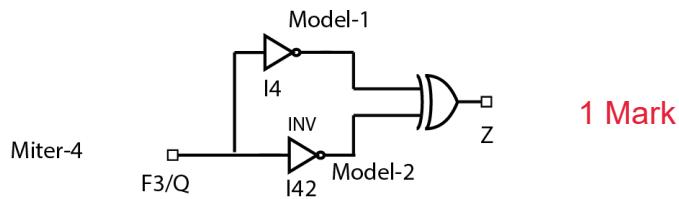
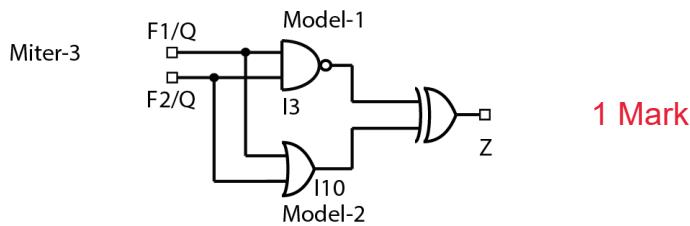
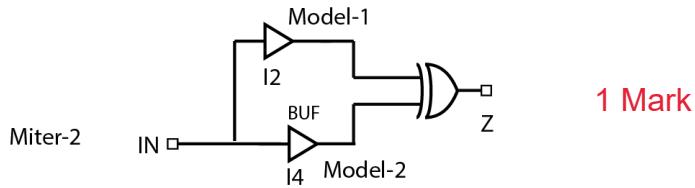
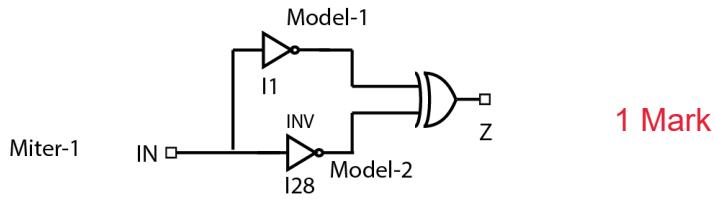
-0.5 if -clock option is missing

3.

a)

Each of the following four miters need to be drawn separately to get marks.

Specifically, the inputs and instance name should be marked correctly in each miter and an XOR gate must be placed at the output.



b) The Miter-3 will show failure because output can be made 1. **2 Marks**

The patterns at inputs that satisfy the miter (or make the models inequivalent or fail) are:

$\$F1/Q=0, F2/Q=0\$$ and $\$F1/Q=1, F2/Q=1\$$. **3 Marks**

c) No, these are invalid patterns, because $F1/D$ is the complement of $F2/D$. Therefore, the possible values of $\{F1/Q, F2/Q\}$ are $\{01\}$ and $\{10\}$. Therefore, $\{00\}$ and $\{11\}$ cannot occur. Thus, it is a false failure. **6 Marks**

VLSI Design Flow

Mid Semester Exam (8th March 2021)

Time allowed: 1 hour

Maximum Marks: 40

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Cheating or use of unfair means will be dealt with as per institute policy.

1. A software was profiled, and the % of time spent (on an average) in different functions are shown below.

Function name	% Time
F1	5
F2	3
F3	15
F4	5
F5	10
F6	30
F7	5
F8	25
F9	2

The cost of a product entirely implemented with the above software running on a general purpose microprocessor is Rs 1000/- . We can implement each function of the software using separate dedicated hardware. The runtime of any function implemented with dedicated hardware is 1/10th of that implemented in software. However, when we implement any function with dedicated hardware, the product cost increases by Rs 400/- per function, while the cost of the software remains unchanged.

- a) Assume that you need to keep the product cost below Rs 2500/- . How will you perform software-hardware partitioning such that you obtain the **minimum** runtime meeting the cost constraint? What is the estimated cost of the system? Assume that a given application consumed 1000s when entirely implemented in software. What is the estimated runtime in your designed system?

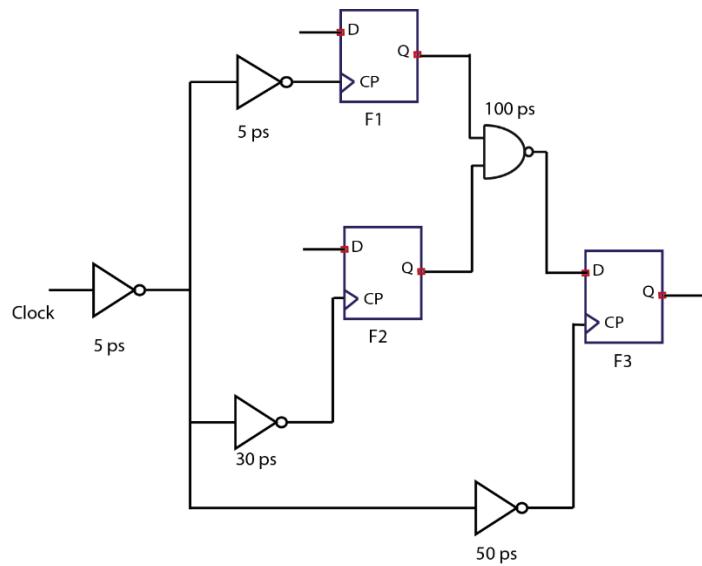
[2+1+2 Marks]

b) This question is independent of part (a). However, the information above part (a) is valid for this question also. Assume that a given application takes a runtime of 1000 s when entirely implemented in software. **However, we need to reduce the runtime of this application below 350 s by running some functions on dedicated hardware.** How will you perform software-hardware partitioning such that you obtain the **minimum** cost and meet the runtime constraint? What is the estimated runtime for the application in your system? What is the estimated cost of your designed system?

[2+1+2 Marks]

2.

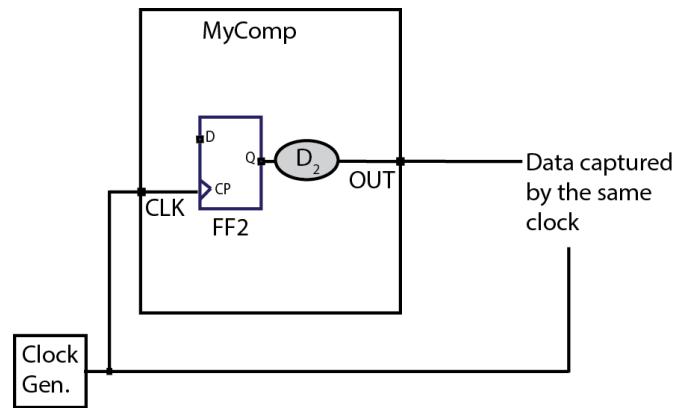
(a)



A portion of a sequential synchronous circuit is shown above. The following attributes are valid for all the flip-flops F1, F2 and F3: Setup time = 30ps, Hold time = 10ps, and CP->Q Delay = 50ps. The delay of the NAND gate N1 is 100ps and the delay of inverters are shown in the figure. The frequency of the Clock is 1GHz. Ignore the delay of all the wires. **Find the worst setup slack and the worst hold slack of the circuit. Show all relevant computations.**

[4+4 Marks]

(b)



Consider the above circuit. The period of the clock signal generated by the clock generator is 2000 ps (unit of time in library is ps). The data generated by the output port OUT of MyComp is captured externally by the same clock signal (as shown above). Additionally, the following requirements for the signal generated at the output port OUT should be satisfied:

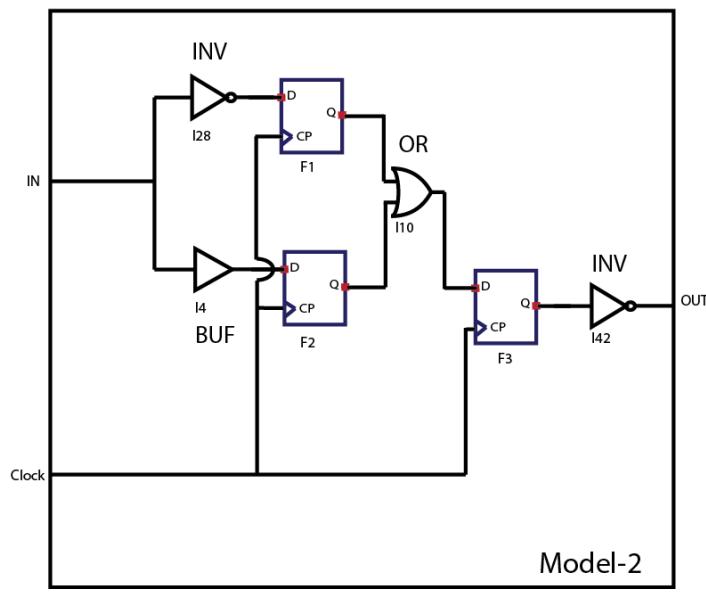
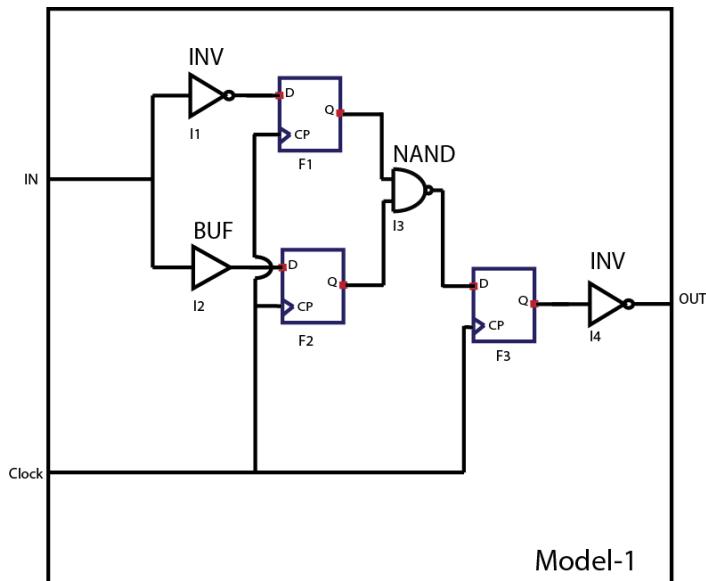
- a) it should be available by 900 ps before the clock edge, and
- b) it should be stable for 600 ps after the clock edge.

Write all the **SDC commands** to model the above requirements (including that of the clock signal).

[1+2+4 Marks]

[See the next page]

3.



Consider the netlist of Model-1 and Model-2 shown above. We perform Combinational Equivalence Checking between the above two models. The ports and registers are matched by their names.

- a) Draw all the miter circuits separately that will be created for CEC for the above models. Label the instances/ports in the miter with their corresponding names in the model [where ever possible].
- b) Which of the miter circuits drawn in (a) will fail [Put some label to miters in (a) and indicate the label here, no need to redraw]? Report all the failing patterns. Explain your answer.
- c) Are the above failures reported by CEC correct (i.e. two models will give different responses) or are they false failures? Explain your answer (no marks without correct explanation).

[4+5+6 Marks]

VLSI Design Flow

End Semester Exam (2nd May 2021)

Time allowed: 70 minutes

Maximum Marks: 45

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in the given time.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Cheating or use of unfair means will be dealt with as per institute policy.

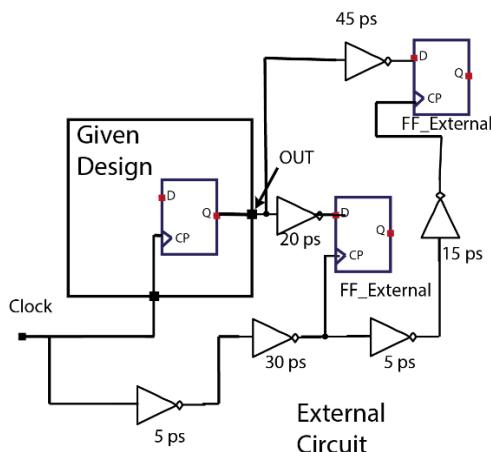
1. For some process, the yield is given by the following equation:

$$Yield = (1 + Ad/\alpha)^{-\alpha} \times 100\%$$

where A is the die area, d is the defect density, and α is the clustering parameter. The wafer diameter is 300 mm, and the die size is 25 mm². Assume that the cost of fabricating a wafer is \$100 and there is no wastage of material in creating dies out of the wafer. Assume defect density is 0.5 defect/cm² and the clustering parameter is 0.5.

- (a) Estimate the yield and the cost per die. [3+3 Marks]
(b) Due to yield learning, defect density decreases to 0.1 defect/cm². Estimate the new yield and the cost per die. [2+2 Marks]

2.



You are the designer of "Given Design". You need to develop a constraint file (SDC file) for the module "Given Design" (as shown above). Assume that, all relevant external circuit connected to "Given Design" is given to you (and shown above). The delay of inverters are shown in the figure itself. Take setup time of all the external flip-flops as 22 ps and that in the "Given Design" as 26 ps. Take the clock-to-q delay of all the external flip-flops as 39 ps and that in the "Given Design" as 47 ps.

You need to write the SDC command “set_output_delay” for the port OUT for **late analysis** (to meet setup-checks in the external circuit). What should be the value of output-delay that must be set at the output port OUT for **the late analysis?** Show relevant calculations for all paths. Write the SDC command “set_output_delay” for the late analysis [Take the name of clock in SDC as CLK]. Ignore early analysis and wire delays in this question. **[10 Marks]**

3. A netlist of a design is as shown below:

```
module top(A, B, C, D, E, Z1, Z2);
    input A, B, C, D, E;
    output Z1, Z2;

    nor I1(n1, A, B);
    and I2(Z1, n1, n2);
    nand I3(n2, B, C, D);
    not I4(n3, D);
    nor I5(n4, n3, E);
    and I6(Z2, n2, n4);

endmodule
```

Draw the schematic of the above netlist

Assume that the output pin of all the gates is represented as Y. Assume single stuck-at fault model in this question. Using path sensitization method, find a test vector that simultaneously detects both SA-0 at the pin I1/Y and SA-0 at the pin I3/Y. **[2+8 Marks]**

4. Assume that there are three nets in a design: N1, N2 and N3. The net N1 is connected to three cells C1, C2, and C3. The net N2 is connected to two cells C4 and C5. The net N3 is connected to five cells C6, C7, C8, C9, and C10. A placement tool has identified the following locations of cells:

C1(0,0), C2(10,4), C3(2,6),
C4(0,10), C5(0,20),
C6(0,30), C7(0,35), C8(20,35), C9(35,35), and C10(70,75).

(a) Compute the total WL of the design, based on half-perimeter wire length approximation. The unit of length is micron. **[5 Marks]**

(b) A placement tool is using a simulated annealing algorithm to find the optimum solution. The acceptance probability of the new solution is given as $e^{-(\Delta E/T)}$ when $\Delta E > 0$. Here ΔE is the increase in the total wire length due to the new solution and $T = 40$ micron. The placement engine perturbs the above solution by changing the location of C10 (all other cells are at the same location as mentioned above). Find ΔE and the acceptance probability if the new location of C10 is as follows:

- i) C10(70,45) **[3 + 2 Marks]**
ii) C10(90,95) **[3 + 2 Marks]**

VLSI Design Flow

Solution of Mid Semester Exam (13th March 2022)

Time allowed: 1 hour

Maximum Marks: 30

1. Area of wafer = $\pi r^2 = \pi * 15 * 15 = 706.85 \text{ cm}^2$

Area of die = 0.25 cm²

Number of dies fabricated = $706.85 / 0.25 = 2827$ **1 mark**

(a) $A_d = 0.25 * 0.5 = 0.125$

$\text{Yield} = (1 + 0.125 / 0.5)^{-0.5} * 100 = 89.44\%$ **1 mark**

Number of good dies = $2827 * 0.8944 = 2528$ **1 mark**

Cost per die = $\$200 / 2528 = 7.92$ cents **1 mark**

(b) New $A_d = 0.25 * 0.1 = 0.025$

$\text{New Yield} = (1 + 0.025 / 0.5)^{-0.5} * 100 = 97.6\%$ **1 mark**

Number of good dies = $2827 * 0.976 = 2758$ **1 mark**

Cost per die = 7.24 cents **1 mark**

The yield improves because the defect density decreases and less percentage of dies get impacted by the defect. **1 mark**

(c) Area of die = 1 cm²

Number of dies fabricated = $706.85 / 1 = 706$ **0.5 mark**

$A_d = 1 * 0.1 = 0.1$

$\text{New Yield} = (1 + 0.1 / 0.5)^{-0.5} * 100 = 91.3\%$ **1 mark**

Number of good dies = $706 * 0.913 = 644$ **0.5 mark**

Cost per die = $20000 / 644$ cents = 31.06 cents **1 mark**

The yield decreases because with the increased die area, the probability of getting a defect on a die increase. **1 mark**

2.

- a. `create_clock -name VCLK -period 1
set_input_delay 0.1 -clock [get_clocks VCLK] [get_ports IN]` **0.5+0.5 mark**
- b. `set_case_analysis 0 [get_ports TM]`

set_case_analysis 1 [get_ports NORMAL] 0.5+0.5 mark

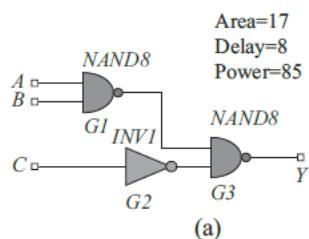
c.

set_multicycle_path 8 -setup -from [get_pins FF1/CP] -to [get_pins FF2/CP]
set_multicycle_path 5 -hold -from [get_pins FF1/CP] -to [get_pins FF2/CP]

1 mark for setup
3 marks for hold
[0 marks if multiplier is wrong in hold]

3.

(a)

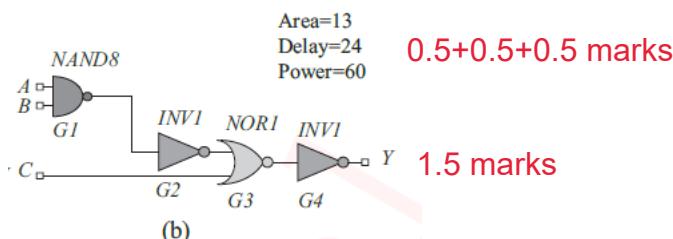


0.5+0.5+0.5 marks for area, delay power calculations

1.5 marks for circuit mapping

(a)

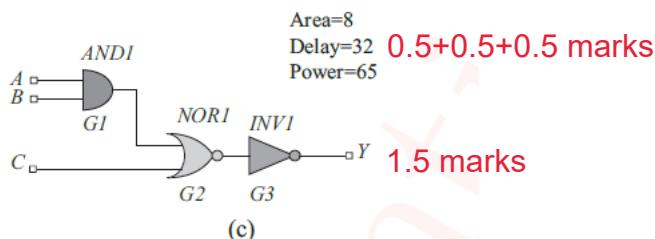
(b)



0.5+0.5+0.5 marks

1.5 marks

(c)



0.5+0.5+0.5 marks

1.5 marks

(c)

(d) (i) (c) has minimum area

(ii) (a) has minimum delay of worst path

(iii) (b) has minimum power

1+1+1 marks

VLSI Design Flow

Mid Semester Exam (13th March 2022)

Time allowed: 1 hour

Maximum Marks: 30

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Cheating or use of unfair means will be dealt with as per institute policy.

1. For a given process, the yield is modeled by the following equation:

$$Yield = \left(1 + \frac{Ad}{\alpha}\right)^{-\alpha} \times 100\%$$

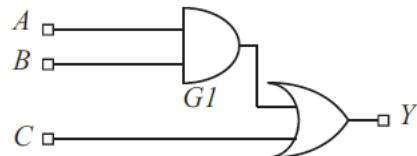
where A is the die area, d is the defect density, and α is the clustering parameter. The wafer size is 300 mm in diameter, and the die size is 25 mm². Assume that the cost of fabricating a wafer is \$200, and there is no wastage of material in creating dies out of the wafer. Assume defect density is 0.5 defect/cm² and the clustering parameter is 0.5.

- (a) Estimate the yield and the cost per die.
- (b) Due to yield learning, defect density decreases to 0.1 defect/cm². Estimate the new yield and the cost per die. Explain why does the yield change from that computed in (a).
- (c) Assume that defect density remains as 0.1 defect/cm², but the die area is increased to 100 mm². Compute the new yield and the cost per die? Explain why does the yield change from that computed in (b). [4+4+4 Marks]

- 2.

- a. You need to define a virtual clock with name *VCLK* and clock frequency 1 GHz. Then you need to define input delay of 100 ps at the input port named *I/N* with respect to the virtual clock *VCLK*. Assume that you need to use nanosecond as the unit of time in the SDC file. Write a set of SDC commands to define these constraints.
- b. You are writing an SDC file for the functional mode. In the functional mode, the input port *TM* should be 0 and the input port *NORMAL* should be 1. Write a set of SDC commands to define these constraints.
- c. Define multicycle path between flip-flop instances FF1 and FF2 (with clock pin name *CP*) that makes setup check on the 8th clock edge (instead of default 1st clock edge) and hold check on 2nd clock edge (instead of default 0th clock edge). Write a set of SDC commands to define these constraints. [1+1+4 Marks]

3. Consider the generic-gate circuit shown in Fig. (a). A technology mapper needs to map this generic circuit using library cells shown in Fig. (b). Show the schematic diagram of the mapped circuit (circuit that contains instances of library cells only) in each of the following cases and compute the circuit area, maximum combinational path delay, and power dissipation in each of the mapped circuit.



(a)

<u>Cell Name</u>	<u>Symbol</u>	<u>Function</u>	<u>Area</u>	<u>Delay</u>	<u>Power</u>
<i>INV1</i>		$Z = A'$	1	4	5
<i>NAND8</i>		$Z = (A \cdot B)'$	8	4	40
<i>NOR1</i>		$Z = (A + B)'$	3	12	10
<i>AND1</i>		$Z = A \cdot B$	4	16	50

(b)

- (a) Mapper uses **NAND gate(s)** and **inverter(s)**. And no other gate.
- (b) Mapper uses only **NAND gate(s)**, **NOR gate(s)** and **inverter(s)**. And no other gate.
- (c) Mapper uses only **AND gate(s)**, **NOR gate(s)** and **inverter(s)**. And no other gate.
- (d) Which of the above cases has (i) minimum area (ii) minimum path delay for the worst case, and (iii) minimum power [Just mention a, b, or c for each part of this question].

[3+3+3+3 Marks]

VLSI Design Flow

End Semester Exam (12th May 2022)

Time allowed: 2 hours

Maximum Marks: 50

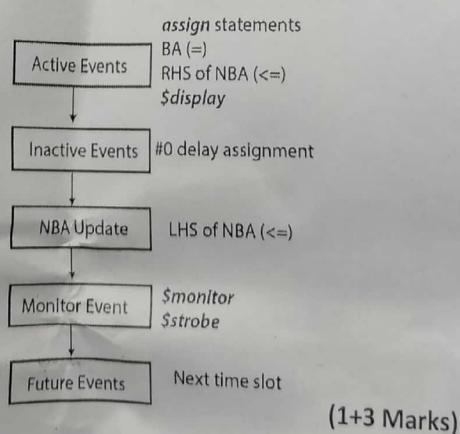
Note:

- I. There are 3 questions (each of them has sub-parts). All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 2 hours.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Use of any communication device is prohibited during examination.
- VI. Cheating or use of unfair means will be dealt with as per institute policy.

1.
 - a. Consider the following piece of Verilog code.

```
→ assign p = q;  
initial  
begin  
→ q = 1;  
#1 q = 0;  
$display(p);  
end
```

What will be displayed by \$display statement above? Explain your answer. The stratified Verilog event queue is shown below (You may use it if you want).



(P=1)

- b. Consider the following Verilog code.

```

module top(a, b, c, s, en, out1, out2);
    input a, b, c, s, en;
    output out1, out2;
    reg out1, out2;

    always @(*) begin
        if (s==1'b0)
            out1 = a;
        else
            out1 = b;
    end

    always @(*) begin
        if (en==1'b1)
            out2 = c;
    end
endmodule

```

Predict and draw the schematic of the synthesized netlist (mark the circuit elements properly).

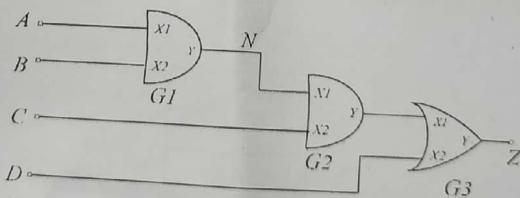
(4 Marks)

- c. Consider an FSM with five states $Q = \{s_0, s_1, s_2, s_3, s_4\}$. Let the states be represented by three state bits a, b, c , and encode the states as bit sequence (abc) . Let the encoding be $\{000, 001, 010, 011, 100\}$ for the states $Q = \{s_0, s_1, s_2, s_3, s_4\}$, respectively. For this encoding, find the characteristic function of the subset of states $\{s_0, s_2, s_4\}$ (a characteristic function of a set indicates whether an element belongs to that set or not). Draw the ROBDD for this function with the variable order a, b, c .
- d. How can increasing the size of a cell in the critical path improve the worst setup slack? (2+3 Marks)

2.

(2 Marks)

- a. Consider the circuit shown below.



- For the net N , find the set of test pattern(s) that will make it 0.
- Find the set of test pattern(s) that will detect SA0 at the net N .
- Choose an appropriate pattern P_1 from (i) above and pattern P_2 from (ii) above such that if we apply P_1 and then P_2 , we will be able to observe the effect of a rise transition occurring at the net N at the output Z .
- Explain how does the pattern chosen in (iii) able to detect a slow-to-rise transition fault at the net N . [A slow-to-rise transition fault is manifested as a signal rising very slowly from the 0 state].

[1+1+1+2 Marks]

- b. There were two chips fabricated: 'chip-A' and 'chip-B,' both fabricated for a frequency of 1 GHz. However, due to human error, 'chip-A' had **setup violations** at 100 different flip-flops and was erroneously ignored by the designer. The correct slacks for setup checks at these flip-flops were -20 ps.

Similarly, due to human error, 'chip-B' had **hold violations** at 100 different flip-flops and was ignored by the designer. The correct slacks for hold check at these flip-flops were 20 ps.

Which of the two chips can be given to a customer who does not require to run the chip at a very high frequency and which cannot be given? Explain both your answers.

(1+2 Marks)

- c. Consider a sub-circuit with three nets N_1 , N_2 , and N_3 .

The net N_1 has 3 pins p_1 , p_2 , and p_3 with locations $(0,0)$, $(1,5)$, and $(4,3)$, respectively.

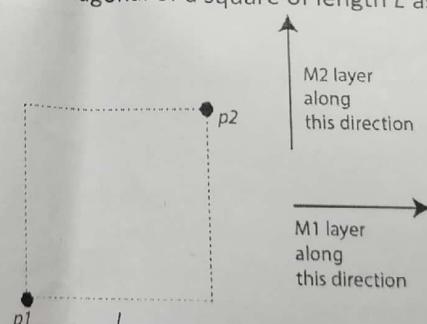
The net N_2 has 4 pins p_4 , p_5 , p_6 , and p_7 with locations $(3,4)$, $(2,5)$, $(4,4)$, and $(2,9)$, respectively.

The net N_3 has 2 pins p_8 and p_9 with locations $(7,7)$ and $(9,16)$, respectively.

Estimate the total wirelength using Half-perimeter Wire length (HPWL) measure.

(4 Marks)

- d. Two pins p_1 and p_2 are at the diagonal of a square of length L as shown below.

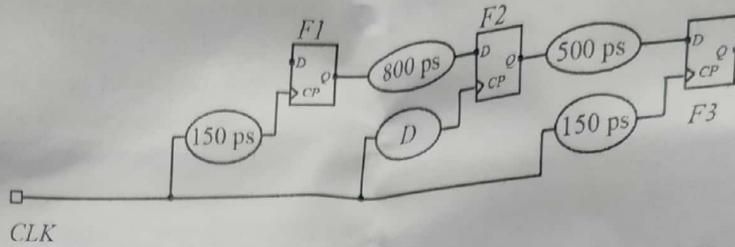


Determine the percentage reduction in the optimum wirelength connecting p_1 to p_2 if the routing along the diagonal (45° orientation) is allowed compared to the traditional Manhattan orientation.

(3 Marks)

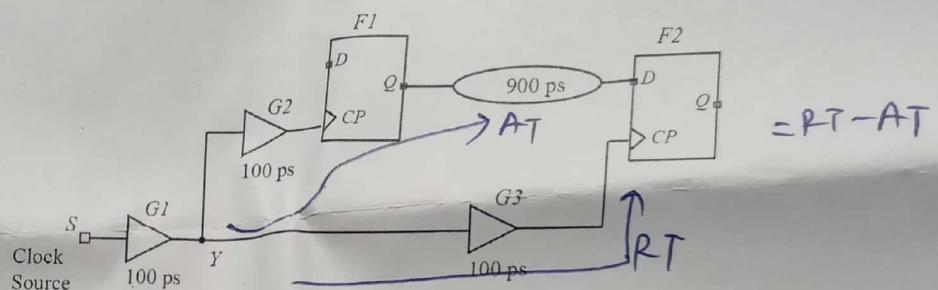
3.

- a. The critical portion of a circuit is shown below.



Assume that all the flip-flops are ideal (setup time, hold time, and CP->Q delay are zero). Find the delay D of the element in the clock path such that the circuit operates at the maximum clock frequency satisfying the setup constraint. Ignore the delay of the wires and the hold constraints. Find the corresponding clock period. (4+1 mark)

- b. A portion of a sequential synchronous circuit is shown in below.

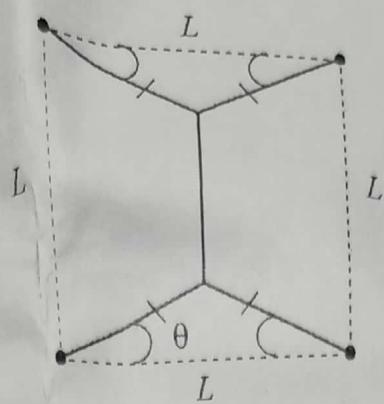


The following attributes are valid for both the flip-flops F1 and F2: setup time=25 ps and CP->Q delay=25 ps. The delay of the combinational block in the data path is 900 ps. The frequency of the Clock is 1 GHz. Ignore the delay of all the wires. Find the setup slack under the following conditions:

- Nominal delays, as shown in the figure, are considered.
- Assume that an OCV derate factor of 1.1 is added to the delay for the late paths, and 0.9 is added to the delay for the early paths.
- Assume that an OCV derate factor of 1.1 is added to the delay for the late paths, and 0.9 is added to the delay for the early paths (same as in part (ii) above). Furthermore, consider Common Path Pessimism Removal (CPPR) in the computation.

(2+4+4 Marks)

- c. Four pins are placed at the corner of a square of length L, as shown on the next page. We want to connect them using wire segments of total minimum length. The solution is given by the Steiner Minimum Tree shown in the figure (All four angles/segments marked in the figure are equal).



Derive the value of θ such that total wire length is minimum. No marks for just writing the answer, you need to derive it. (5 Marks)

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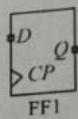
Protocol: Cache Line Characteristics

b.

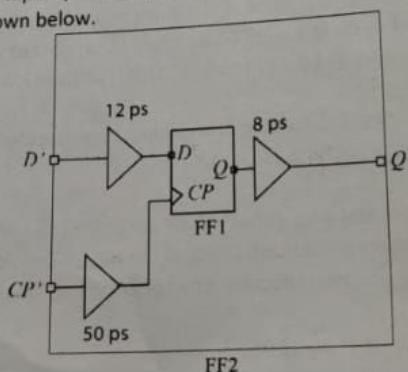
```
module top(c, en, out2);
    input c, en;
    output out2;
    reg out2;
    always @(*) begin
        if (en==1'b0)
            out2 = c;
        end
    endmodule
```

[2+2 Marks]

3. A library contains a flip-flop named FF1 (shown below) with a setup time of 20 ps, hold time of 10 ps, clock-to-Q delay of 10 ps.



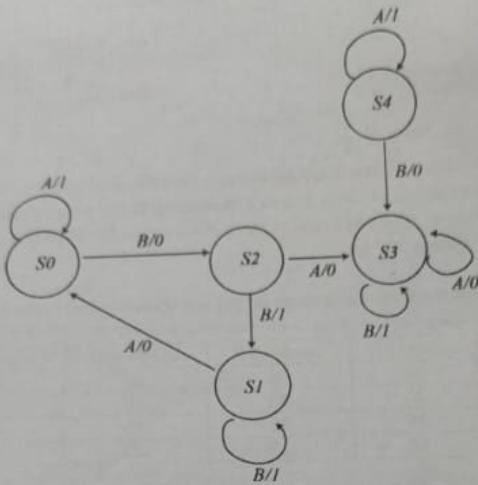
A designer made another flip-flop FF2 by reusing FF1 and adding three buffers having delays 12 ps, 8 ps, and 50 ps, as shown below.



Compute the setup time, hold time and clock-to-Q delay of FF2 (the data, clock, and Q pins of FF2 are D', CP', and Q', respectively).

[2+2+2 Marks]

4. Consider the portion of a synchronous circuit shown below.



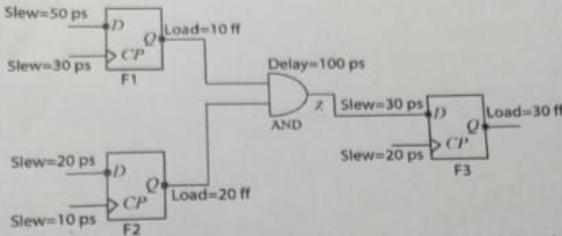
The state bits are a, b, c . The input set is $\{A, B\}$ and the output set is $\{0, 1\}$.

The state encoding is as shown in the following table.

	a	b	c
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	0	1	1
S_4	1	0	0

- a) Write the characteristics function of the set of reachable states when the starting state is S_1 .
- b) Write the characteristics function of the set of reachable states when the starting state is S_4 .

[2+2 Marks]



Assume that the clock period is 1000 ps. Assume that the arrival time of the clock signal at the clock pin of all the flip-flops is 0 ps. The signals arriving at the input of the flip-flops have slews as shown in the figure. Also, the loads at the output of the flip-flops are shown in the figure. The delay of the AND gate is 100 ps.

The NLDM table for the clock-to-Q delay (in ps) are shown below [valid for all flip-flops].

	Load=10 ff	Load=20 ff	Load=30 ff	Load=40 ff
Clk Slew=10ps	10	20	30	40
Clk Slew=20ps	20	30	40	50
Clk Slew=30ps	25	35	45	55
Clk Slew=40ps	28	38	48	58

The NLDM table for the setup time (in ps) are shown below [valid for all flip-flops].

	Clk Slew=10ps	Clk Slew=20ps	Clk Slew=30ps	Clk Slew=40ps
Data Slew=20ps	10	12	14	16
Data Slew=30ps	12	16	18	20
Data Slew=40ps	14	18	22	26
Data Slew=50ps	18	25	30	40

For data not given for the problem (such as wire delay), assume that ideal conditions exist. The setup slack is defined as the difference between the required time and the arrival time.

- a) Compute the setup slack for the path between F1 and F3.
- b) Compute the setup slack for the path between F2 and F3. [2+2 Marks]

5. The state diagram for an FSM with five states S_0, S_1, S_2, S_3 , and S_4 is shown below:

VLSI Design Flow
Mid Semester Exam (27th February 2023)

Time allowed: 1 hour

Maximum Marks: 30

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Use the marks allotted to each question as an indicator of how elaborate you need to answer.
- V. Cheating or use of unfair means will be dealt with as per institute policy.

1.
 - a. Briefly explain Optical Proximity Correction (OPC). [2 Marks]
 - b. Explain why does a designer (or verification engineer) needs to make more effort in determining the functional coverage than determining the code coverage for an RTL design written in Verilog? [2 Marks]
 - c. Explain how does SoC design methodology help in reducing design effort. [2 Marks]
 - d. A designer wants to capture within-cycle glitches for combinational circuit elements/logic in RTL simulation. Which type of simulator can be used for this purpose: event-based or cycle-based. Give reason in support of your answer. [0.5+1.5 Marks]
 - e. What is the effect of unquification in RTL synthesis? When do we want to perform unquification? [1+1 Marks]
 - f. When can you get a warning of a module being treated as black-box during elaboration? How can the problem be solved? [1+1 Marks]
2. Draw the schematic of the circuit that will be generated by the synthesis of the following Verilog codes (No need of any explanation). Label all the design entities (including pins and ports) appropriately (marks will be deducted for wrong/missing labeling).
 - a.

```
module top(a, b, s, out1);
    input a, b, s;
    output out1;
    reg out1;
    always @(*) begin
        if (s==1'b1)
            out1 = a;
        else
            out1 = b;
    end
endmodule
```

VLSI Design Flow

Mid Semester Exam (27th February 2023)

Time allowed: 1 hour

Maximum Marks: 30

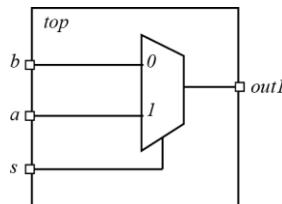
1.

- a. Optical Proximity Correction (OPC) is a Resolution Enhancement Techniques (RET) that pre-compensates a mask such that the features obtained on the mask is same as is desired. It adds appropriate serifs, hammerheads, and mouse bites to the mask and improves the resolution of photolithography by compensating errors due to diffraction etc. It can avoid problems of rounding of corners, and line end pullback when the wavelength of light used in photolithography is greater than the feature size.
- b. For performing functional coverage, a designer (or a verification engineer) needs to create a functional coverage model. This requires additional effort in determining the functional coverage of an RTL model. On the other hand, the code coverage can be determined directly by the RTL code, and does not require any extra effort from the designer.
- c. In SoC design methodology, only IP integration or IP assembly is required. The internal details of IP are already available and hence no extra effort is required in creating a complex IP. Thus, SoC design methodology help reduce design effort.
- d. Event-based simulator should be used. An event-based simulator can capture events or changes in the signal within a clock cycle for combinational circuit elements. Hence, it can capture within-cycle glitches. A cycle-based simulator only computes values at clock edges. Hence, it will miss within-cycle glitches.
- e. Uniquification creates separate copies of the module for different instances. It is required when we want different instances of the same module to be synthesized differently.
- f. We can get a warning of a module being treated as black-box during elaboration when we instantiate a module in the model, while the definition of that module is missing. We can fix this problem by providing definition (or including the module or its file) that is missing.

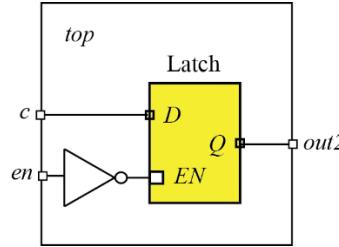
[2+2+2+2+2+2 Marks]

2.

a.



b.



3. Setup time = $20 + 12 - 50 = -18 \text{ ps}$

Hold time = $10 - 12 + 50 = 48 \text{ ps}$

Clock-to Q delay = $10 + 50 + 8 = 68 \text{ ps}$

4.

	Load=10 ff	Load=20 ff	Load=30 ff	Load=40 ff
Clk Slew=10ps	10	20	30	40
Clk Slew=20ps	20	30	40	50
Clk Slew=30ps	25	35	45	55
Clk Slew=40ps	28	38	48	58

	Clk Slew=10ps	Clk Slew=20ps	Clk Slew=30ps	Clk Slew=40ps
Data Slew=20ps	10	12	14	16
Data Slew=30ps	12	16	18	20
Data Slew=40ps	14	18	22	26
Data Slew=50ps	18	25	30	40

a) Path between F1 and F3.

Setup time of F3 = 16 ps

Clock to Q delay of F1 = 25 ps

Arrival Time = $25 + 100 \text{ ps} = 125 \text{ ps}$

Required Time = $1000 - 16 \text{ ps} = 984 \text{ ps}$

Slack = $984 - 125 = 859 \text{ ps}$

b) Path between F2 and F3.

Setup time of F3 = 16 ps

Clock to Q delay of F2 = 20 ps

Arrival Time = $20 + 100 \text{ ps} = 120 \text{ ps}$

Required Time = $1000 - 16 \text{ ps} = 984 \text{ ps}$

Slack = $984 - 120 \text{ ps} = 864 \text{ ps}$

5.

a) The set of reachable states is $\{S_1, S_0, S_2, S_3\}$. And the characteristics functions is:

$$a'b'c' + a'b'c + a'bc' + a'bc$$

b) The set of reachable states is $\{S_4, S_3\}$. And the characteristics functions is: $ab'c' + a'bc$

VLSI Design Flow

Mid Semester Exam (2nd March 2024)

Maximum Marks: 30

Time allowed: 1 hour

Note:

- I. All questions are compulsory.
- II. Marks are indicated in bold at the end of each question.
- III. Be crisp and precise in your answer so that you can complete the answers in 1 hour.
- IV. Cheating or use of unfair means will be dealt with as per institute policy.

1.
 - a. What are inputs and outputs of Behaviour Synthesis or High-level Synthesis from the perspective of VLSI Design Flow? [2 Marks]
 - b. What do you understand by the Engineering Change Order (ECO) fixes/changes in VLSI Design Flow? [2 Marks]
 - c. What is the effect of increasing the area of a die on the yield of manufacturing that die? Give reason in support of your answer. [0.5+1.5 Marks]
 - d. Which of the two types of RTL simulator (cycle-based or event-based) can report within-cycle glitches for combinational circuit elements/logic. Give reason in support of your answer. [0.5+1.5 Marks]
 - e. What is the typical effect of reducing the slew at the data pin of a D flip-flop in a technology library on: A) setup-time of that flip-flop B) clock-to-Q delay of that flop-flip. [1+1 Marks]

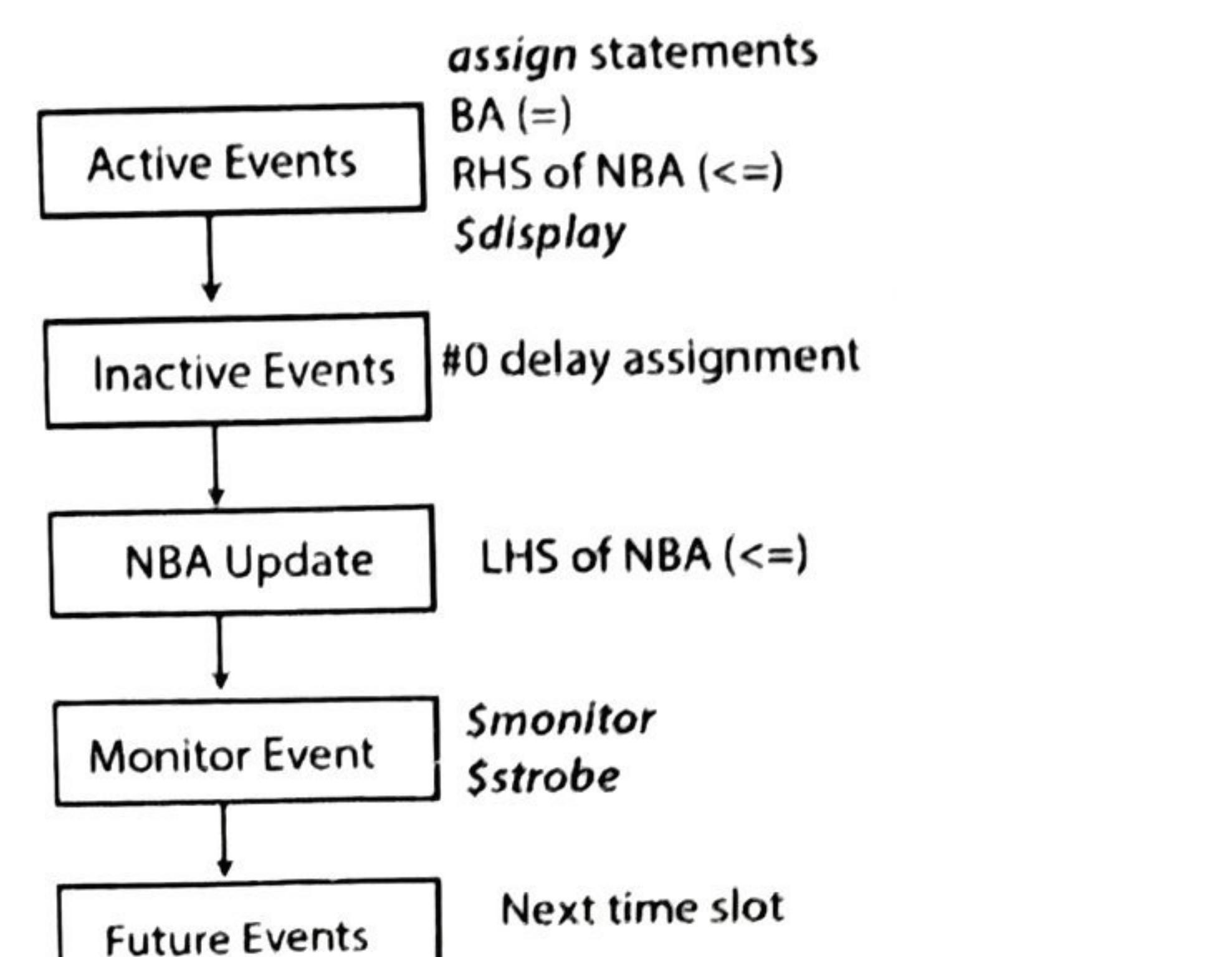
2. Consider the following piece of Verilog code. What will be the output when simulation is performed? Give a very brief explanation for your answer.

```
module top();
    reg a, b;

    initial begin
        a = 1'b1;
        a <= 1'b0;
        b = a;
        b <= a;

        $display("Display a=%b b=%b", a, b);
        $monitor("Monitor a=%b b=%b", a, b);

    end
endmodule
```



The stratified Verilog event queue is shown for your convenience.

[4 Marks]

3. Draw the schematic of the typical circuit that will be generated by an RTL synthesis tool for the following Verilog codes (No need of any explanation). Label all the design entities (including pins and ports) appropriately (marks will be deducted for wrong/missing labeling). [3+3 Marks]

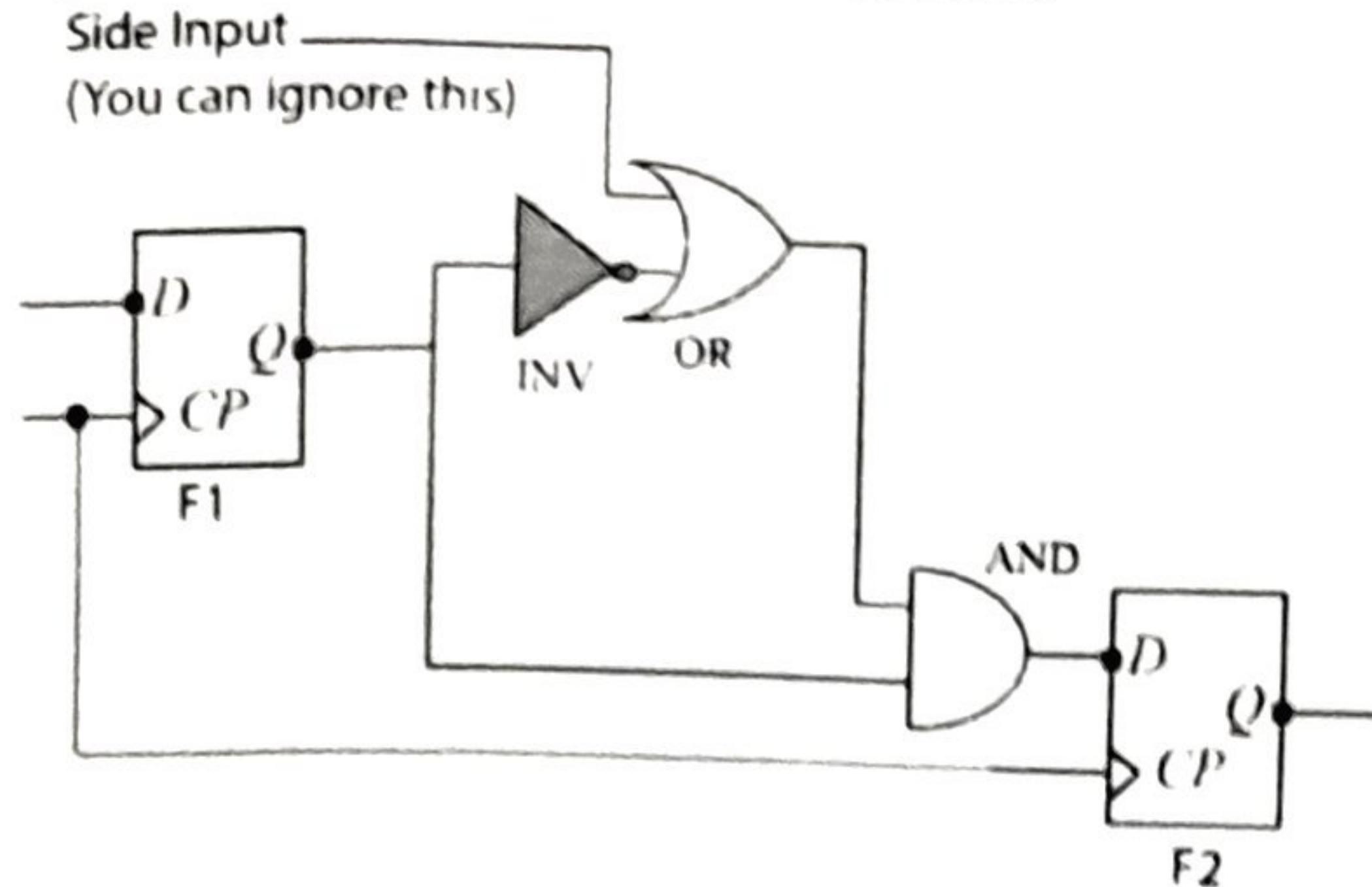
a.

```
module top(clk, in1, out1);
    input clk;
    input [1:0]in1;
    output [1:0]out1;
    reg [1:0]cur_state;
    reg [1:0]next_state;
    always @(posedge clk) begin
        cur_state <= next_state;
    end
    always @* begin
        case (in1)
            2'b00 : next_state = 2'b00;
            2'b01 : next_state = 2'b01;
            2'b10 : next_state = 2'b10;
            2'b11 : next_state = 2'b11;
        endcase
    end
    always @* begin
        out1 <= cur_state;
    end
endmodule
```

b.

```
module top(clk, in, out);
    input clk;
    input in;
    output out;
    reg [3:0]q;
    reg i;
    always @(posedge clk) begin
        for (i=0; i<4; i=i+1) begin
            if (i == 0) begin
                q[i] <= in;
            end else begin
                q[i] <= q[i-1];
            end
        end
    end
    always @* begin
        out = q[3];
    end
endmodule
```

4. Consider the portion of a synchronous circuit shown below.



Assume that the clock period is 1000 ps. Assume that the arrival time of the clock signal at the clock pin of all the flip-flops is 0 ps. For data not given for the problem (such as wire delay), assume that ideal conditions exist.

Assume that:

For the flip-flop F1: setup time = 22 ps, hold time = 12 ps, clock to Q delay = 17 ps

For the flip-flop F2: setup time = 37 ps, hold time = 15 ps, clock to Q delay = 34 ps

For the AND gate: delay = 23 ps

For the OR gate: delay = 44 ps

For the inverter: delay = 14 ps.

Consider the timing paths between F1 and F2. Compute the a) setup slack at F2 and b) hold slack at F2. [2+2 Marks]

5. Consider the following two Verilog netlists:

```
module top(in1, in2, in3, in4, clk, out1);
    input in1, in2, in3, in4, clk;
    output out1;
    wire y1;
    wire y2;
    wire z1;
    wire q1, q2;
    NAND2 N1( .A1(in1), .A2(in2), .ZN(y1));
    BUF B1 ( .I(in3), .Z(y2));
    DFF F1 (.CLK(clk), .D(y1), .Q(q1));
    DFF F2 (.CLK(clk), .D(y2), .Q(q2));

    NAND2 N2( .A1(q1), .A2(q2), .ZN(z1));
    NAND2 N3( .A1(z1), .A2(in4), .ZN(out1));
endmodule
```

```
module top(in1, in2, in3, in4, clk, out1);
    input in1, in2, in3, in4, clk;
    output out1;
    wire y1;
    wire y2;
    wire z1;
    wire q1, q2;
    NAND2 N1( .A1(in1), .A2(in2), .ZN(y1));
    INV I1 ( .I(in3), .ZN(y2));
    DFF F1 (.CLK(clk), .D(y1), .Q(q1));
    DFF F2 (.CLK(clk), .D(y2), .Q(q2));

    NAND2 N2( .A1(q1), .A2(q2), .ZN(z1));
    NAND2 N3( .A1(z1), .A2(in4), .ZN(out1));
endmodule
```

The cells DFF, NAND2, BUF, and INV are D flip-flop, NAND gate, buffer and inverter, respectively.

These cells have typical pin names found in libraries. These two netlists are subjected to combinational equivalence checking (CEC). The ports and registers are matched by names.

- Draw the schematic of both the netlists. Label the ports and instances (no other label needed). [2 Marks]
- Draw the schematic of all the miters separately that the CEC tool will internally create. Label the ports and instances (no other label needed). [3 Marks]
- Which of the miters drawn above will show inequivalence? Give the input pattern that will cause that miter to indicate inequivalence. [1 Marks]

VLSI Design Flow

Mid Semester Exam (2nd March 2024)

Time allowed: 1 hour

Maximum Marks: 30

1.

- a. Inputs:
- Algorithm or Design in C/C++/SystemC/MATLAB, High-level Programming Language
 - Constraints (Frequency, Latency, Area, Power etc.) and list of resources that can be used
- Output: RTL in Verilog or VHDL **[0.5+0.5+1 Marks]**
- b. ECO involves making small final fixes/changes in the design at the last stages of a design flow. **[2 Marks]**
- c. Increasing the area of a die reduces the yield of manufacturing that die. With increased area the probability of introducing at least one fatal random defect on the given die increases, which will reduce the yield. **[0.5+1.5 Marks]**
- d. Event-based simulator should be used. An event-based simulator can capture events or changes in the signal within a clock cycle for combinational circuit elements. Hence, it can capture within-cycle glitches. A cycle-based simulator only computes values at clock edges. Hence, it will miss within-cycle glitches. **[0.5+1.5 Marks]**
- e.
- Setup-time of the flip-flop will decrease
 - Clock-to-Q delay of the flop-flip is not impacted by the slew at the D-pin **[1+1 Marks]**

2. Output will be:

Display a=1 b=1

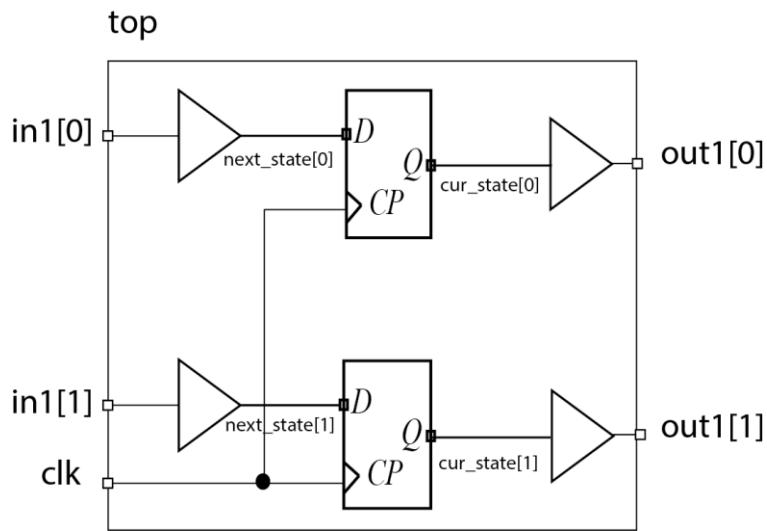
Monitor a=0 b=1

The two blocking assignments will be executed before the display statement.

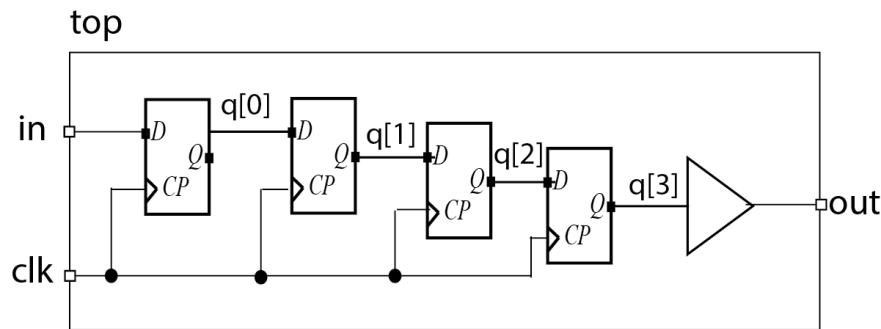
The LHS of non-blocking assignment will be executed before the monitor statement. The values that are assigned by NBA was pre-determined while executing the RHS of NBA. Hence b gets the old value of a. **[1.5+0.5+1.5+0.5 Marks]**

3.

a.



b.



4.

a) Taking maximum arrival time = $17 + 14 + 44 + 23 \text{ ps} = 98 \text{ ps}$

Required Time = $1000 - 37 \text{ ps} = 963 \text{ ps}$

Slack = RT-AT=963-98=865 ps

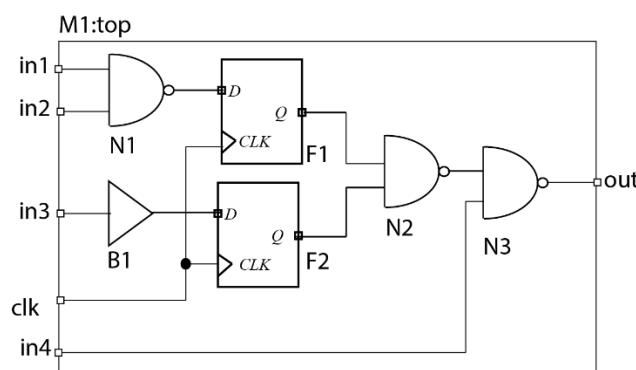
b) Taking minimum arrival time = $17 + 23 \text{ ps} = 40 \text{ ps}$

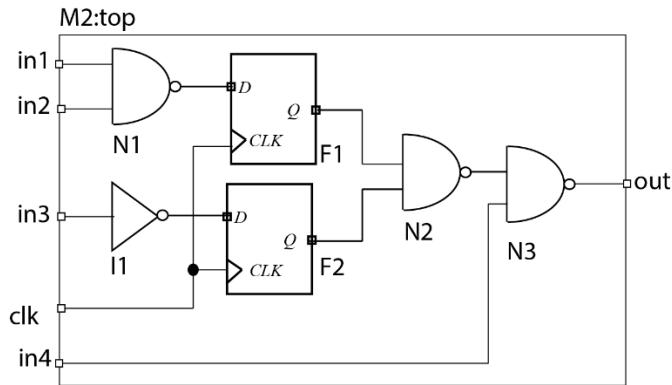
Required Time = 15 ps

Slack = AT-RT=40-15=25 ps [2+2 Marks]

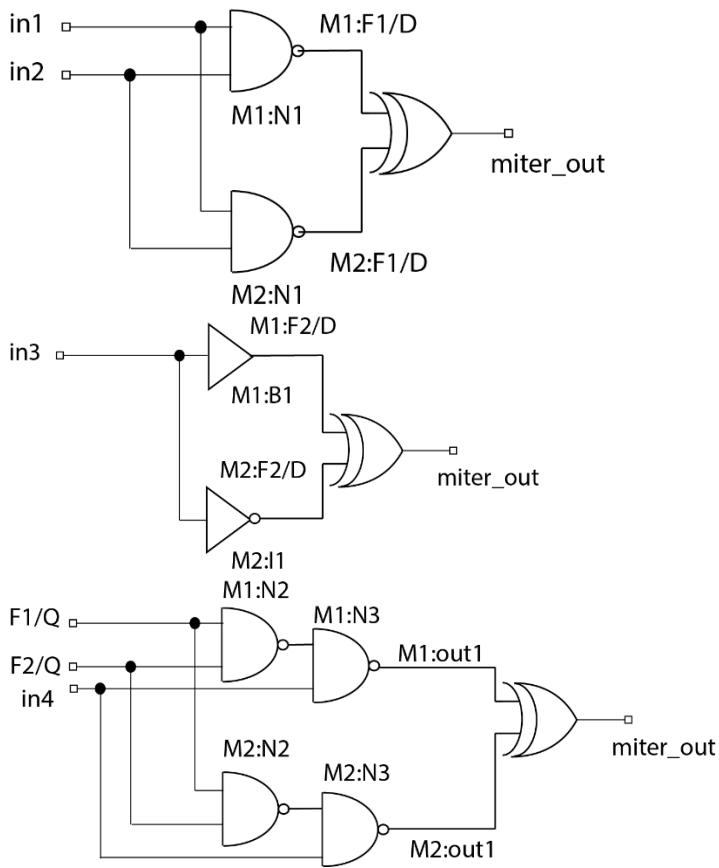
5.

a)





b)



- c) Second miter will fail. The input pattern is in1=X, in2=X, in3=0, in4=X or in1=X, in2=X, in3=1, in4=X

VLSI Design Flow

End Semester Exam (6th May 2024)

Time allowed: 2 hours

Maximum Marks: 80

Note:

- I. **Marks are indicated in bold at the end of each question.**
- II. **There are 5 questions of 15, 15, 10, 20 and 20 marks. All questions are compulsory.**
- III. **Be crisp and precise in your answer so that you can complete the answers in 2 hours.**
- IV. **Cheating or using unfair means will be dealt with as per institute policy.**

1.

- a. Regarding the semiconductor business ecosystem, answer the following questions:
 - i. What are fabless design companies?
 - ii. How can merchant foundries, such as TSMC, become profitable despite having a huge capital cost?
 - iii. What is the role of PDKs in ensuring that the layout produced (designed) by a fabless design company is profitably manufactured by a given merchant foundry? **[2+2+2 Marks]**
- b. Regarding photolithography, answer the following questions:
 - i. What is the role of mask in photolithography?
 - ii. How does OPC help in improving the resolution of photolithography? **[2+2 Marks]**
- c. How does SoC-based design methodology improve a designer's productivity? **[2 Marks]**
- d. What is the package's role in managing a chip's thermal profile? **[2 Marks]**
- e. What information does a GDS file contain? **[1 Mark]**

2.

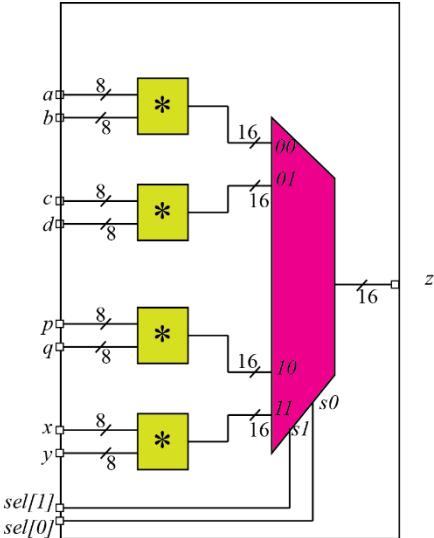
- a. Consider the following Verilog module.

```
module top(in1, in2, clk, out);  
  
    input in1, in2, clk; output out;  
    reg q1, q2;  
  
    always @ (posedge clk) q1 <= !(in1 & in2);  
    always @ (posedge clk) q2 <= (in1 & in2);  
    always @* out = !(q1 & q2);  
endmodule
```

Draw the schematic of the synthesized netlist and mark the circuit elements. Assume that the library used in synthesis contains only the following circuit elements: inverter, two-input NAND gate, and D flip-flop. **[4 Marks]**

- b. Consider the unoptimized netlist (circuit) generated by an RTL synthesis tool shown alongside. The numbers on the nets indicate the number of lines in a bus. The multiplexer selects one of the four buses based on the select lines s_0 and s_1 . The elements marked * are multipliers.

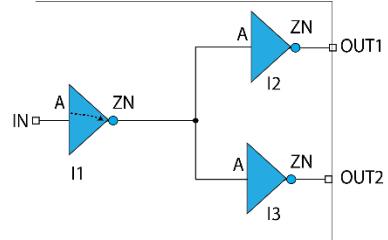
Redraw the circuit with resource sharing that minimizes the circuit area (**mark the number of lines in each bus**). Assume that the area of a multiplier is significantly higher than the multiplexers. Hence, the number of multipliers needs to be minimized. Increasing the number of multiplexers is permitted. Further, assume that the timing constraints are relaxed. **[4 Marks]**



- c. Consider the circuit shown alongside. It consists of instances of three **identical** inverters. The input capacitance of the pin A for each inverter is 10 fF . The NLDM table for the timing arc $A \rightarrow ZN$ for the inverter is also shown below the circuit.

The minimum and maximum transition time at the input port IN are 10 ps and 20 ps , respectively. Ignore net capacitances. Compute

- Delay of the arc $A \rightarrow ZN$ for the instance I_1 for the setup analysis
- Delay of the arc $A \rightarrow ZN$ for the instance I_1 for the hold analysis



	$C=10 \text{ fF}$	$C=20 \text{ fF}$	$C=50 \text{ fF}$
10 ps	20	30	60
20 ps	30	45	75
100 ps	60	75	90

[2+2 = 4 Marks]

- d. The ROBDD for a Boolean function of 7 variables is a leaf vertex labeled 1. Is this function satisfiable? Explain your answer. **[0.5+0.5=1 Mark]**
- e. Consider combinational equivalence checking (CEC) of two purely combinational circuit (i.e. a circuit that does not contain any flip-flops or latches).
- Which types of design entities are treated as **matching points** for these circuits (i.e., the design entities whose matching will be done by the CEC tool)?
 - Which types of design entities are treated as **compare points** for these circuits (i.e., design entities where equivalence will be established by the CEC tool by creating miters)? **[2 Marks]**

3.

- Name the type of unate-ness for the following logic gates: i) NAND ii) NOT **[0.5+0.5=1 Mark]**
- Name any one tool (can be open-source or commercial) that is used for i) combinational equivalence checking ii) automatic test pattern generation iii) clock tree synthesis iv) RTL simulation **[0.5+0.5+0.5+0.5=2 Marks]**

- c. Why do we typically not focus on hold violation during logic synthesis? **[2 Marks]**
- d. Write a UNIX command for doing the following i) going to a parent directory from any given directory ii) searching all the occurrences of the word “port” in a Verilog file “test.v” **[1+1=2 Marks]**

- e. Write an SDC command to create a clock named “CLOCK” on a pin named “Gen/Clk” with a period of 1000 ps and 50% duty cycle. Assume that the unit for time in the SDC file is ps. **[1 Mark]**

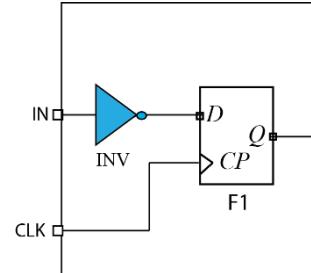
- f. Answer the following questions based on the report shown alongside. It was generated by an open-source STA tool:

Startpoint: F1 (rising edge-triggered flip-flop clocked by CLK)
 Endpoint: F2 (rising edge-triggered flip-flop clocked by CLK)
 Path Group: CLK
 Path Type: max

- (i) Name of the capture flip-flop (ii) Whether the timing analysis is for the setup constraint or the hold constraint? **[1+1=2 Marks]**

4.

- a. Consider the following portion of a circuit shown alongside. The delay of the inverter is 100 ps. The setup and hold time of the flip-flop F1 is 50 ps and 20 ps, respectively. The following constraints are given in the SDC file.

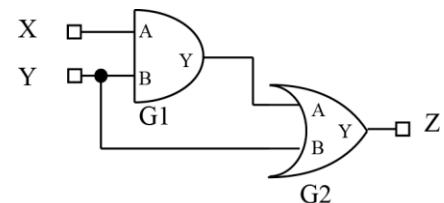


```
create_clock -name CLK -period 1000 [get_ports CLK]
set_input_delay 100 -min -clock [get_clocks CLK] [get_ports IN]
set_input_delay 500 -max -clock [get_clocks CLK] [get_ports IN]
```

Compute the setup and hold slack at the flip-flop F1. Ignore wire delays. **[2+2 Marks]**

- b. Consider the circuit shown alongside.

- i. How many fault sites are there in the circuit for single stuck-at faults? (Just give the number)
- ii. Determine the test pattern for SA0 at G2/A.
- iii. Using the results of the above question, transform the given circuit to reduce area and draw its schematic representation.
- iv. Consider CEC for the given circuit and the circuit you have drawn in the above question. Draw the miter circuit employed for carrying out CEC.
- v. What is the output of the above miter circuit for various input values? Using this observation, comment on the functional equivalence of the given and the transformed circuits. **[1+2+2+2+1 Marks]**



- c. What do you understand by the recovery time constraints for a flip-flop having an asynchronous reset pin? **[2 Marks]**
- d. What is aliasing in signature analysis for a BIST? **[2 Marks]**

- e. Why do we typically route power lines on the higher layer of the interconnect stack? [2 Marks]
- f. What is the motivation for adding spare cells in a design? [2 Marks]

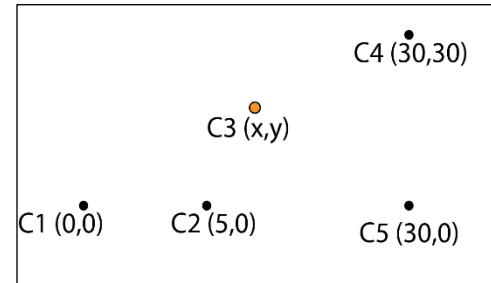
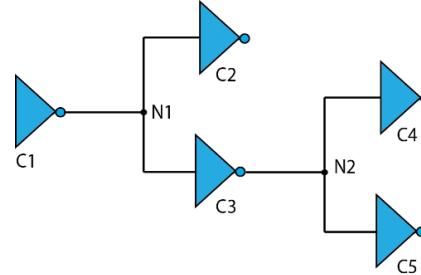
5.

- a. Consider the portion of a netlist shown alongside. The five cells C_1, C_2, C_3, C_4 , and C_5 are connected using two nets N_1 and N_2 .

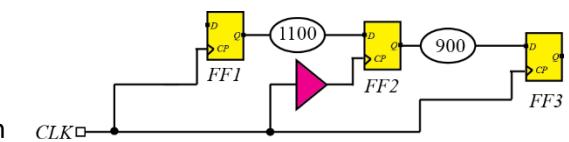
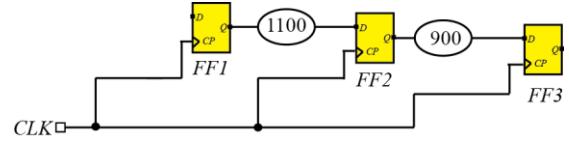
Each cell is treated as a point object during placement. The location of the cells on the layout (X and Y coordinates) is also shown alongside.

The location of C_3 is unknown and marked as (x,y) . The half perimeter wirelength estimate of the net N_1 is 20 units and of the net N_2 is 45 units. Given that: $5 \leq x \leq 30$ and $0 \leq y \leq 30$, determine x and y . {Hint: For a net with multiple pins at (x_i, y_i) , HPWL estimate is $[MAX(x_i) - MIN(x_i)] + [MAX(y_i) - MIN(y_i)]$ }

[3+3 Marks]



- b. Consider the most critical portion of a synchronous sequential circuit shown alongside. The combinational circuit elements shown in the figure have a delay of 1100ps and 900ps. Assume that the setup time and clock-to-Q delay of all the flip-flops are zero. Ignore wire delays. What is the minimum clock period at which the circuit can operate? [2 Marks]
- c. This is a continuation of the above question. A designer wishes to increase the maximum operable frequency of the circuit by adding a single buffer, as shown in the figure alongside. There are three buffers in the library of delay: 50 ps, 100 ps, and 150 ps. The designer tries these buffers one by one. Evaluate separately the minimum clock period the circuit can operate for each buffer. [2+2+2 Marks]



Using the above evaluations, determine which buffer should be inserted to obtain the maximum operable frequency and also compute the maximum operable frequency of the circuit? [1+1=2 Marks]

- d. Explain how self-healing of the electromigration effect can occur in the clock lines or nets. [2 Marks]
- e. Why do we insert redundant vias in a design? [2 Marks]