DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

MONSOON Semester | ECE 315/ ECE515: Analog CMOS Circuit Design | 2023 – 2024

Time: 1 hour | **Mid-Semester Exam-Late** | **M.M.: 25**

Instructions: All questions carry sufficient information. **No further information will be provided during the exam.** Please answer all parts of the same question together at the same place, not here and there.

1. For the circuit shown in Fig. 1, the bias current must be $I_{bias} = 0.5$ mA. Assume $\mu C_{ox} = 100\ \mu A/V^2$, $V_{TH} = 0.4$ V.
   (a) Neglecting channel-length modulation, compute the required value of V_{b2} for both the transistors to be in saturation. **[3+3]**
   (b) What is the minimum tolerable value of V_{b1} if M_2 must remain in saturation?

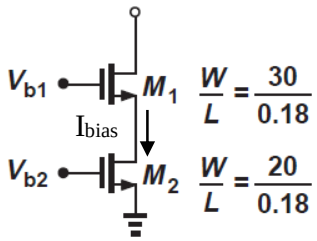

Fig. 1

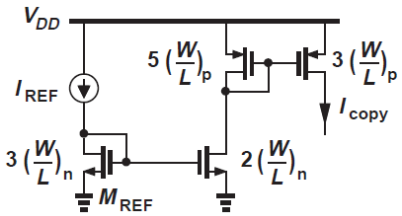

Fig. 2

2. (a) Calculate I_{copy} for the circuit shown in Fig. 2. Assume all of the transistors operate in saturation.
   (b) Calculate the small voltage gain of the circuit shown in Fig. 3. Assume $\lambda = 0$ for M_1 and M_3 but $\lambda \neq 0$ for M_2. Also assume $\gamma = 0$ for all the transistors. **[3+4]**

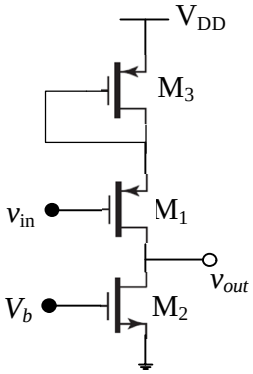

Fig. 3

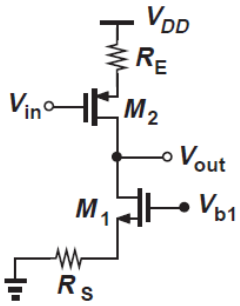

Fig. 4

3. (a) Assuming all the MOSFETs in Fig. 4 are in saturation and $\lambda \neq 0$, $\gamma = 0$, calculate the small-signal voltage gain of the circuit. **[5+1+1]**
   (b) Why do current mirrors usually employ same length for the transistors in its circuit? Explain briefly in 2-3 sentences.
   (c) Out of the following four single-stage MOS amplifiers with resistive loads, which one gives the voltage gain less than unity?
   (i) common-source, (ii) common-gate, (iii) common-drain, (iv) common-source with source degeneration

4. (a) Determine the output impedance of the stage shown in Fig. 5. Assume all of the transistors operate in saturation, $\lambda \neq 0$, $\gamma = 0$ and $g_m r_o >> 1$. **[4]**

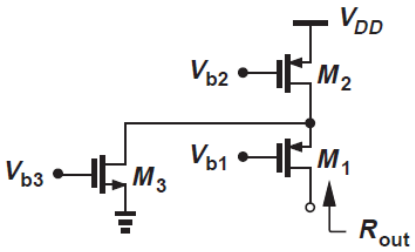

Fig. 5