VLSI Design Flow

Mid Semester Exam (8th March 2021)

Time allowed: 1 hour *Maximum Marks: 40*

1.

a)

Let N functions be implemented in hardware.

Total cost = 1000+N*400

To meet cost constraint

1000+N*400 < 2500

N < 3.75

Maximum N=3

The three functions that take maximum percentage of time are moved to dedicated hardware are: F6, F8 and F3. 2 Marks

Cost = 1000+3*400=Rs 2200/- 1 Mark

Runtime of functions implemented in software = 0.30*1000=300 s

Runtime of functions implemented using dedicated hardware = (1/10)*0.70*1000=70 s

Total runtime = 300+70=370 s. 2 Marks

b) Since runtime with 3 functions moved to dedicated hardware is 370 s (more than target of below 350), we need to move more function to dedicated hardware.

Let us move 4th top function F5 to dedicated hardware that consumes 10% of total runtime.

Total runtime = 0.20*1000+(1/10)*0.80*1000=200+80=280 s.

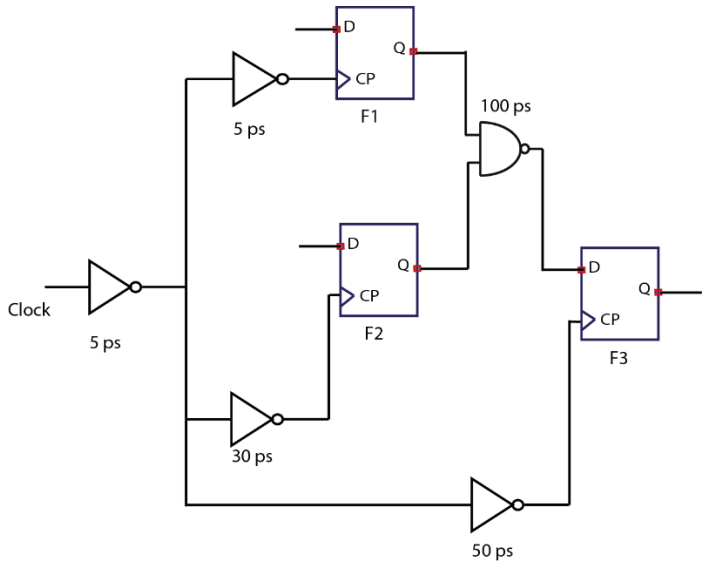
So we need to move F6, F8, F3, and F5 to dedicated hardware. 2 Marks

Runtime = 280 s 1 Mark

Cost = 1000+4*400=Rs. 2600/- 2 Marks

2.

(a)



Clock-frequency $= 1\ GHz$
Time period $= 10^{-9}s = 1000\ ps$

Setup analysis

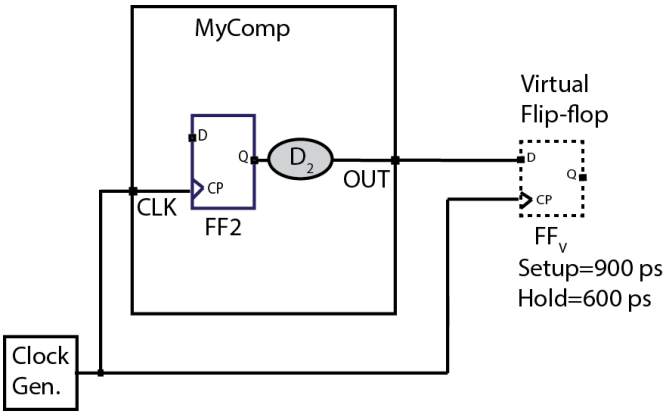
Path from F1 to F3:
Setup Slack: (1000+5+50)-(5+5+50+100+30)=865 ps 1.5 Marks
Path from F2 to F3:
Setup Slack: (1000+5+50)-(5+30+50+100+30)=840 ps 1.5 Marks
Therefore, the worst setup slack is 840 ps (F2 to F3) 1 Mark

Hold analysis

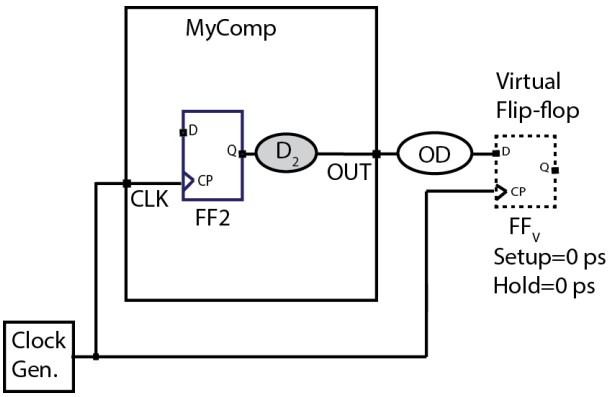
Path from F1 to F3:
Hold Slack: (5+5+50+100)-(5+50+10)=95 ps 1.5 Marks
Path from F2 to F3:
Hold Slack: (5+30+50+100)-(5+50+10)=120 ps 1.5 Marks
Therefore, the worst hold slack is 95 ps (F1 to F3) 1 Mark

(b)

The requirement is similar if we consider a flip-flop at the output port with a setup and hold times of 900 ps and 600 ps, as follows:



This situation needs to be modelled using SDC set_output_delay which works as follows:



The above two figures should yield the same constraint or requirement.

To make them same, we need to find adjust the delay of the element OD for the maximum case (setup) and the minimum case (hold).

For setup analysis:

From first figure:

$T_{FF} + T_{D2,max} + 900 < T_{period}$

From second figure:

$T_{FF} + T_{D2,max} + T_{OD,max} < T_{period}$

Therefore: $T_{OD,max}$ =900 ps 1 Marks

For hold analysis:

From first figure:

$T_{FF} + T_{D2,min} > 600$

$T_{FF} + T_{D2,min} - 600 > 0$

From second figure:

$T_{FF} + T_{D2,min} + T_{OD,min} > 0$

Therefore: $T_{OD,min}$ =-600 (Note the negative sign). 3 Marks

We need to find the value of delay

The SDCs are:

create_clock -name SYS CLOCK -period 2000 [get ports CLK] 1 Mark

set output delay 900 -max -clock [get clocks SYS CLK] [get ports OUT]
set output delay -600 -min -clock [get clocks SYS CLK] [get ports OUT]

2 Marks

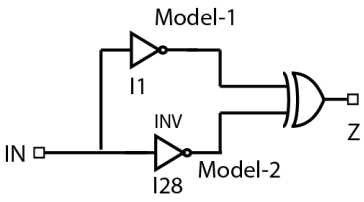
-0.5 if -clock option is missing

3.

a)

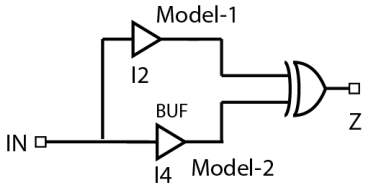
Each of the following four miters need to be drawn separately to get marks.
Specifically, the inputs and instance name should be marked correctly in each miter and an XOR gate must be placed at the output.

Miter-1



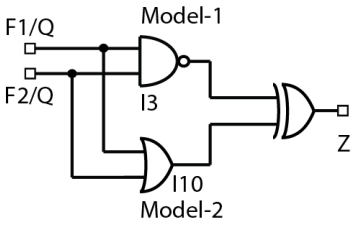
1 Mark

Miter-2



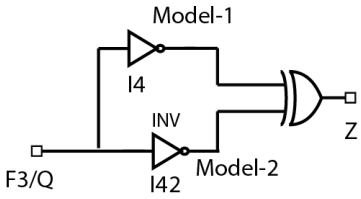
1 Mark

Miter-3



1 Mark

Miter-4



1 Mark

b) The Miter-3 will show failure because output can be made 1. 2 Marks

The patterns at inputs that satisfy the miter (or make the models inequivalent or fail) are: $F1/Q=0,F2/Q=0$ and $F1/Q=1,F2/Q=1$. 3 Marks

c) No, these are invalid patterns, because F1/D is the complement of F2/D. Therefore, the possible values of {F1/Q,F2/Q} are {01} and {10}. Therefore, {00} and {11} cannot occur. Thus, it is a false failure. 6 Marks