

INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI
ECE 315/515 ANALOG CMOS
END-TERM EXAMINATION

Date: DECEMBER 2, 2025 Max. Marks: 100 Time: 9:30 AM to 11:30 AM

Note:

- PLEASE READ THE INSTRUCTIONS CAREFULLY. ANY NON-ADHERENCE TO INSTRUCTIONS WILL BE CONSIDERED AS CHEATING.
- THERE ARE FOUR PAGES IN THE QUESTION PAPER. ANSWER ANY FIVE OUT OF SEVEN QUESTIONS.
- ALL QUESTIONS CARRY EQUAL MARKS.
- No Mobile Phones, laptop or solution manual/or its print out will be permitted in the examination hall.
- It is a CLOSED BOOK TEST AND NO NOTES OR BOOKS ARE ALLOWED.
- The only person you are allowed to talk to is your invigilators.
- Any rough work should be done in the answer script and submitted. You are not permitted to take your rough work outside the examination hall.

1. Calculate the transfer function $v_{out}(s)/v_{in}(s)$ for the circuit shown in Fig. 1. The W/L of M1 is $2\mu\text{m}/0.8\mu\text{m}$ and the W/L of M2 is $4\mu\text{m}/4\mu\text{m}$. Note that this is a small signal analysis and the input voltage v_{IN} has a dc value of 2 volts and ac signal of 1 mV(rms). [20 Marks]

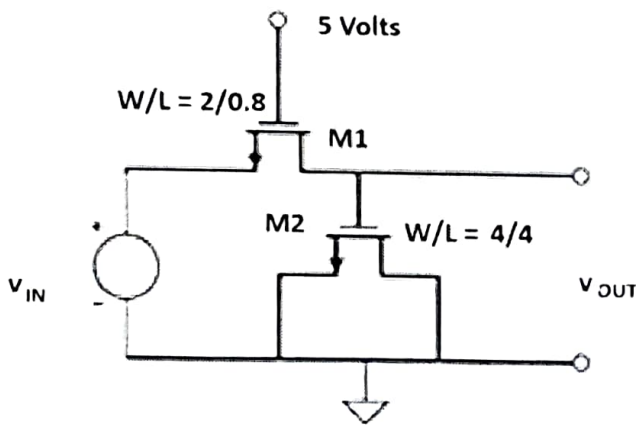


Figure 1

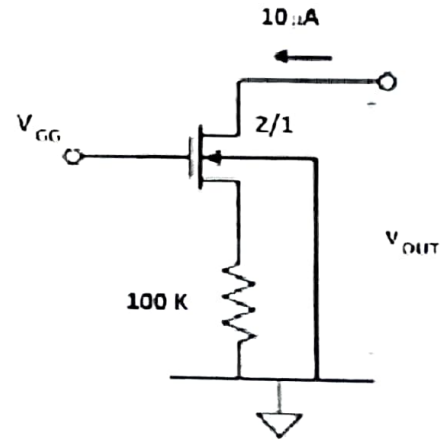


Figure 2

2. Figure 2 illustrates a source-degenerated current source. Using Table 1 model Parameters, calculate the output resistance at the given current bias. [20 Marks]
3. An improved bandgap reference generator is illustrated in Fig. 3. Assume that the devices M1 through M5 are identical in W/L. Further assume that the area ratio for the bipolar transistors is 10:1. Design the components to achieve an output reference voltage of 1.262 V. Assume that the amplifier is ideal. What advantage, if any, is there in stacking the bipolar transistors? [20 Marks]

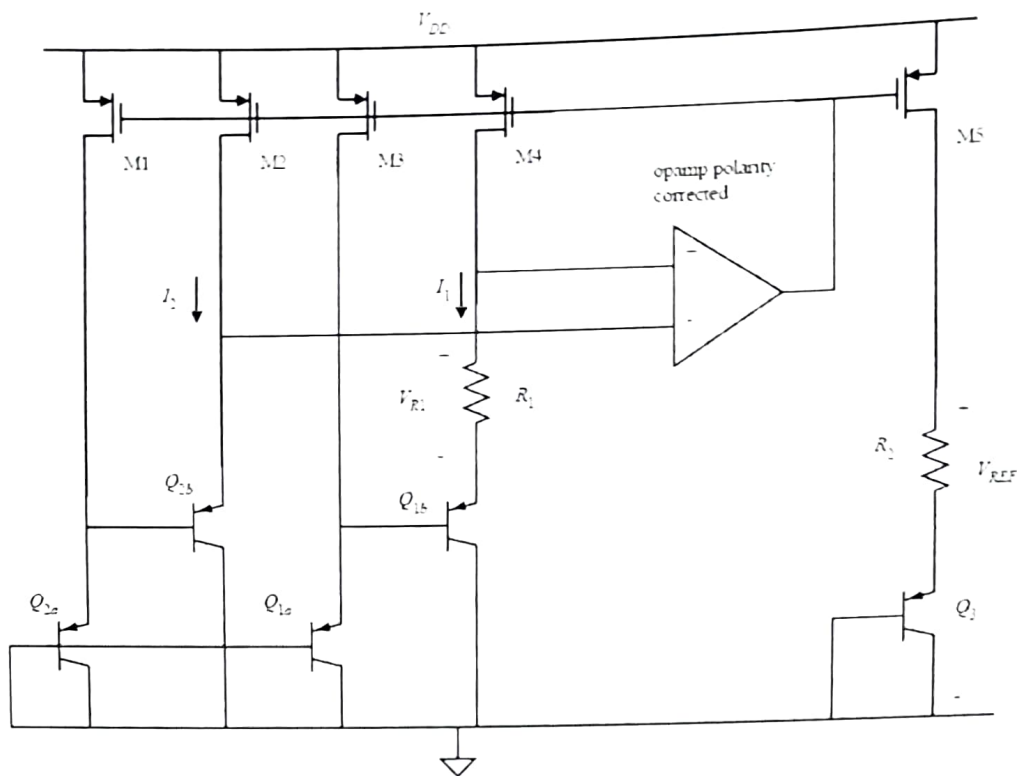


Figure 3

4. A CMOS amplifier is shown in Fig. 4. Assume M1 and M2 operate in the saturation region.
- What value of V_{GG} gives $100\mu A$ through M1 and M2?
 - What is the DC value of V_{IN} ?
 - What is the small signal voltage gain, v_{out}/v_{in} , for this amplifier?
 - What is the -3dB frequency in Hz of this amplifier if $C_{gd1} = C_{gd2} = 5fF$, $C_{bd1} = C_{bd2} = 30fF$, and $C_L = 500fF$?
- [20 Marks]**

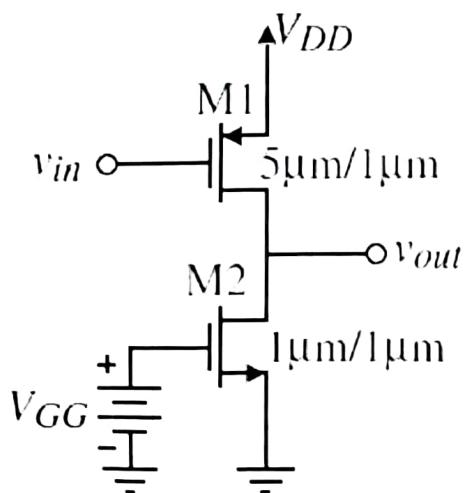


Figure 4

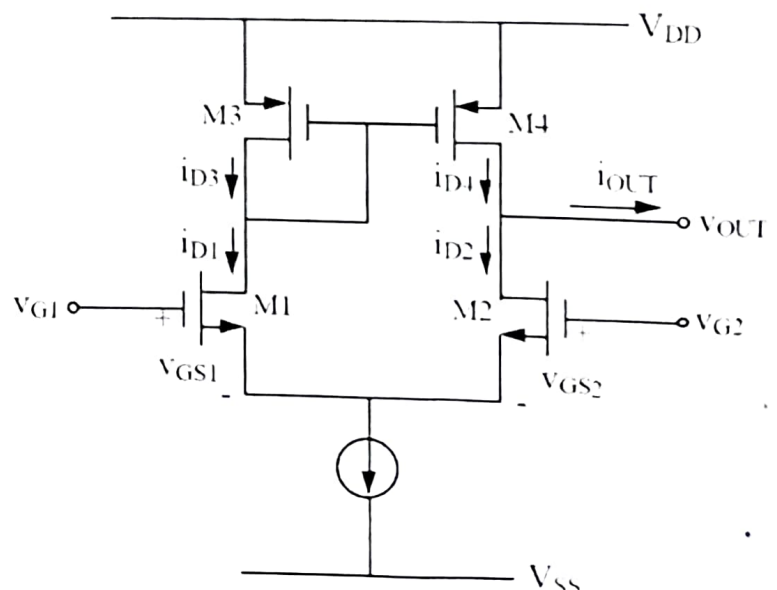


Figure 5

5. If all the devices in the differential amplifier of Fig. 5 are saturated, find the worst-case input offset voltage, V_{OS} , if $|V_{Ti}| = 1 \pm 0.01$ volts and $\beta_i = 10^{-5} \pm 5 \times 10^{-7}$ amperes/volt². Assume that $\beta_1 = \beta_2 = 10 \beta_3 = 10 \beta_4$ and

$$\frac{\Delta\beta_1}{\beta_1} = \frac{\Delta\beta_2}{\beta_2} = \frac{\Delta\beta_3}{\beta_3} = \frac{\Delta\beta_4}{\beta_4}$$

Carefully state any assumptions that you make in working out this problem. [20 Marks]

6. Use the Miller simplification on the capacitor C_2 of Fig. 6 and derive an expression for the pole, p_1 , assuming that the reactance of C_2 at the frequency of interest is greater than R_3 . [20 Marks]

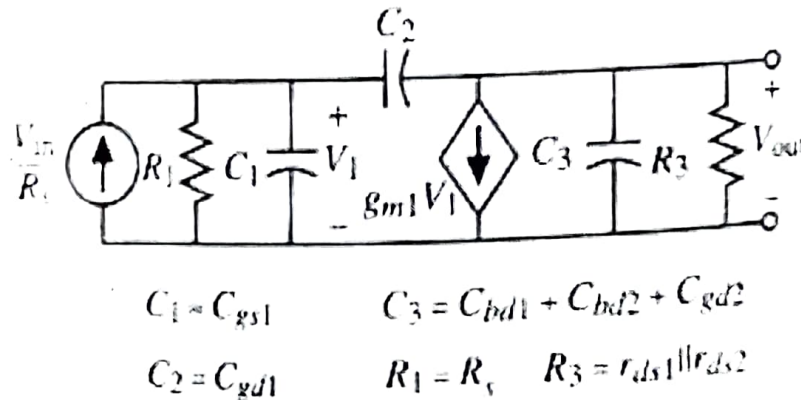


Figure 6

7. A two-stage, Miller-compensated CMOS op amp has a RHP zero at $20GB$, a dominant pole due to the Miller compensation, a second pole at p_2 and a mirror pole at $-3GB$.
- If GB is 1MHz, find the location of p_2 corresponding to a 45° phase margin.
 - Assume that in part (a) that $|p_2| = 2GB$ and a nulling resistor is used to cancel p_2 . What is the new phase margin assuming that $GB = 1$ MHz?
 - Using the conditions of (b), what is the phase margin if C_L is increased by a factor of 4?
- [20 Marks]

Table 1

Parameter SymbolGB	Parameter Description	Typical Parameter Value		Units
		n-channel	p-channel	
V_{TO}	Threshold voltage ($V_{BS} = 0$)	0.7 ± 0.15	0.7 ± 0.15	V
κ'	Transconductance parameter (in saturation)	$110.0 \pm 10\%$	$50.0 \pm 10\%$	$\mu\text{A}/\text{V}^2$
γ	Bulk threshold Parameter	0.4	0.57	$\text{V}^{0.5}$
λ	Chanel length modulation parameter	0.04 ($L = 1 \mu\text{m}$) 0.01 ($L = 2 \mu\text{m}$)	0.05 ($L = 1 \mu\text{m}$) 0.01 ($L = 2 \mu\text{m}$)	V^{-1}
$2 \Phi_F $	Surface potential at strong inversion	0.7	0.8	V

The drain current $I_D = K' \frac{W}{L} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right] V_{DS}$ and at saturation $V_{DS}(\text{sat}) = V_{GS} - V_T$, where gate to source voltage is V_{GS} , V_{DS} is drain to source voltage and V_T is threshold voltage.

The threshold voltage V_T is given by

$$V_T = V_{T_0} + \gamma \left[\sqrt{2|\Phi_F| + v_{SB}} - \sqrt{2|\Phi_F|} \right]$$