# DVD Monsoon 2025:Quiz-5

Total points 6/10

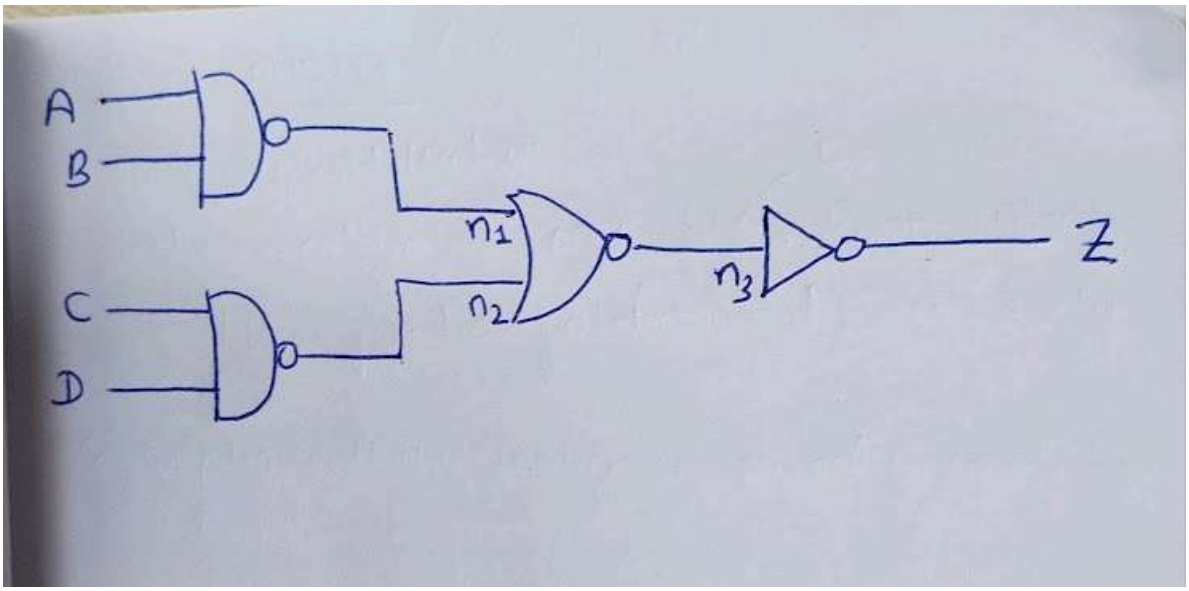
**Quiz Instruction**

- The test will be live from **4:00 PM to 7:00 PM**.
- You must submit your response **before 7:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

✗ 3. Choose the correct options for the following circuit 0/2

Assuming the input probability of 0.5 at each input. Load at Output is 50fF and frequency of clock is 1Ghz and Voltage as 1.2V .




- [ ] Activity Factor at node n2 is 3/4
- [x] Activity Factor at node n3 is 15/256 ✓
- [ ] Dynamic power consumption for the circuit is 0.281 μW
- [ ] Probability of node n3 to be high is 15/16
- [ ] Dynamic power consumption for the circuit is 4.21 μW

Correct answer

- [x] Activity Factor at node n3 is 15/256
- [x] Dynamic power consumption for the circuit is 4.21 μW

Roll No. *

2023024

✗ A designer wants to design a digital circuit in which he has to operate a clock at 1ns speed but during the design process he finds out that power consumption is very high, choose the correct ways to reduce the power consumption. 0/1

- [x] Designer can find the way to reduce the load capacitance so as to decrease the dynamic power consumption ✓
- [x] He can operate the circuit in low voltage which helps to reduce the power as well as It helps to reduce the overall area of a design . ✗
- [x] Dynamic Power is directly proportional to frequency , Designer can reduce the frequency of operation . ✗
- [x] He can improve the slope of all inputs to reduce the short circuit power . ✓
- [x] He can use the High Vt devices . ✓

Correct answer

- [x] Designer can find the way to reduce the load capacitance so as to decrease the dynamic power consumption
- [x] He can improve the slope of all inputs to reduce the short circuit power .
- [x] He can use the High Vt devices .

**Feedback**

*By reducing load capacitance we can reduce dynamic power.*
*When we design for a target performance goal at low voltage, the area of the design increases (not reduces) to be able to drive similar currents to achieve the desired performance.*
*Changing frequency is not an option here because operating at 1ns is the specification / user requirement.*

✓ Draw CMOS schematic for the boolean expression and size the transistors with respect to the unit inverter. 2/2

**Y' = (A+B).C + (D.E)**

- [ ] If we consider the size of unit inverter a 1 unit , then addition of size of PMOS in which Input is D and E is connected is 10
- [x] Total area consumed by NMOS stack is 10 units ✓
- [ ] Logical effort at input C is 2
- [ ] Rise contamination delay is 8RC .

Name *

Abhinav Maurya

✓ We know that one of the methods to achieve high Ion in active mode and low Ioff in sleep mode is to dynamically adjust the threshold voltage of the transistors by applying a body bias. 1/1

Select the correct statement about this :

- [x] Low-Vt devices can be used and a reverse body bias (RBB) can be applied during sleep mode to reduce leakage ✓
- [x] Higher-Vt devices can be used, and then a forward body bias (FBB) can be applied during active mode to increase performance ✓
- [ ] Low-Vt devices can be used and a forward body bias (FBB) can be applied during active mode to reduce leakage
- [ ] There is no effect of Vt variation in sleep mode as there is no current flowing .

**Feedback**

*This technique is sometimes called variable threshold CMOS (VTCMOS).*

*For example, low-Vt devices can be used and a reverse body bias (RBB) can be applied during sleep mode to reduce leakage . Alternatively, higher-Vt devices can be used, and then a forward body bias (FBB) can be applied during active mode to increase performance .*

*Body bias can be applied to the power gating transistors to turn them off more effectively during sleep.*

✓ Which of the following are components of Leakage Power Dissipation? 1/1

- [x] Subthreshold Leakage ✓
- [ ] Bias Current
- [x] Junction Leakage ✓
- [ ] Short- circuit Current

**Feedback**

*Short-circuit current is indeed not a component of static power dissipation. It occurs during the switching events when both NMOS and PMOS transistors are momentarily conducting, leading to a direct path from VDD to GND. This type of power dissipation is categorized under dynamic power dissipation.*

*Bias currents are designed into the circuit for correct operation of analog circuits. Therefore these are not leakage power. However, they are a part of static power.*

✓ For a 3-input NAND gate (A-B-C), which of the following statements about leakage current is true? 1/1

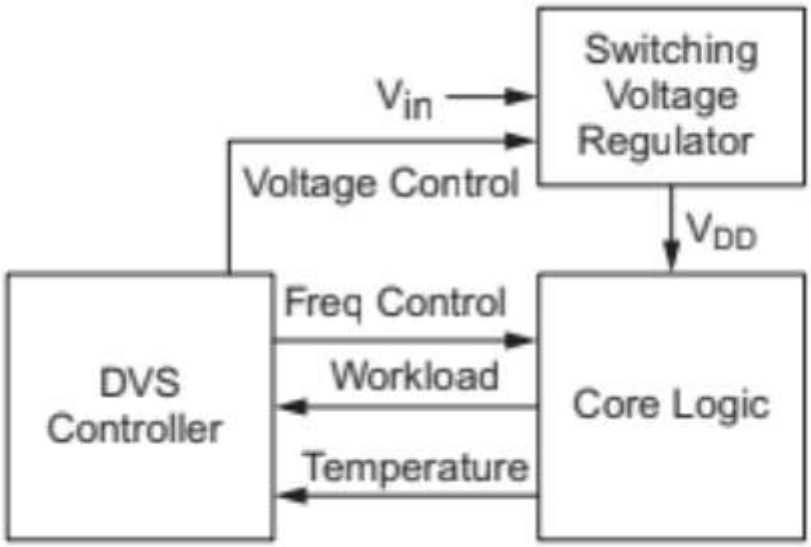
- [x] For input ABC = 111, the highest leakage current occurs. ✓
- [x] For input ABC = 111, there is no stack effect. ✓
- [x] For input ABC = 000, the stack effect is present. ✓
- [x] For input ABC = 000, the leakage current is less compared to input ABC = 111 ✓

**Feedback**

*The NAND3 benefits from the stack effect to reduce subthreshold leakage. In the 000 case, all three nMOS transistors are OFF and the triple stack effect cuts leakage by a factor of 10. Both intermediate nodes drift up to somewhere around 100–200 mV set by the stack effect. In the 001 and 100 cases, two nMOS transistors are OFF and the double stack effect cuts leakage by a factor of 5. In the 110 case, the nMOS stack experiences full subthreshold leakage because only one transistor is OFF and it sees Vds = VDD. In the 011 and 101 cases, the single OFF nMOS transistor sees Vds = VDD – Vt, so the leakage is partially reduced. In the 111 case, all three parallel pMOS transistors leak.*

✓ Dynamic Voltage frequency Scaling is a popular method for reducing the power consumption , 1/1

Choose the correct statements :
A basic DVFS/DVS system is as shown is figure :




- [x] The DVS controller determines the operating frequency, then chooses the lowest supply voltage suitable for that frequency. ✓
- [x] When moving from High power to Low power mode , the regulator first decreases the frequency then voltage . ✓
- [x] When moving from Low power to High power mode , the regulator first increases the voltage then frequency . ✓
- [x] Subthreshold and gate leakage are strongly sensitive to the supply voltage, so DVFS is effective at reducing leakage during periods of low activity. ✓

**Feedback**

*The DVS controller determines the operating frequency, then chooses the lowest supply voltage suitable for that frequency. One method of choosing voltage is with a prechar-acterized table of voltage vs. frequency. This is inherently conservative because the voltage should be high enough to suffice for even worst-case parts*

✗ Select the incorrect statements from below . 0/1

- [x] We use at least 4 different Vt devices in a design so that we can reduce the leakage as well as cost of a design ✓
- [ ] We use high High Vt device in memory design compared to logic design
- [ ] Using multiple thresholds requires additional implant masks that add to the cost of a CMOS process.
- [x] Good design practice starts with high-Vt devices everywhere and selectively introduces low-Vt devices where necessary to reduce the static power consumption. ✗
- [x] Designers can decrease the channel length, which tends to raise the threshold voltage via the short channel effect. ✓

Correct answer

- [x] We use at least 4 different Vt devices in a design so that we can reduce the leakage as well as cost of a design
- [x] Designers can decrease the channel length, which tends to raise the threshold voltage via the short channel effect.

**Feedback**

*Overall Cost of the product increases, when we use more than 3 vt as it requires more implant masks. To reduce leakage, we often use high vt devices.*
*To circumvent the costly addition of numerous implant masks for a wide range of Vt options, designers can turn to a clever technique known as poly biasing. This method involves adjusting the physical dimensions of the transistor's gate, to modulate its on and off current in-line with the requirements.*