DVD Monsoon 2025: Review Quiz-9

Total points 7/10

Quiz Instruction

- The test will be live from **5:00 PM to 7:00 PM**.
- You must submit your response **before 7:00 PM**; no responses will be accepted afterward.
- Each question may have multiple correct options. You get points only when you select all the correct options and no incorrect option.
- Only **one attempt** is allowed per student.
- You must attempt the quiz using your **college email ID**.

The respondent's email (**abhinav23024@iiitd.ac.in**) was recorded on submission of this form.

What are the sources of Clock uncertainties? 1/1

- [x] Coupling ✓
- [x] Temperature ✓
- [x] Power Supply Noises ✓
- [x] IR drop through interconnects ✓
- [x] Through clock generators ✓

Feedback

Clock uncertainty arises due to variations in the clock's arrival time caused by physical and electrical effects.

Temperature changes and power-supply noise alter clock delays.

PLL/DLL jitter introduces random edge shifts in the period of the clock signal.

Coupling from nearby nets adds additional delay variations, while process variations create mismatched delays across the clock tree.

IR drop and delays through interconnets affects the clock signals which makes signal strength weak.

✗ Select the incorrect statements out of the given statements

0/2

- [ ] PnR tools demands that metal layers are placed orthogonally
- [x] M2 can be placed horizontally or vertically orthogonally with respect to M3. ✗
- [ ] M2 or higher layer bends are not allowed in standard cell area.
- [x] Higher metal layers have lower capacitances compared to lower metal layers.Hence preffered for local routing of signals ✓
- [ ] Higher metal layers are preffered for power and clock signals because they have less resistance
- [x] Metal bends cannot have any fabrication effects ✓
- [x] Metal bends doesnt lead any congestion as higher metal layers are orthogonals ✓
- [ ] Higher metal layers should be placed orthogonally and it will cause no drc issue .
- [x] metals bends are not related to Vias placements ✓

Correct answer

- [x] Higher metal layers have lower capacitances compared to lower metal layers.Hence preffered for local routing of signals
- [x] Metal bends cannot have any fabrication effects
- [x] Metal bends doesnt lead any congestion as higher metal layers are orthogonals
- [x] metals bends are not related to Vias placements

Feedback

Each metal layer is assigned a preferred routing direction during PnR stage. If all metals are routed in any direction, wires would cross and overlap more often, creating congestion. Hence consecutive metal layers are placed orthogonally

Higher metal layers are thicker, have more spacing requirements, and lesser coupling capacitance. So, they also have lower resistance and can be used to route long global signals and clocks.

Vias placements can be easier when consecutive metal layers are placed orthogonally, which will results in lesser congestion

✓ **During Presentation Sir pointed about the sizing of the pmos clock? Select the correct statements** 2/2

- [ ] Pmos should be sized 0.135um as it will reduces Area in our layout.
- [ ] In Dynamic Circuits, Rise times are not important and they are not part of the evaluation phase
- [x] It could lead to incomplete charging to VDD before evaluation phase. ✓
- [ ] It will not help in logic Evaluation hence we can keep it small.
- [x] Noise Margin will get affected. ✓
- [ ] There will be enough time to precharge the circuit.Hence keeping it small and large doesn't matter at all.
- [x] It can lead to glitch in the output ✓
- [ ] Output will be well settled and do not depends on the sizing of the pmos clock.
- [x] It can limit the clock frequency at which the circuit is operating. ✓

Feedback

If the pmos is kept small , it will have higher resistance and the charging of the dynamic nodes slowes down and the evaluation phase may come before the output is precharged to full VDD.

Noise margin will get affected as the node may not get charged to full VDD if the precharge phase is not kept High for too long Thereby reducing Noise margin.

Incomplete charging can leads to glitches in the output node.

✓ **What makes clock skew different from the clock jitter ?Select the correct statements** 2/2

- [x] clock skew is the difference between the arrival time at the sequential elements ✓
- [x] Clock jitter is temporal variation and random ✓
- [x] Clock jitter affects the periodicity of the clock signals. ✓
- [x] Both affects the performance of the design. ✓

Feedback

Clock skew is systematic, deterministic difference in arrival time of the same clock edge at two different flip flops.

clock jitter is random or variation in the timing of a clock edge at a single circuit element

✗ **Which of the following statements are incorrect based on your understanding while making layouts.** 0/1

- [x] There is no problem in splitting nwell as no drc will occur regarding breaking of nwells. ✓
- [ ] We may face NW-NW DRC's and No LVS error will occur
- [x] There will be LVS error if Nwells are not spaced properly uptil minimum drc. ✓
- [ ] We will encounter LVS error if NW's are not connected.
- [ ] There is minimum area related drc with respect to NW.

Correct answer

- [x] There is no problem in splitting nwell as no drc will occur regarding breaking of nwells.
- [x] We may face NW-NW DRC's and No LVS error will occur
- [x] There will be LVS error if Nwells are not spaced properly uptil minimum drc.

Feedback

NWell have minimum area related DRC.

Nwell can be split but it should be connected otherwise we will have LVS S_CONNECT issue.

If two NWell are seperated and kept seperately then it will have some DRC constraints .

✓ **At what PVT Corners should be simulate our design for sub threshold leakage** *1/1

- [ ] PMOS - Fast; NMOS - Fast; VDD - 1.08; Temperature - Low
- [ ] PMOS - Slow; NMOS - Slow; VDD - 1.32; Temperature - High
- [ ] PMOS - Fast; NMOS - Fast; VDD - 1.32; Temperature - low
- [x] PMOS - Fast; NMOS - Fast; VDD - 1.32; Temperature - High ✓

Feedback

Subthreshold Leakages increase exponentially at high temperatures.

Sub-threshold current is also higher at high voltages because electrons have high energy and effectively available for charge transfer (current).

Fast lots have lower threshold voltage, indicating that higher current is possible at lower voltages. So, sub-threshold leakage is higher.

✓ **During the presentation, we saw that one group placed all the input pins of their design continuously, without spreading them out. What implications could this have?** 1/1

- [ ] It reduces capacitance and results in fewer DRC violations
- [ ] It makes accessing the pins using higher metal layers easier
- [x] It could lead to congestion ✓
- [ ] Routing efficiency will increase and pins can be accessed through vias using higher metal layers

Feedback

Pins should be uniformly spread rather placed close to each other. Adjacent placement can cause routing congestion especially due to constraints placed by foundries and/ or PnR tools to route metals in single direction.

More congestion also results in increased capacitances at the inputs.