INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI
ECE 515/315 ANALOG CMOS
MID-TERM EXAMINATION

Date: SEPTEMBER 28, 2025 Max. Marks: 30 Time: 3:00 PM to 4:00 PM

Note:

- **PLEASE READ THE INSTRUCTIONS CAREFULLY. ANY NON-ADHERENCE TO INSTRUCTIONS WILL BE CONSIDERED AS CHEATING.**
- **ANSWER ALL QUESTIONS. IT IS AN OPEN BOOK TEST.**
- **No Mobile Phones, laptop or solution manual/or its print out will be permitted in the examination hall.**
- **It is an open BOOK AND HANDWRITTEN NOTES PREPARED BY YOURSELF and lecture slides distributed to the class.**
- **Borrowing of BOOKS, handwritten notes, lecture slides from others is strictly prohibited.**
- **NO PHOTOCOPIED NOTES PREPARED BY ANOTHER STUDENT WILL BE PERMITTED.**
- **The only person you are allowed to talk to is your invigilators.**
- **Any rough work should be done in the answer script and submitted. You are not permitted to take your rough work outside the examination hall.**
- **If you carry solutions to tutorials and practice problems in your handwriting it will be permitted. However, photocopies of these solutions, unless uploaded in the classroom, will not be permitted.**

Q.1 Show that the series connection of MOSFETs in Fig. 1 behaves as a single MOSFET with twice the length of individual MOSFETs. Assume (W/L) ratio is same for both transistors and the transistors are in triode state. Neglect the body effect.

[10 marks]

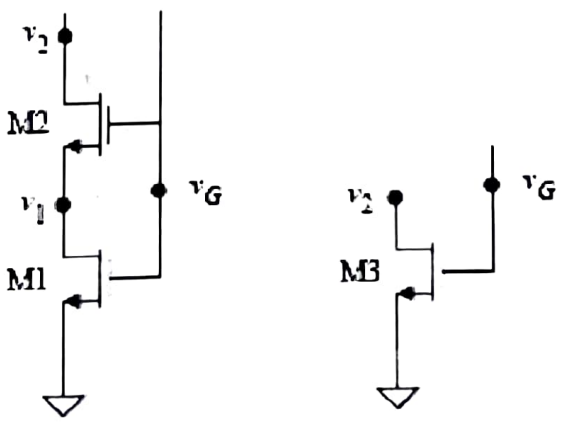
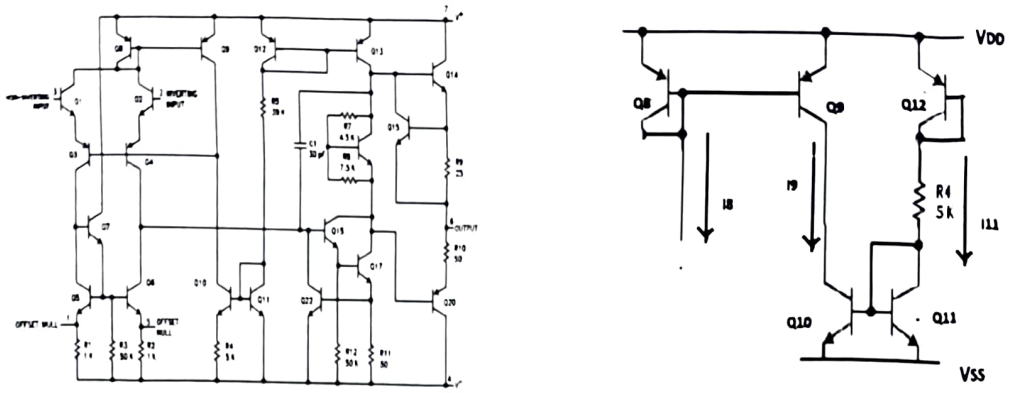


Figure 1

Q.2 Figure 2(a) shows the internal circuit of IC741 and a part of IC741 circuit, which generates the necessary current to bias different stages of 741 amplifier, is shown in Figure 2(b). We would like to replace all BJTs in Figure 2(b) with MOS transistors only to achieve the same functionality as in IC741.

(i) Draw the appropriate circuit equivalent to Figure 2(b) using only MOS transistors and resistance. **[4 MARKS]**

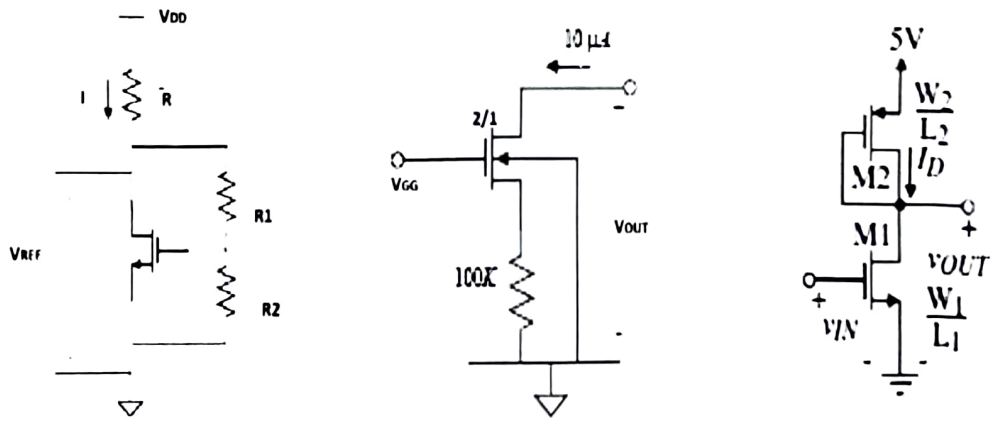
(ii) Design this circuit to give I8 equal to 1 mA for V_{DD} = 5 V and V_{SS} = -5 V. Assume V_{TH} = 0.75 V and all transistors to have same (W/L) ratio. Give all the design steps. **[6 MARKS]**



(a) (b)

Figure 2

Q.3 (a) Draw the small signal equivalent circuit for the circuits given in Figure 3(a) and 3(b). **[6 MARKS]**



(a) (b) (c)

Figure 3

(b) What value of V_{in} will give a current of 100 µA in the active load inverter in Figure 3(c), if W_1/L_1 = 5µm /1µm and W_2/L_2= 2µm /1µm? Assume $\mu_n C_{ox}$ = 100. **[4 MARKS]**