ECE315/ECE515 Practice Problems 2

1. A large-signal model for the MOSFET that features symmetry for the drain and source is given by

$$i_D = K'\frac{W}{L}\Big\{\big(v_{GS}-V_{TS}\big)^2\,u\big(v_{GS}-V_{TS}\big)-\big(v_{GD}-V_{TD}\big)^2\,u\big(v_{GD}-V_{TD}\big)\Big\},$$

where $u(x)$ is the step function

$$u(x)=\begin{cases}1, & x\geq 0,\\ 0, & x<0,\end{cases}$$

and V_{RX} denotes the threshold voltage evaluated from the gate to node X (with X equal to S for source or D for drain).

Sketch this model in the form of i_D versus v_{DS} for a constant value of v_{GS} (assume $v_{GS} > V_{TS}$), and identify the saturated and nonsaturated regions. Be sure to extend this sketch for both positive and negative values of v_{DS}.

Repeat the sketch of i_D versus v_{DS} for a constant value of v_{GD} (assume $v_{GD} > V_{TD}$). Assume that both V_{TS} and V_{TD} are positive.

2. Calculate the transfer function $\dfrac{v_{\text{out}}(s)}{v_{\text{in}}(s)}$ for the circuit shown in Fig. P3.3-1. The W/L of M1 is $2\,\mu$m/$0.8\,\mu$m and the W/L of M2 is $4\,\mu$m/$4\,\mu$m.

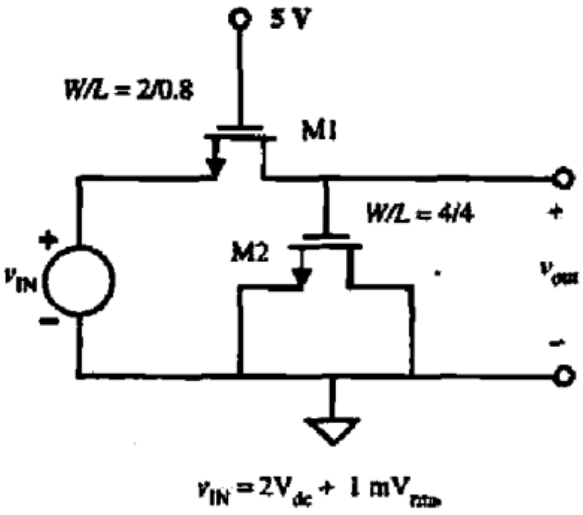

Figure P3.3-1

Figure 1: Circuit for Question P3.3-1.

3. Consider the circuit in Fig. P3.3-5. It is a parallel connection of n MOSFET transistors. Each transistor has the same length, L, but each transistor can have a different width, W.

Derive an expression for W and L for a single transistor that replaces, and is equivalent to, the multiple parallel transistors.

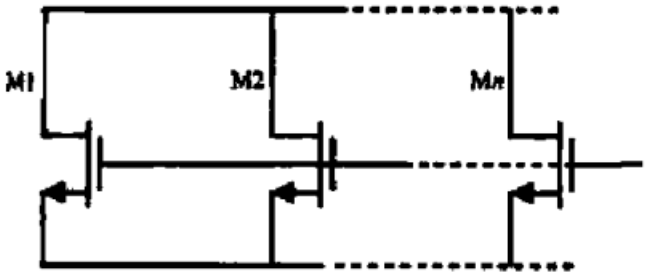

Figure P3.3-5

Figure 2: Circuit for Question P3.3-5.

4. Consider the circuit in Fig. P3.3-6. It is a series connection of n MOSFET transistors. Each transistor has the same width, W, but each transistor can have a different length, L_i. Derive an expression for the width W' and length L' of a single transistor that replaces, and is equivalent to, the multiple series transistors. When using the simple model, you must ignore body effect.

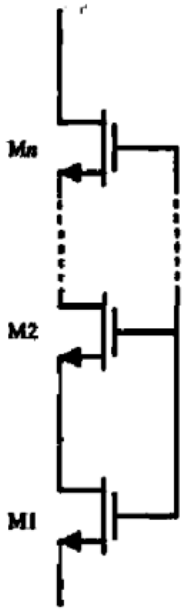

Figure P3.3-6

Figure 3: Circuit for Question P3.3-6.

5. Another way to approximate the transition from strong inversion to weak inversion is to find the current at which the weak-inversion transconductance and the strong-inversion

transconductance are equal. Using this method and the approximation for drain current in weak inversion (Eq. (3.5-5)), derive an expression for the drain current at the transition between strong and weak inversion. For hand calculations, a simple model describing weak inversion operation is given as

$$i_D \approx \frac{W}{L} I_{D0} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) \tag{3.5-5}$$

where the term n is the subthreshold slope factor, and I D0 is a process-dependent parameter that is dependent also on v SB and V T . These two terms are best extracted from experimental data. Typically n is greater than 1 and less than 3 (1¡n¡3). The point at which a transistor enters the weak inversion region can be approximated as

$$v_{GS} < V_T + \frac{kT}{nq} \tag{3.5-6}$$

6. The circuit shown in Fig. P4.1-2 illustrates a single-channel MOS resistor with a W/L of 2 m/1 m. Using Table 3.1-2 model parameters, calculate the small-signal ON resistance of the MOS transistor at various values for V_S and fill in the table below.

V_S (volts)	R (ohms)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

Table.

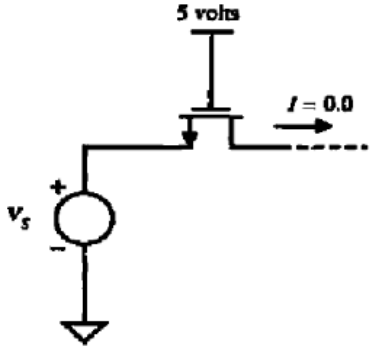

Figure P4.1-2

7. The circuit shown in Fig. P4.1-4 illustrates a complementary MOS resistor with an n-channel W/L of 2 $\mu m/1$ μm and a p-channel W/L of 4 $\mu m/1$ μm. Using Table 3.1-2 model parameters, calculate the small-signal ON resistance of the complementary MOS resistor at various values for V_S and fill in the table below.Note that the most positive supply voltage is 5 V.

V_S (volts)	R (ohms)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

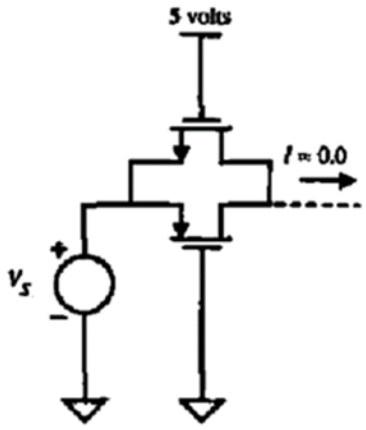

Figure P4.1-4

Fig P4.1-4.

8. Calculate the temperature coefficient of the circuit in Fig. 4.5-4(a), where $W/L = 2$, $V_{DD} = 5$ V, and $R = 100$ kΩ, using the parameters of Table 3.1-2. Resistor R is polysilicon and has a temperature coefficient of 1500 ppm/°C.

TABLE 3.1-2 Model Parameters for a Typical CMOS Bulk Process Suitable for Hand Calculations Using the Simple Model with Values Based on a 0.8 μm Silicon-Gate Bulk CMOS n-Well Process

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage ($V_{BS} = 0$)	0.7 ± 0.15	−0.7 ± 0.15	V
K'	Transconductance parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L = 1 μm) 0.01 (L = 2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	V^{-1}
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

Table 3.1-2.

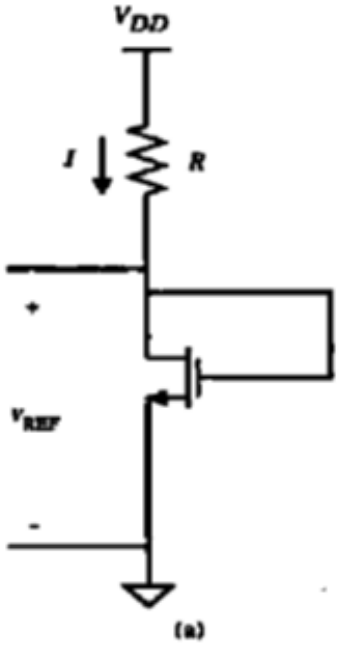

Fig. 4.5-4(a).

9. (Problem:A) Figure P4.3-1 illustrates a source-degenerated current source. Using Table 3.1-2 model parameters, calculate the output resistance at the given current bias.

(Problem:B) Calculate the minimum output voltage required to keep the device in saturation in Problem A.

(Problem:C) Using the cascode circuit shown in Fig. P4.3-3, design the W/L of M_1 to achieve the same output resistance as the circuit in Fig. P4.3-1.

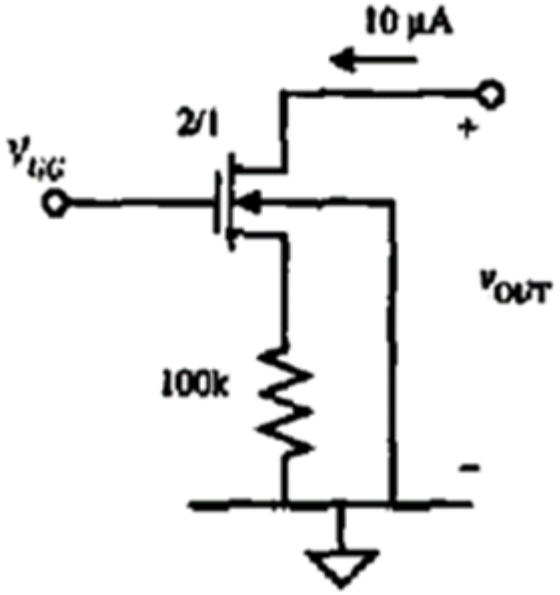

Figure P4.3-1

Fig. P4.3-1

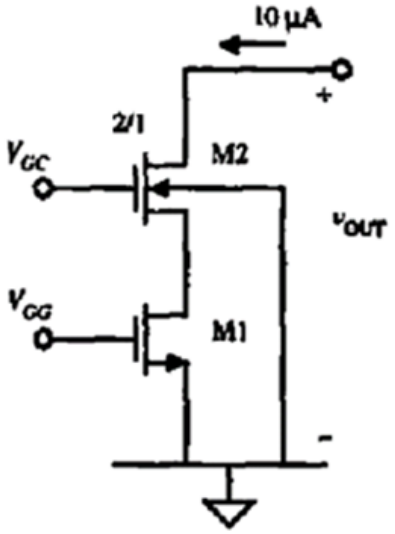

Figure P4.3-3

Fig. P4.3-3.

10. Calculate the output resistance and the minimum output voltage, while maintaining all devices in saturation, for the circuit shown in Fig. P4.3-6. Assume that i_{OUT} is 10 μA.

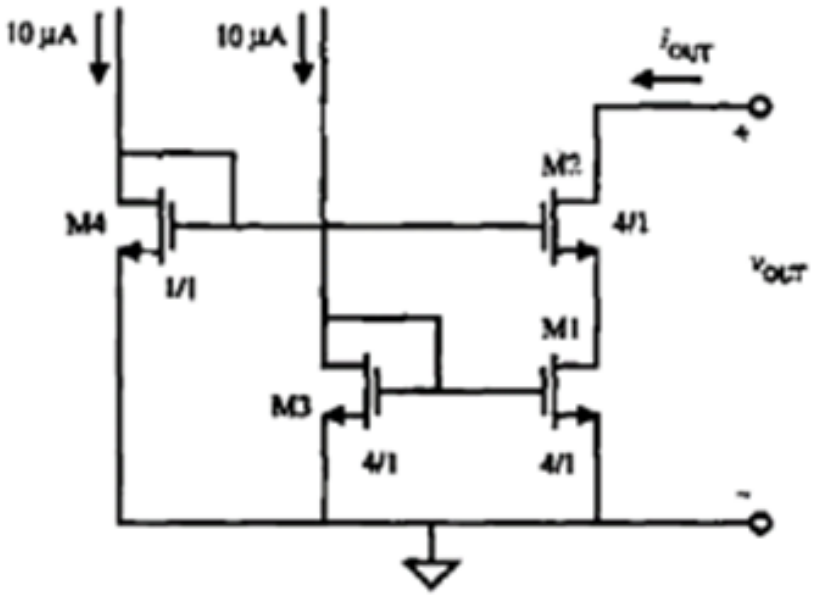

Figure P4.3-6

Fig. P4.3-7.

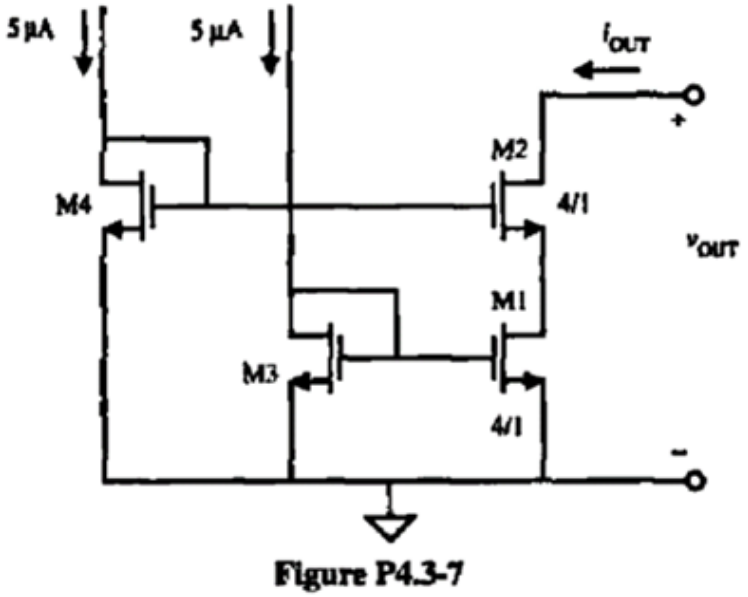

Figure P4.3-7

Fig. P4.3-7.

11. Design M_3 and M_4 of Fig. P4.3-7 so that the output characteristics are identical to the circuit shown in Fig. P4.3-6. It is desired that i_{OUT} is ideally 10 μA.

12. Consider the simple current mirror illustrated in Fig. P4.4-1. Over the process, the absolute variations of physical parameters are as follows:

Width variation	±5%
Length variation	±5%
K' variation	±5%
V_T variation	±5 mV

Assuming that the drain voltages are identical, what is the minimum and maximum output current measured over the process variations given above?

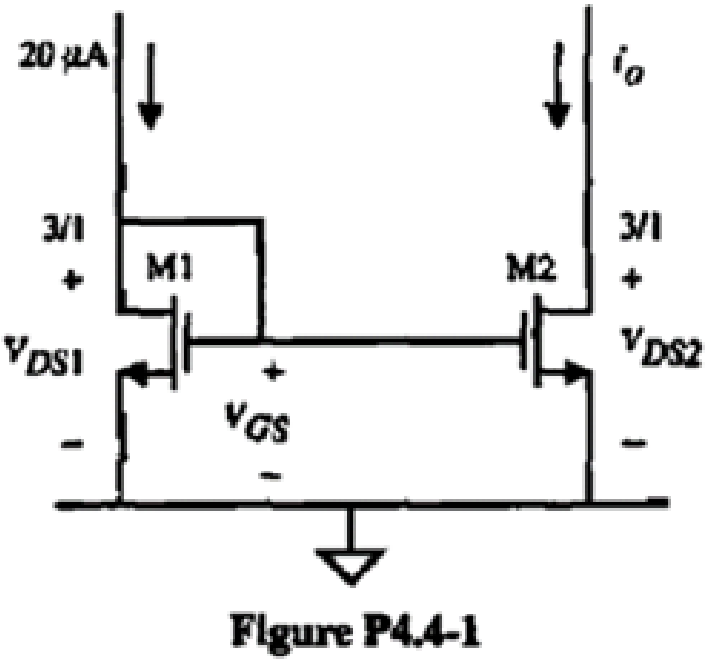

Figure 4: Circuit for Fig. P4.4-1.

13. Consider the circuit in Fig. P4.4-2, where a single MOS diode (M2) drives two current mirrors (M1 and M3). A signal (v_{sig}) is present at the drain of M3 (due to other circuitry not shown). What is the effect of v_{sig} on the signal at the drain of M1, v_{out}? Derive the transfer function $v_{sig}(s)/v_{out}(s)$. You must take into account the gate–drain capacitance of M3 but you can ignore the gate–drain capacitance of M1.

Given that $I_{BIAS} = 10$, W/L of all transistors is 2/1, and using the data from Tables 3.1-2 and 3.2-1, calculate v_{out} for $v_{sig} = 100$ at 1MHz.

TABLE 3.2-1 Capacitance Values and Coefficients for the MOS Model

Type	p-Channel	n-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 Å or $C_{ox} = 24.7 \times 10^{-4}$ F/m^2.

tableTable 3.2-1

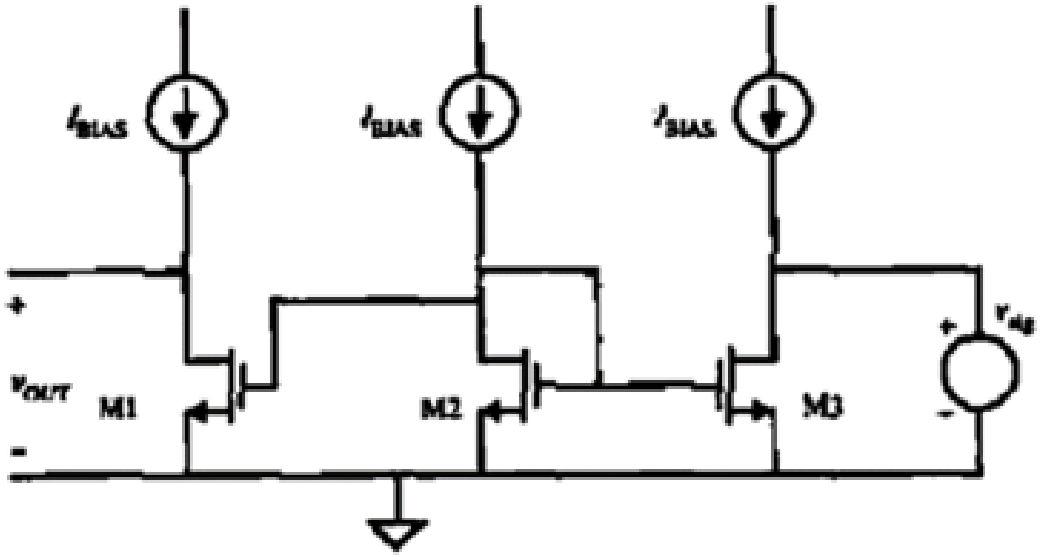

Figure P4.4-2

figureFig. P4.4-2

14. An improved bandgap reference generator is illustrated in Fig. P4.6-1. Assume that the devices M1 through M5 are identical in W/L. Further assume that the area ratio for the bipolar transistors is 10 : 1. Design the components to achieve an output reference voltage of 1.262. Assume that the amplifier is ideal. What advantage, if any, is there in stacking the bipolar transistors?

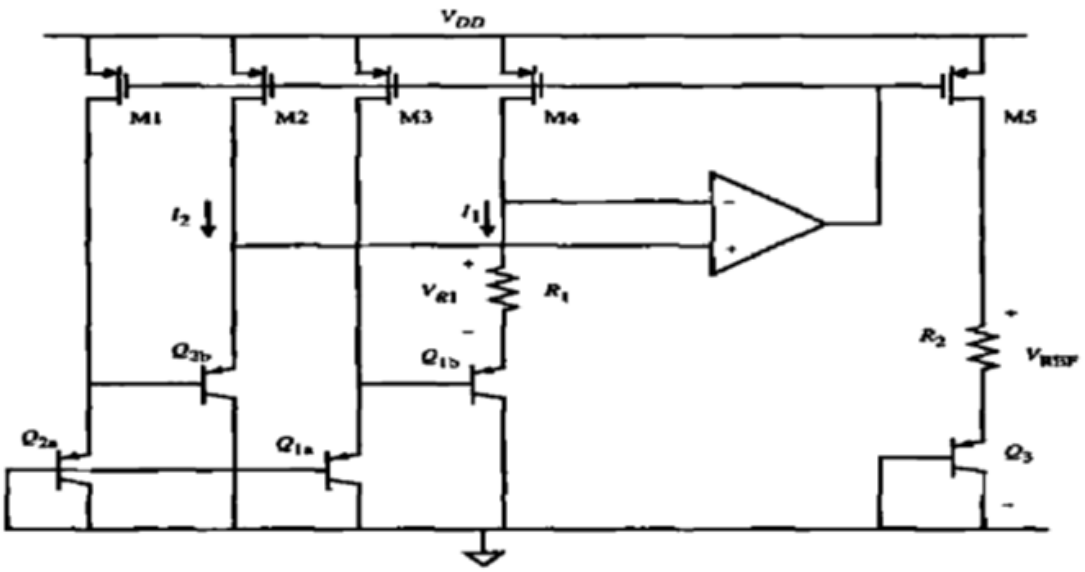

Figure P4.6-1

figureCircuit for Fig. P4.6-1.

15. **T**he following problem is related to an active inverter:

(A) **W**hat value of β_1/β_2 will give a voltage swing of 80% of V_{DD} if V_T is 20% of V_{DD}? What is the small-signal voltage gain corresponding to this value of β_1 / β_2?

(B) **W**hat value of V_{in} will give a current in the active load inverter of 100 μA if $W_1/L_1 =$ 5 μm/1 μm and $W_2/L_2 = 2$ μm/1 μm? For this value of V_{in}, what is the small-signal voltage gain and output resistance assuming all transistors are saturated?

16. Assume that W/L ratios of Fig. P5.1-6 are $W_1/L_1 = 2$ μm/1 μm and $W_2/L_2 = W_3/L_3 = W_4/L_4 = 1$ μm/1 μm. Find the dc value of V_{in} that will give a dc current in M1 of 110 μA. Calculate the small-signal voltage gain and output resistance of Fig. P5.1-6 using the parameters of Table 3.1-2 assuming all transistors are saturated.

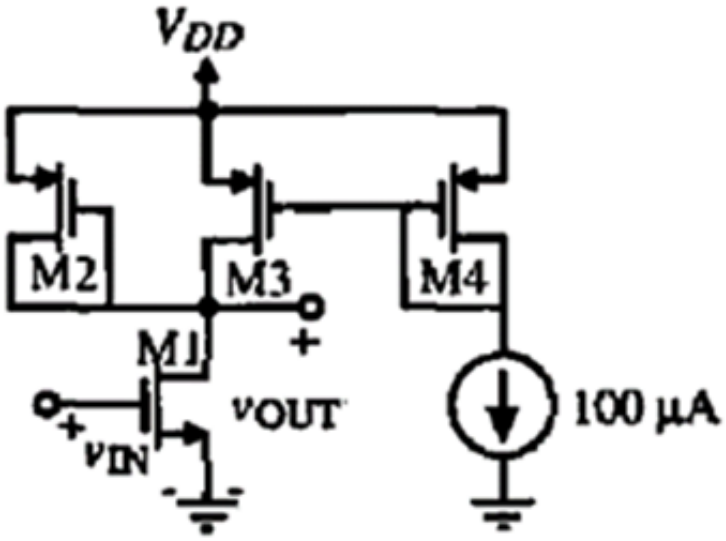

Figure P5.1-6

figureCircuit for Fig. P5.1-6.

17. A CMOS amplifier is shown in Fig. P5.1-9. Assume M1 and M2 operate in the saturation region.

(a) What value of V_{GG} gives 100 μA through M1 and M2?

(b) What is the dc value of v_{IN}?

(c) What is the small-signal voltage gain, $v_{\text{out}}/v_{\text{in}}$, for this amplifier?

(d) What is the -3 dB frequency in hertz of this amplifier if $C_{gd1} = C_{gd2} = 5$ fF, $C_{bd1} = C_{bd2} = 30$ fF, and $C_L = 500$ fF?

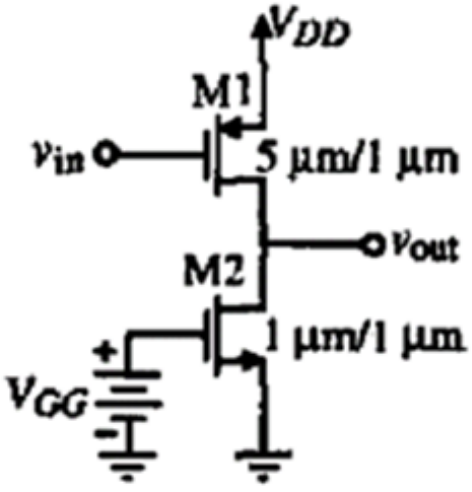

Figure P5.1-9

figureCircuit for Fig. P5.1-9.

18. Six inverters are shown in Fig. P5.1-11. Assume that $K'N = 2K'P$ and that $\lambda_N = \lambda_P$, and the dc bias current through each inverter is equal. Qualitatively select, without using extensive calculations, which inverter(s) has/have

(a) the largest ac small-signal voltage gain,

(b) the lowest ac small-signal voltage gain,

(c) the highest ac output resistance, and

(d) the lowest ac output resistance.

Assume all devices are in saturation.

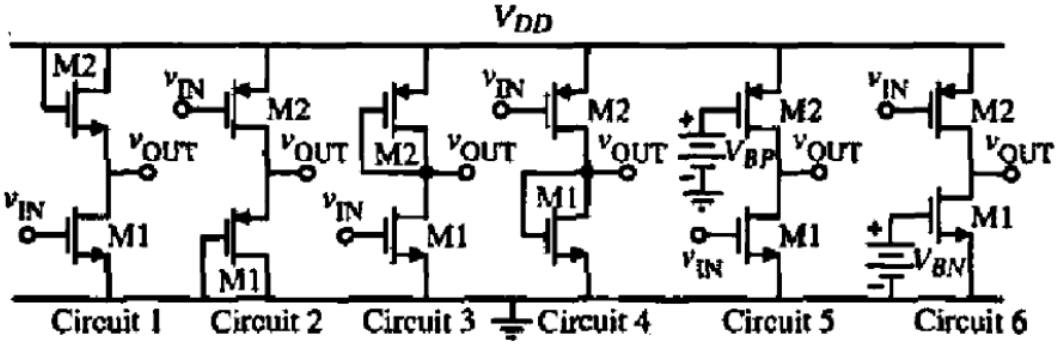

Figure P5.1-11

figureCircuit for Fig. P5.1-11.

19. If all the devices in the differential amplifier of Fig. 5.2-9 are saturated, find the worst-case input offset voltage, V_{OS}, if $|V_t| = 1 \pm 0.01$ V and $\beta_1 = 10^{-5} \pm 5 \times 10^{-7}$ A/V^2. Assume that

$$\beta_1 = \beta_2 = 10\beta_3 = 10\beta_4$$

and

$$\frac{\Delta\beta_1}{\beta_1} = \frac{\Delta\beta_2}{\beta_2} = \frac{\Delta\beta_3}{\beta_3} = \frac{\Delta\beta_4}{\beta_4}$$

Carefully state any assumptions that you make in working this problem.

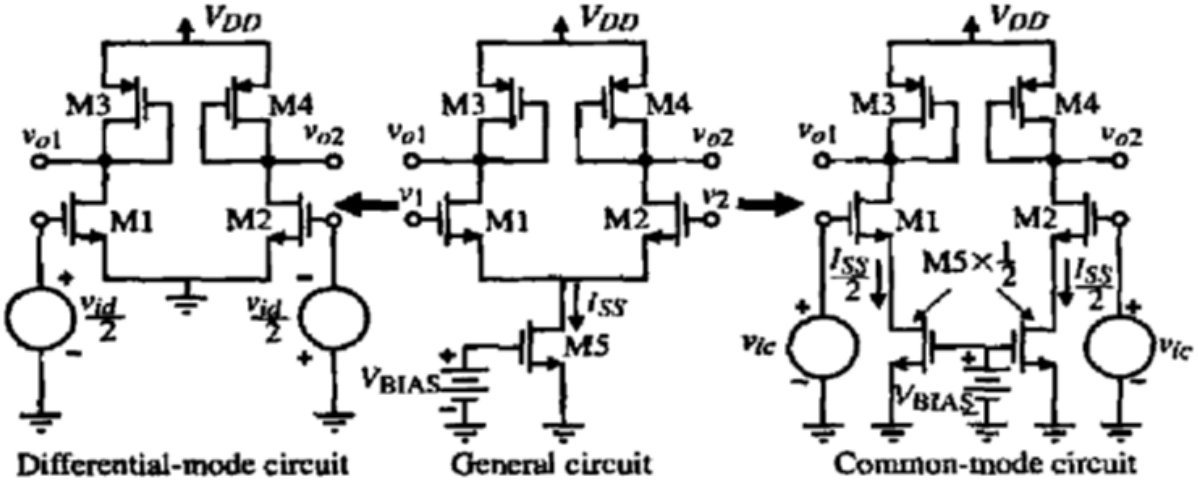

Figure 5.2-9 Illustration of the simplications of the differential amplifier for small-signal, differential-mode, and common-mode analysis.

figureCircuit for Fig. P5.2-9.

20. Five different CMOS differential amplifier circuits are shown in Fig. P5.2-15. Use the intuitive approach of finding the small-signal current caused by the application of a small-signal input, v_{in}, and write by inspection the approximate small-signal output resistance, R_{out}, seen looking back into each amplifier and the approximate small-signal differential-voltage gain, $v_{\text{out}}/v_{\text{in}}$. Your answers should be in terms of g_{mi} and g_{dsi}, $i = 1$ through 8. (If you have to work out the details by small-signal model analysis, this problem will take too much time.)

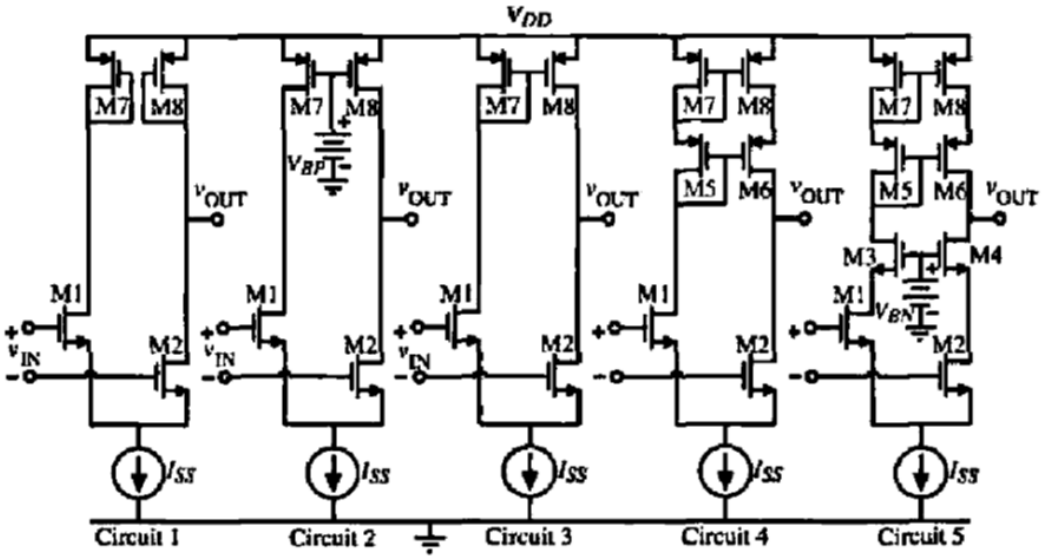

Figure P5.2-15

figureCircuit for Fig. P5.2-15.