- # Implement full adder with two 4x1 multiplexer:

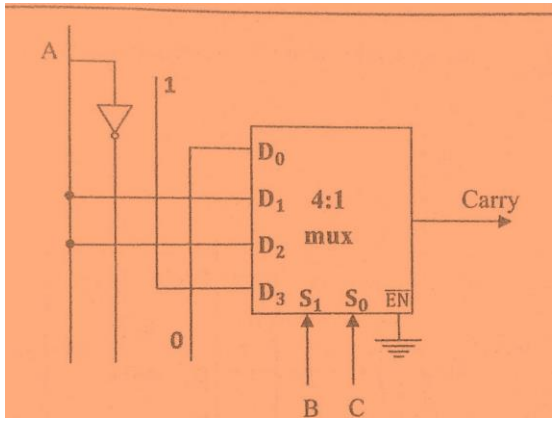
  - From the truth table,
  - Carry=$\sum_m(3,5,6,7)$
  - Sum=$\sum_m(1,2,4,7)$

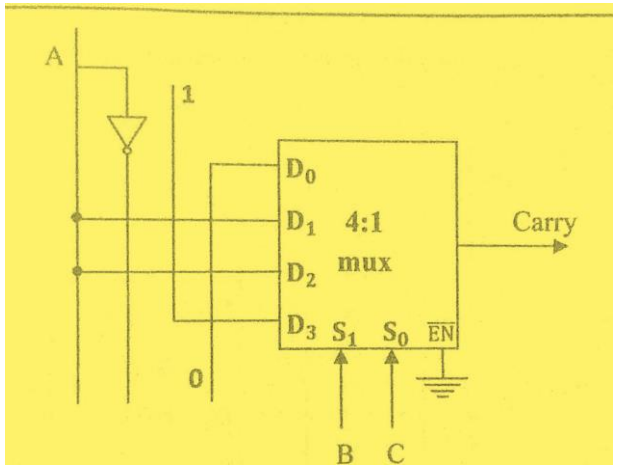
Implementation table for Sum

	D0	D1	D2	D3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	A	$\bar{A}$	$\bar{A}$	A

Implementation Table for Carry:

	D0	D1	D2	D3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	0	A	A	1





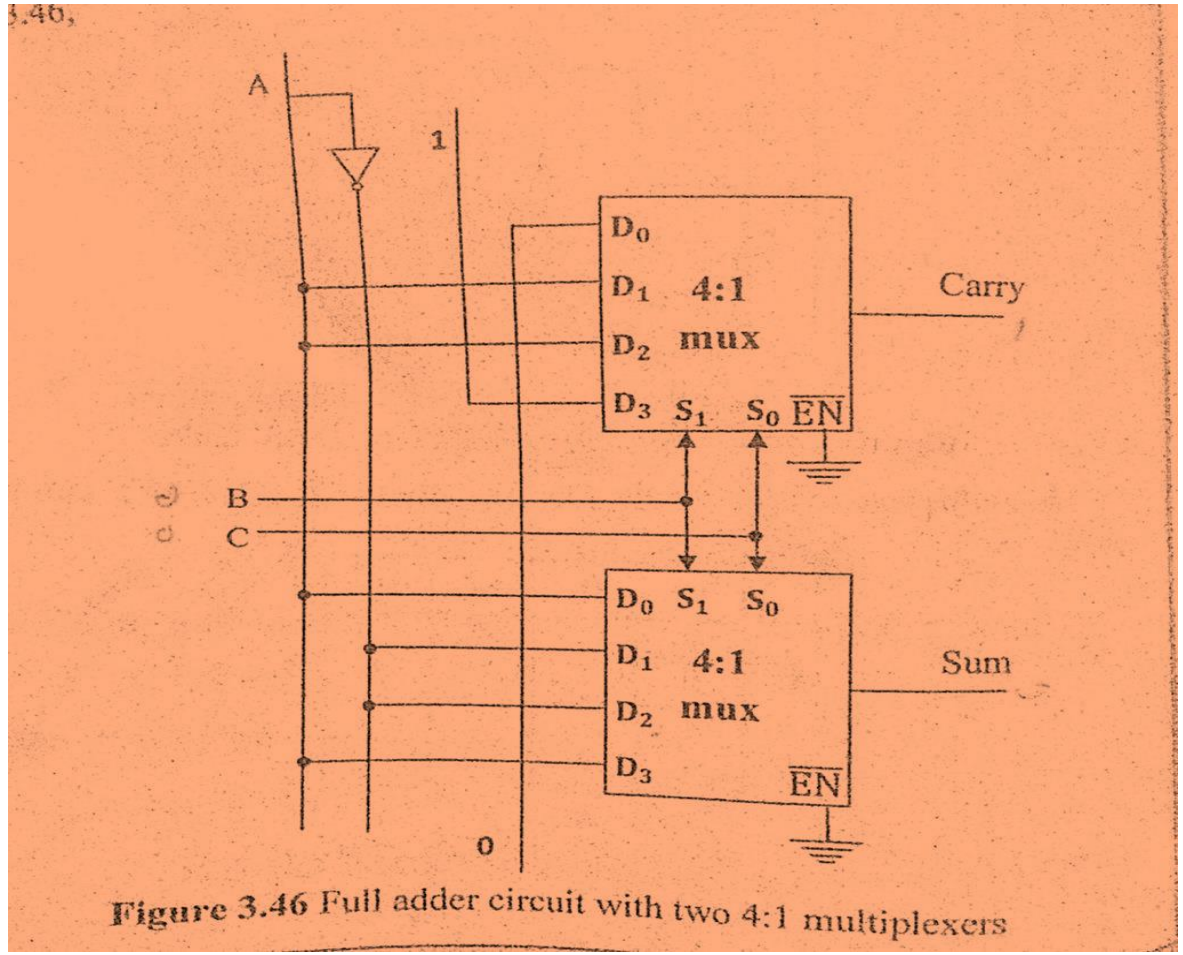
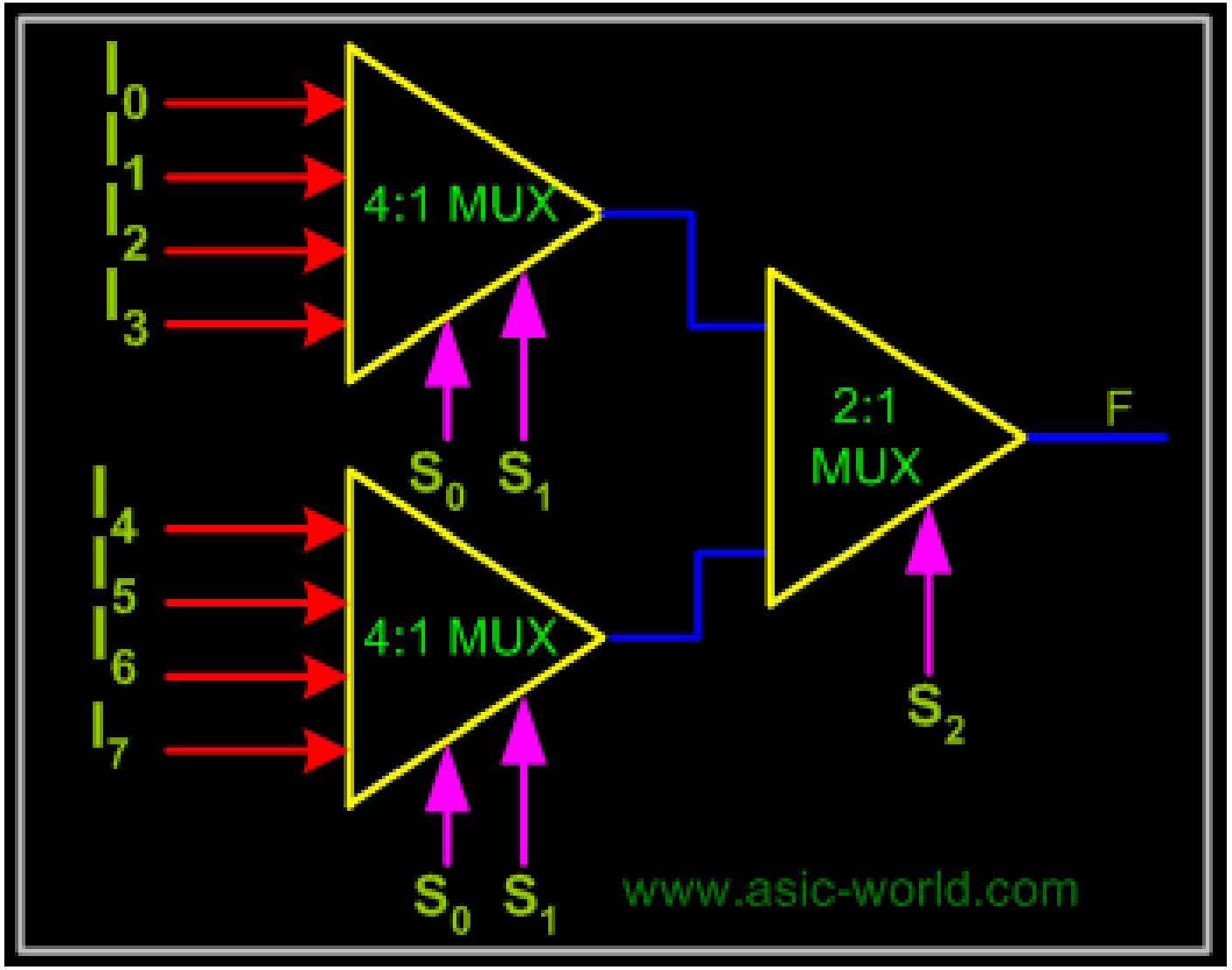


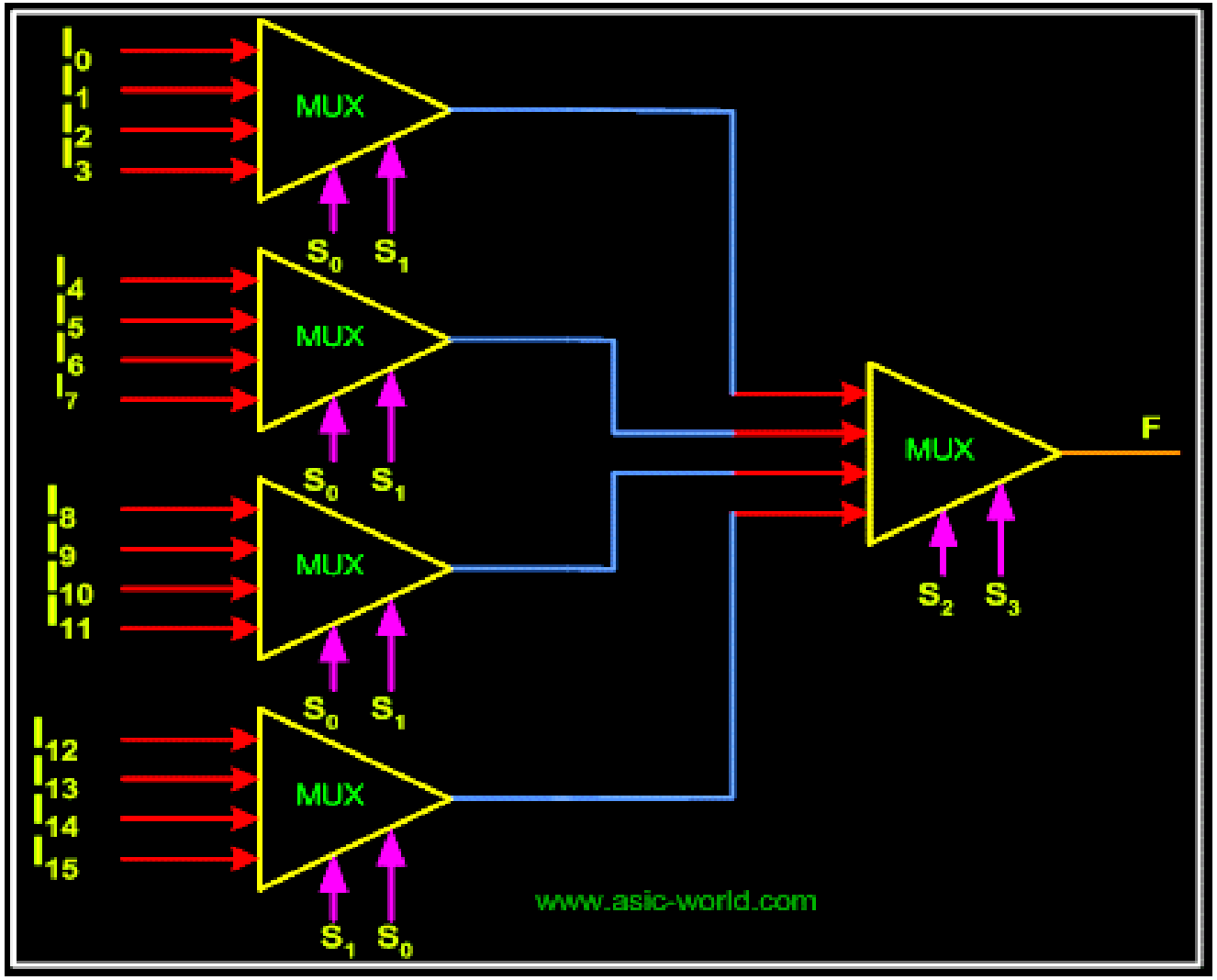
Figure 3.46 Full adder circuit with two 4:1 multiplexers

Large Multiplexer: Ex: 8:1 Mux Using 4:1



S2	S1	S0	F
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

16:1 Multiplexer using 4:1 mux.



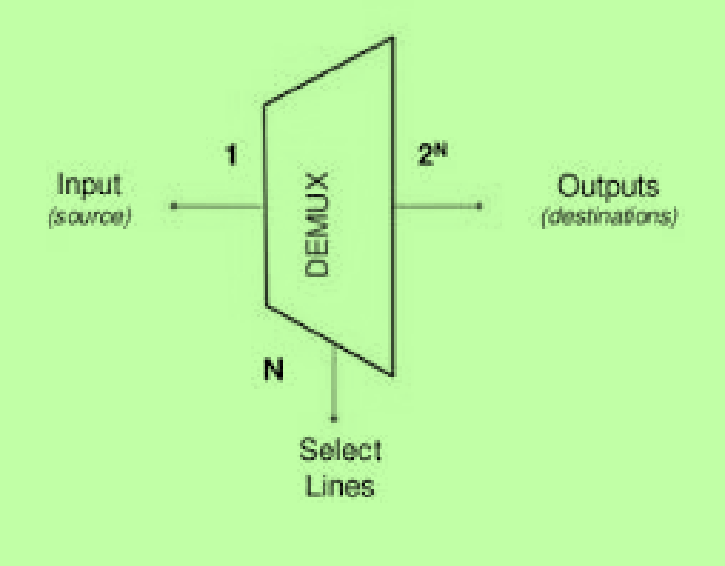
S3	S2	S1	S0	F
0	0	0	0	I0
0	0	0	1	I1
0	0	1	0	I2
0	0	1	1	I3
0	1	0	0	I4
0	1	0	1	I5
0	1	1	0	I6
0	1	1	1	I7
1	0	0	0	I8
1	0	0	1	I9
1	0	1	0	I10
1	0	1	1	I11
1	1	0	0	I12
1	1	0	1	I13
1	1	1	0	I14
1	1	1	1	I15

Applications of Multiplexer:

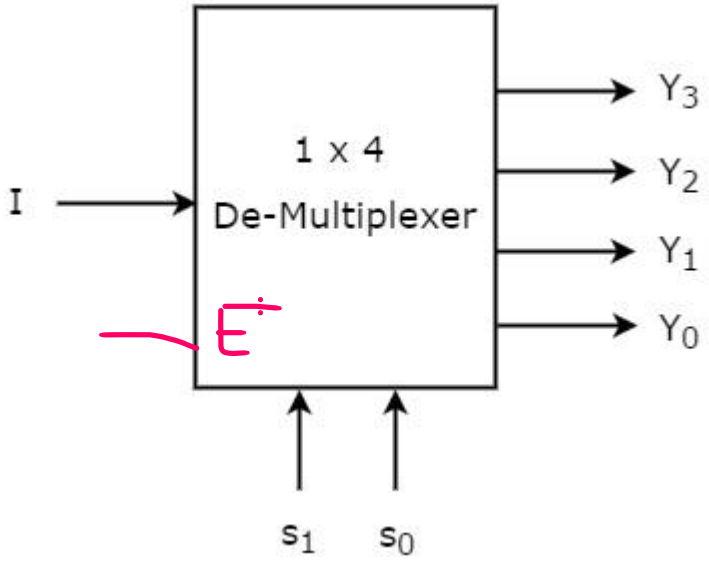
- Data Routing
- Logic Function generator
- Control sequencer
- Parallel to serial converter

Demultiplexer(Data Distributor):

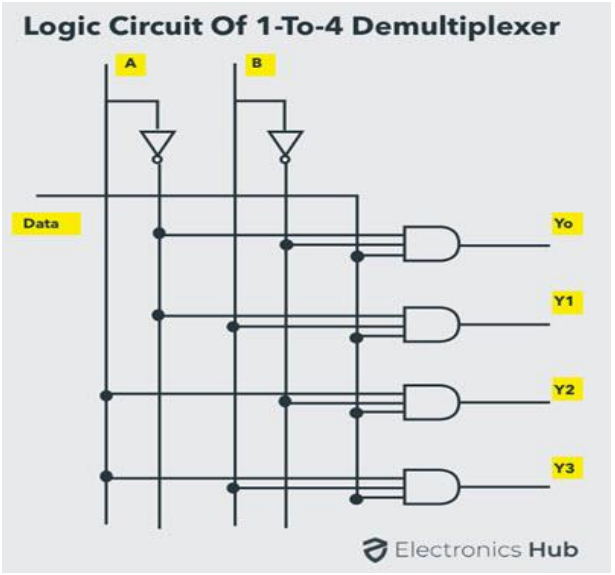
- The word Demultiplex is one to many. Demultiplexing is a process of taking information from one input and transmitting the same over one of several output
- It is also called data distributor or serial to parallel converter.



1:4 Demultiplexer:-



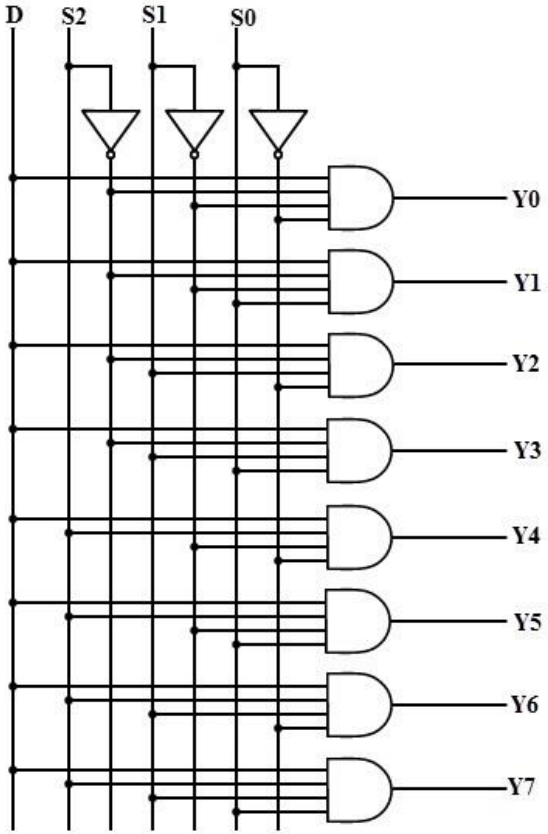
S1	S0	Y0	Y1	Y2	Y3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

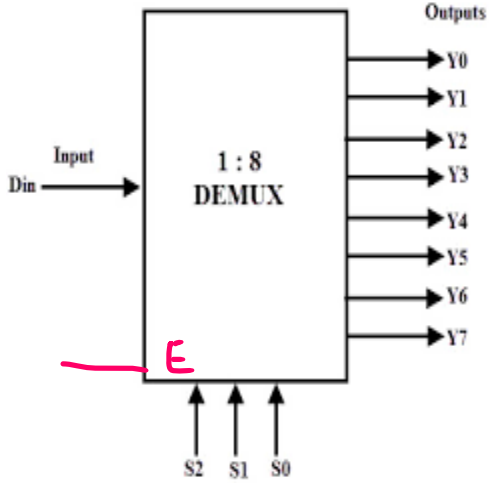


When S1S0=00,the output Y0=Din and the remaining output are '0'.

When S1S0=00,AND gate associated with the data input Y0 has two of its input is equal to 1 and third input is connected to Din. The other AND gates have at least one input equal to 0,which makes their output equal to 0.

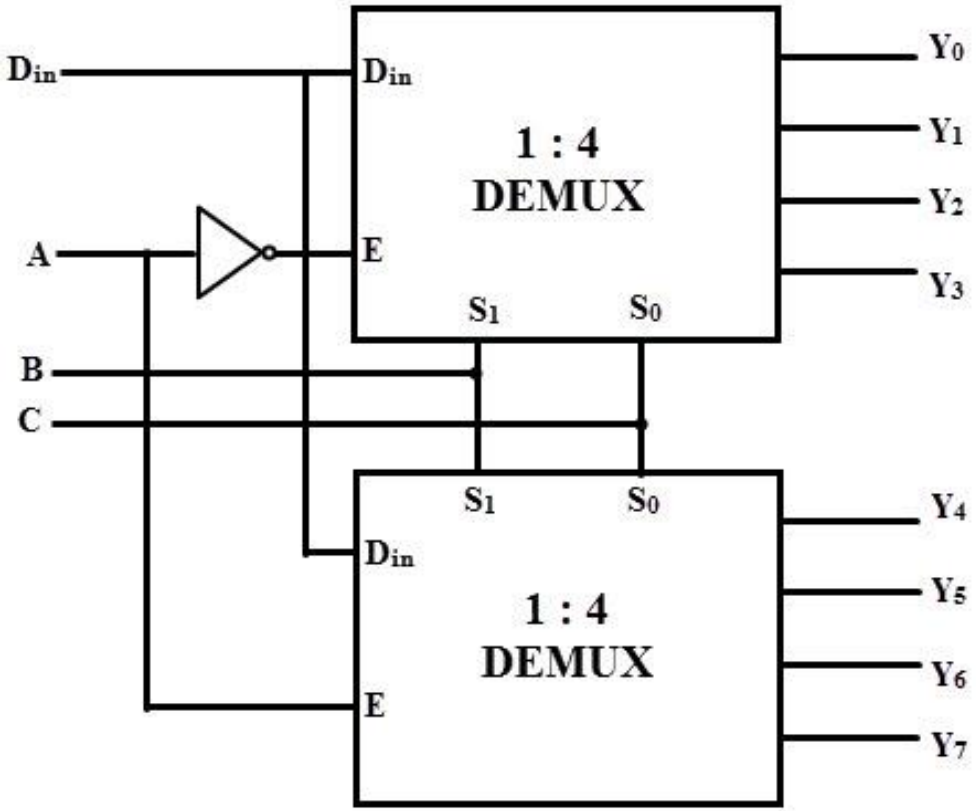
1:8 Demultiplexer:





INPUT					OUTPUT							
En	D	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	X	X	X	X	0	0	0	0	0	0	0	0
1	X	0	0	0	D	0	0	0	0	0	0	0
1	X	0	0	1	0	D	0	0	0	0	0	0
1	X	0	1	0	0	0	D	0	0	0	0	0
1	X	0	1	1	0	0	0	D	0	0	0	0
1	X	1	0	0	0	0	0	0	D	0	0	0
1	X	1	0	1	0	0	0	0	0	D	0	0
1	X	1	1	0	0	0	0	0	0	0	D	0
1	X	1	1	1	0	0	0	0	0	0	0	D

1:8 Demux Using two 1:4 Demux:



- Implement the full subtractor using Demultiplexer

Difference D=f(A,B,C)=$\sum m(1,2,4,7)$
Bout= f(A,B,C)=$\sum m(1,2,3,7)$

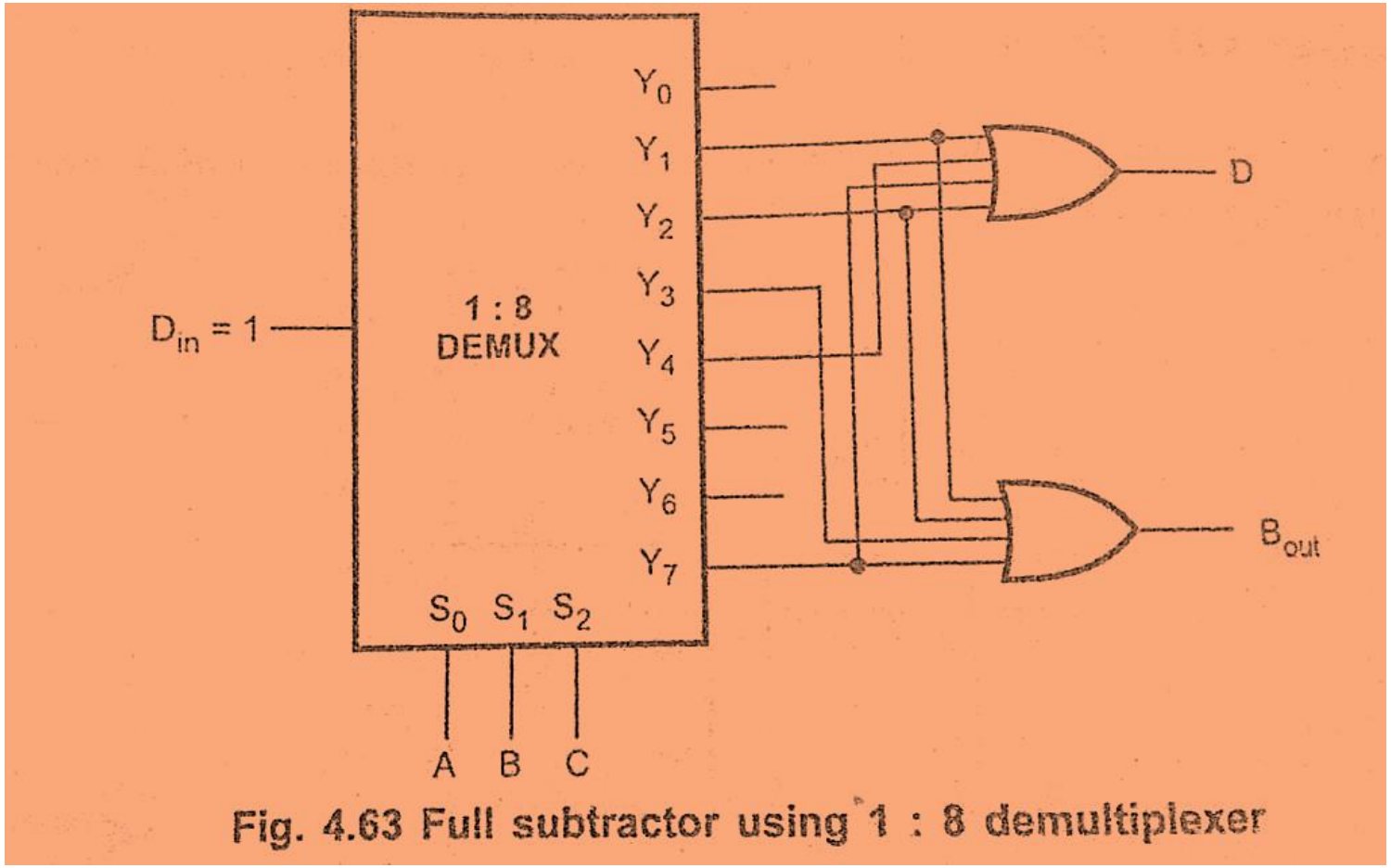


Fig. 4.63 Full subtractor using 1 : 8 demultiplexer

- Design 1:32 demultiplexer tree using 1:4 and 1:8 demux and implement following multi output combinational logic. F1=$\sum m(0,10,20,30)$

And F2=$\sum m(0,5,15,25)$

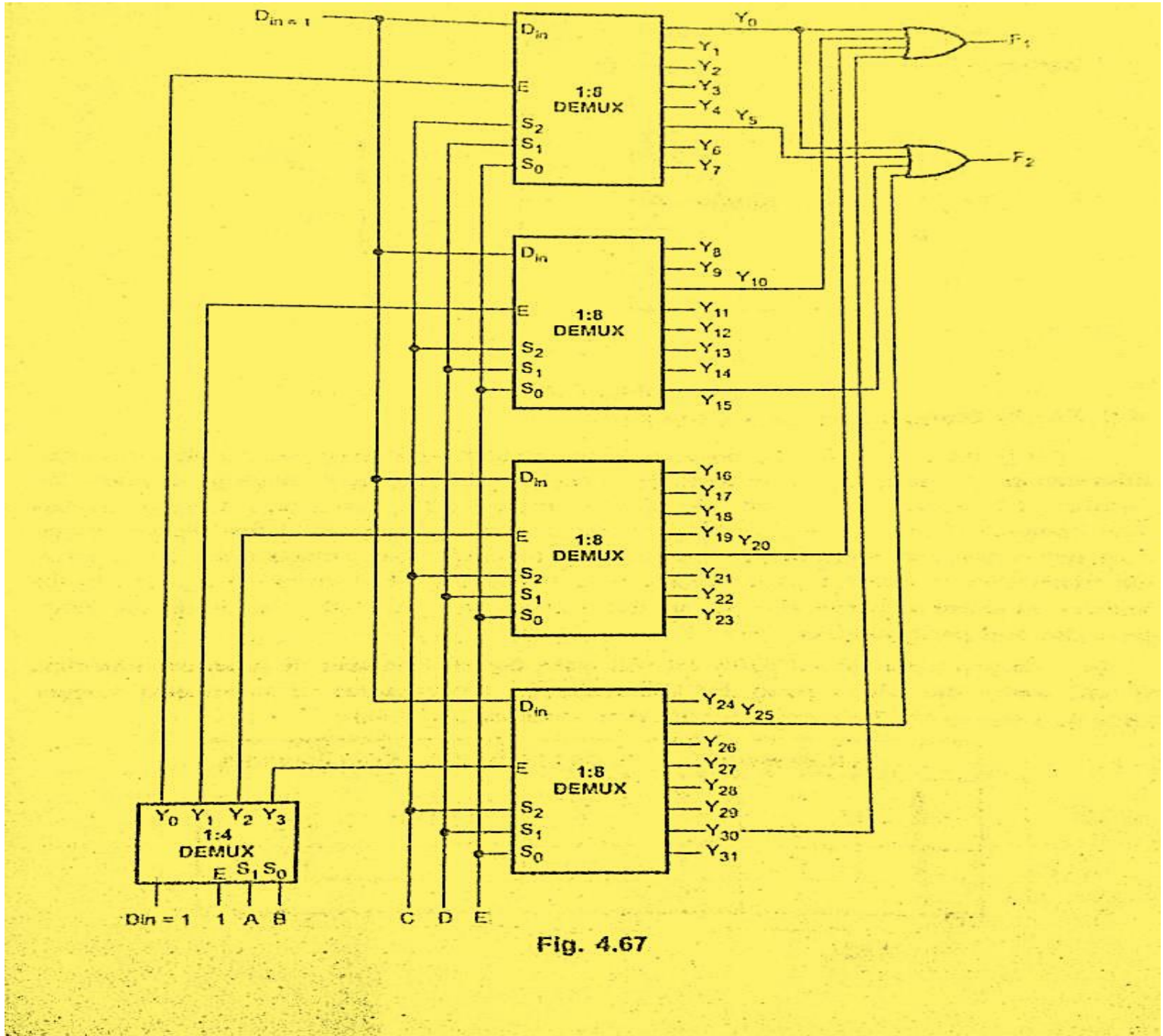
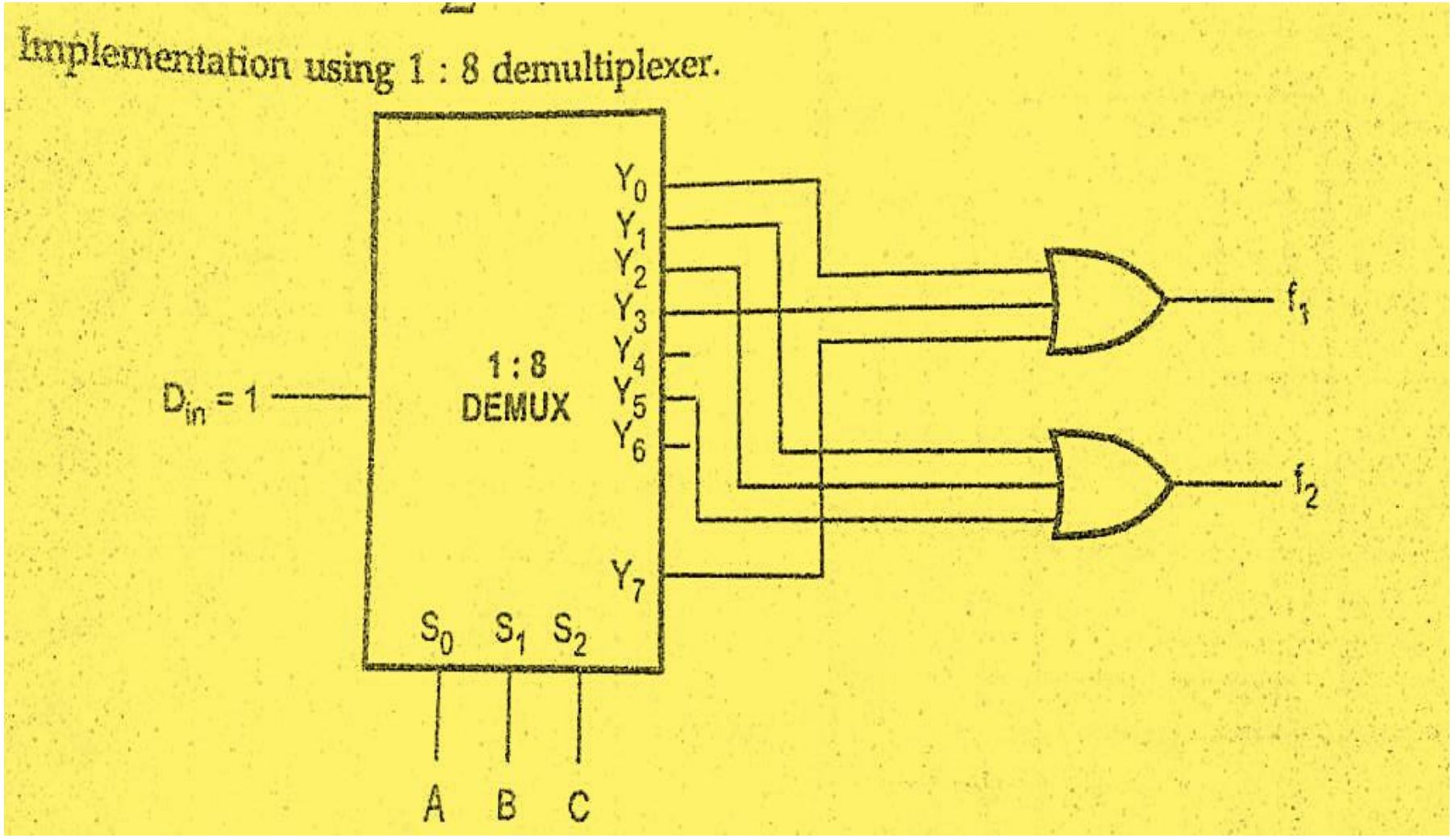


Fig. 4.67

❖ Implement the following function using Demux:f1(A,B,C)=$\sum(0,3,7)$, f2(A,B,C)=$\sum m(1,2,5)$



Parity Generator and Checker:

What is Parity Generator?

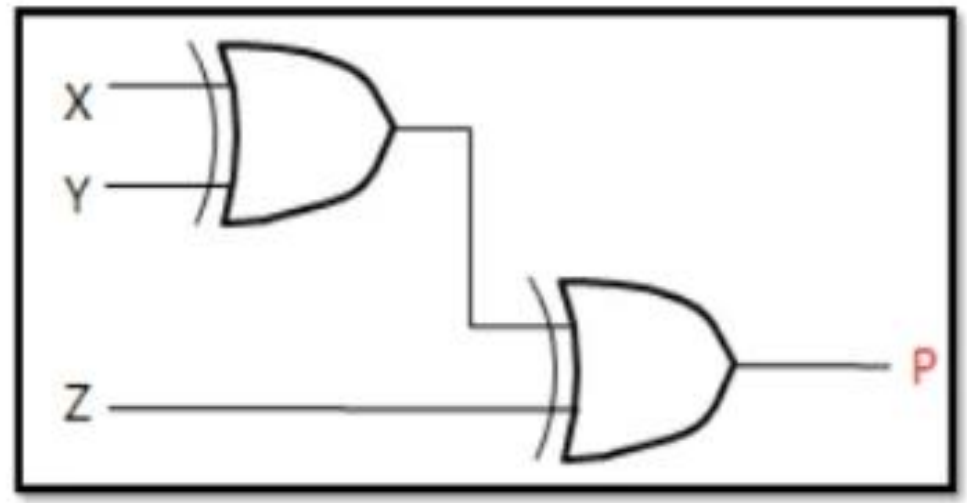
- A **Parity Generator** is a Combinational Logic Circuit that Generates the Parity bit in the Transmitter.
- A Parity bit is used for the Purpose of Detecting Errors during Transmissions of binary Information.
- It is an Extra bit Included with a binary Message to Make the Number of 1's either Odd or Even.

Two Types of Parity

- In **Even** Parity, the added Parity bit will Make the Total Number of 1's an Even Amount.
- In **Odd** Parity, the added Parity bit will Make the Total Number of 1's an Odd Amount.

Parity Generator Truth Table and Logic Diagram

3-bit Message			Odd Parity Bit	Even Parity Bit
X	Y	Z		
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1



Boolean Expression

Even Pair

$$P=\bar{X}\bar{Y}Z+\bar{X}Y\bar{Z}+X\bar{Y}\bar{Z}+XYZ$$
$$=\bar{X}(\bar{Y}Z+Y\bar{Z})+X(\bar{Y}\bar{Z}+YZ)$$
$$=\bar{X}(Y\oplus Z)+X(\overline{Y\oplus Z})$$
$$=X\oplus(Y\oplus Z)$$

Odd Pair

$$P=\bar{X}\bar{Y}\bar{Z}+\bar{X}YZ+X\bar{Y}Z+XY\bar{Z}$$
$$=\bar{X}(\bar{Y}\bar{Z}+YZ)+X(\bar{Y}Z+Y\bar{Z})$$
$$=\bar{X}(\overline{Y\oplus Z})+X(Y\oplus Z)$$
$$=\overline{X\oplus(Y\oplus Z)}$$

K-Map Simplification

X \ YZ	00	01	11	10
0	0	1	0	1
1	1	0	1	0

X \ YZ	00	01	11	10
0	1	0	1	0
1	0	1	0	1

Parity Checker

- A Circuit that Checks the Parity in the Receiver is called **Parity Checker**.
- The Parity Checker Circuit Checks for Possible Errors in the Transmission.
- Since the Information Transmitted with Even Parity, the Received must have an even number of 1's.If it has odd number of 1's, it indicates that there is a Error occurred during Transmission.
- The Output of the Parity Checker is denoted by PEC(Parity Error Checker).If there is error, that is,if it has odd number of 1's, it will indicate 1.If no then PEC will indicate 0.

Even Parity Checker:

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

AB \ CD	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

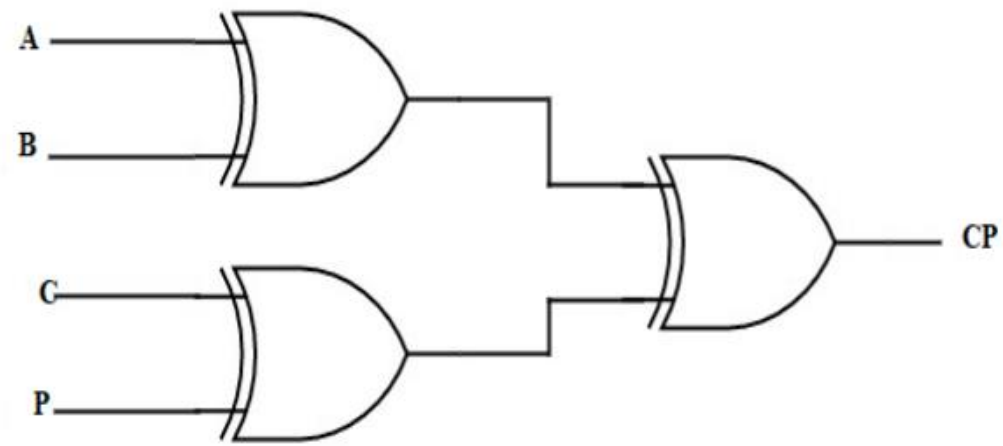
(b) $A \oplus B \oplus C \oplus D$

$$CP = \bar{A}\,\bar{B}\,(\bar{C}\,D + C\,\bar{D}) + \bar{A}\,B\,(\bar{C}\,\bar{D} + C\,D) + A\,B\,(\bar{C}\,D + C\,\bar{D}) + A\,\bar{B}\,(\bar{C}\,\bar{D} + C\,D)$$

$$= \bar{A}\,\bar{B}\,(C \oplus D) + \bar{A}\,B\,(\overline{C \oplus D}) + A\,B\,(C \oplus D) + A\,\bar{B}\,(\overline{C \oplus D})$$

$$= (\bar{A}\,\bar{B} + A\,B)\,(C \oplus D) + (\bar{A}\,B + A\,\bar{B})\,(\overline{C \oplus D})$$

$$= (A \oplus B) \oplus (C \oplus D)$$



Odd Parity Check

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

The expression for the PEC in the above truth table can be simplified by K-map as

AB \ CP	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1