| BECE102L | Digital Systems Design | L | T | P | C |
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| | | 3 | 0 | 0 | 3 |
| **Pre-requisite** | **Nil** | **Syllabus version** | | | |
| | | **1.0** | | | |

**Course Objectives**

1. Provide an understanding of Boolean algebra and logic functions.
2. Develop the knowledge of combinational and sequential logic circuit design.
3. Design and model the data path circuits for digital systems.
4. Establish a strong understanding of programmable logic.
5. Enable the student to design and model the logic circuits using Verilog HDL.

**Course Outcome**

At the end of the course the student will be able to

1. Optimize the logic functions using and Boolean principles and K-map
2. Model the Combinational and Sequential logic circuits using Verilog HDL
3. Design the various combinational logic circuits and data path circuits
4. Analyze and apply the design aspects of sequential logic circuits
5. Analyze and apply the design aspects of Finite state machines
6. Examine the basic architectures of programmable logic devices

| **Module:1** | **Digital Logic** | **8 hours** |
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Boolean Algebra: Basic definitions, Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Simplification of Boolean functions. Gate-Level Minimization: The Map Method (K-map up to 4 variable), Product of Sums and Sum of Products Simplification, NAND and NOR Implementation. Logic Families: Digital Logic Gates, TTL and CMOS logic families.

| **Module:2** | **Verilog HDL** | **5 hours** |
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Lexical Conventions, Ports and Modules, Operators, Dataflow Modelling, Gate Level Modelling, Behavioural Modeling, Test Bench

| **Module:3** | **Design of Combinational Logic Circuits** | **8 hours** |
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Design Procedure, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Decoders, Encoders, Multiplexers, De-multiplexers, Parity generator and checker, Applications of Decoder, Multiplexer and De-multiplexer. Modeling of Combinational logic circuits using Verilog HDL.

| **Module:4** | **Design of data path circuits** | **6 hours** |
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N-bit Parallel Adder/Subtractor, Carry Look Ahead Adder, Unsigned Array Multiplier, Booth Multiplier, 4-Bit Magnitude comparator. Modeling of data path circuits using Verilog HDL

| **Module:5** | **Design of Sequential Logic Circuits** | **8 hours** |
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Latches, Flip-Flops - SR, D, JK & T, Buffer Registers, Shift Registers - SISO, SIPO, PISO, PIPO, Design of synchronous sequential circuits: state table and state diagrams, Design of counters: Modulo-n, Johnson, Ring, Up/Down, Asynchronous counter. Modeling of sequential logic circuits using Verilog HDL

| **Module:6** | **Design of FSM** | **4 hours** |
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Finite state Machine(FSM):Mealy FSM and Moore FSM , Design Example : Sequence detection, Modeling of FSM using Verilog HDL

| **Module:7** | **Programmable Logic Devices** | **4 hours** |
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Types of Programmable Logic Devices: PLA, PAL, CPLD, FPGA Generic Architecture

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| **Module:8** | **Contemporary issues** | **2 hours** |
| Guest lecture from Industries and R & D Organizations | | |
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| | **Total Lecture hours:** | **45 hours** |

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| **Textbook(s)** | |
| 1. | M. Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL and System Verilog, 2018, 6th Edition, Pearson Pvt. Ltd. |
| **Reference Books** | |
| 1. | Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, 2015, 2nd Edition, Create Space Independent Publishing Platform. |
| 2. | Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2009, 2nd edition, Prentice Hall of India Pvt. Ltd. |
| 3. | Stephen Brown and ZvonkoVranesic, Fundamentals of Digital Logic with Verilog Design, 2013, 3rd Edition, McGraw-Hill Higher Education. |

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| Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test | | | |
| Recommended by Board of Studies | 14-05-2022 | | |
| Approved by Academic Council | No. xx | Date | DD-MM-YYYY |

| BECE102P | Digital Systems Design Lab | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 2 | 1 |
| **Pre-requisite** | **Nil** | | | **Syllabus version** | |
| | | | | **1.0** | |

**Course Objective**

- To apply theoretical knowledge gained in the theory course and get hands-on experience of the topics.

**Course Outcome**

At the end of the course the student will be able to

1. Design, simulate and synthesize combinational logic circuits, data path circuits and sequential logic circuits using Verilog HDL
2. Design and implement FSM on FPGA
3. Design and implement small digital systems on FPGA

**Indicative Experiments**

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|---|---|---|
| 1. | Characteristics of Digital ICs, Realization of Boolean expressions | 2 hours |
| 2. | Design and Verilog modeling of Combinational Logic circuits | 4 hours |
| 3. | Design and Verilog modeling of various data path elements - Adders | 2 hours |
| 4. | Design and Verilog modeling of various data path elements - Multipliers | 2 hours |
| 5. | Implementation of combinational circuits – (FPGA / Trainer Kit) | 2 hours |
| 6. | Implementation of data path circuit - (FPGA / Trainer Kit) | 2 hours |
| 7. | Design and Verilog modeling of simple sequential circuits like Counters and Shift registers | 2 hours |
| 8. | Design and Verilog modeling of complex sequential circuits | 2 hours |
| 9. | Implementation of Sequential circuits - (FPGA / Trainer Kit) | 2 hours |
| 10. | Design and Verilog modeling of FSM based design – Serial Adder | 2 hours |
| 11. | Design and Verilog modeling of FSM based design – Traffic Light Controller / Vending Machine | 4 hours |
| 12. | Design of ALU | 4 hours |
| | **Total Laboratory Hours** | **30 hours** |

Mode of Assessment: Continuous Assessment and Final Assessment Test

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| Recommended by Board of Studies | 14-05-2022 | | |
| Approved by Academic Council | No. xx | Date | DD – MM - YYYY |