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Design of Manchester Carry Chain Adder using High speed Domino Logic

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Abstract. Dynamic logic circuits are preferred over static logic circuits for their increased speed performance and lower power consumption. However, they are found prone to false evaluation while cascading multiple stages of dynamic logic circuits. To overcome this problem, the domino logic circuits were proposed by researchers. However, they offer reduced noise margins due to increased leakage current and charge sharing problems. In this paper, Manchester Carry Chain Adder design is explored for use with domino logic and comparison of various domino logic topologies intended for improved noise immunity and reduced leakage current against the proposed structure have been carried out. Wide fan-in gates and 8-bit Manchester Carry Chain Adder (MCC) based on various high speed domino logic circuit topologies have been designed using Cadence® using 180nm technology library from TSMC. Design of 8-bit OR gate, using High Speed Domino (HSD) topology consumes 10.8% lower power in comparison with Controlled-Current Comparison-based domino logic (C3D) topology. Furthermore, it is observed that an 8-bit Manchester Carry Chain adder using HSD topology is 5.027 times faster than C3D topology and the leakage power consumption is also reduced.

Keywords. Domino logic, Leakage Current in Dynamic Logic, Low Power Domino Circuit, Dynamic Logic Circuit, Noise immunity in Domino Logic

1. Introduction

Most of the present-day digital circuits find the conventional static Complementary Metal Oxide Semiconductor (CMOS) prevalent for their primary advantages of robustness, low sensitivity to noise, increased speed performance and lower power consumption [1, 2]. The transistor count increases with rise in the number of inputs N and the number of transistors required to implement an N -input logic gate is $2N$ [3, 4]. To realize non-inverting Boolean function at the output, it requires addition of an additional inverter stage. This increases the static power consumption and area consumption. In the case of dynamic logic, the numbers of transistors are reduced to $N+2$ and it also minimizes the static power consumption [5]. The realization of complex digital systems requires cascading which however is not possible in dynamic logic. To overcome this problem, the concept of domino logic circuit was propounded [6]. Domino logic circuit offers many advantages such as easier cascading of several stages, reduction in device count and lower power consumption, to name a few, over the static CMOS logic counterparts. In this paper, comparative performance analysis of various domino logic circuit topologies using wide fan-in gates are performed. Furthermore, an 8-bit MCC adder circuits are designed using various domino logic circuit styles for comparison.

This paper is arranged as follows. Section II presents the literature survey on Domino Logic circuits, followed by Section III with discussion on Manchester Carry Chain based Adder circuits and proposed design of using the same in domino logic. Simulation results have been explored in Section IV and Section V concludes.



2. Literature Survey

Dynamic logic comprises of a pre-charge transistor, pull down network (PDN) and an optional footer transistor. Based on the logic level of clock signal, the dynamic logic consists of two phases of operation, namely, (i) Pre-charge phase, when clock is logic LOW and (ii) Evaluation phase, when the clock is in logic HIGH state. The dynamic CMOS logic utilizes only $N+2$ transistors, whereas the static CMOS counterpart needs $2N$ number of devices. Here, N represents the number of input signals applied as fan-in to the logic gate. The static inverter connected at the dynamic node yields a non-complemented output and it also facilitates correct driving of the next stage of the dynamic cascade and this structure through its operational and logical transporting ability of signal is referred as the domino logic circuit [5].

Fig.1. illustrates the footed domino logic circuit with keeper transistor M_K . The pre-charge transistor M_{Pre} and the footer transistor M_f are controlled by the clock signal CLK at their respective gate inputs. Normally, the configuration using the footer transistor M_f is referred as Standard Footed Domino (SFD) circuit and the configuration without the footer transistor M_f is referred as Standard Footless Domino (SFLD) circuit. When the CLK is LOW, the dynamic node is pre-charged HIGH and the inverter output becomes LOW. When CLK is HIGH, the footer devices conducts and the dynamic node is conditionally discharged based on the inputs to the PDN and the output OUT attains HIGH. It is to be noted that in the domino logic, the discharge can happen only once and this imposes the condition that the pre-charge operation takes place after every evaluation [3-6]. However, if the input signal to PDN did not prove TRUE, then the state of dynamic output remains the same. The pre-charging will then happen only to compensate any charge lost due to charge sharing or leakage from the dynamic node [7].

It is an unambiguously acknowledged serious concern that technology scaling has aggravated the issue of leakage current, due to the sub-threshold conduction and thinner gate oxide layer of devices [7]. Therefore, to retain the charge at dynamic node despite various leakage current sources and charge sharing mechanisms, a weak PMOS transistor called a *keeper transistor* M_K is incorporated in the circuit as shown in Figure 1. The keeper is sized minimally, so that it avoids the *contention* between the keeper circuit and the PDN [3]. However, upsizing the keeper transistor increases the robustness, thus trading-off on the speed performance of the circuit.

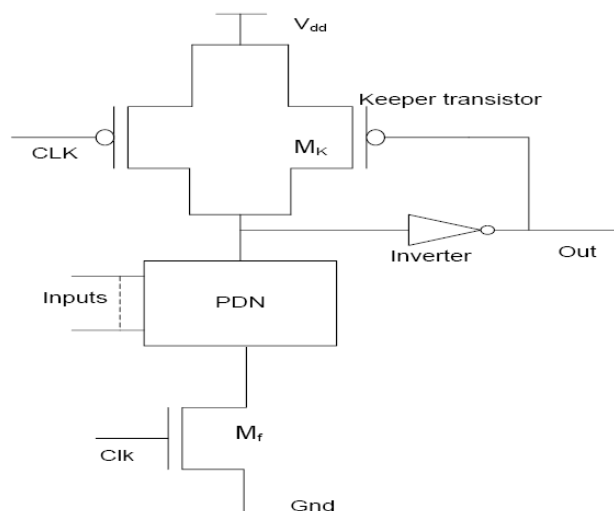


Figure 1. Conventional Domino logic

An NMOS footer transistor M_f connected as shown in Figure 1 in series with the PDN facilitates the evaluation of the circuit and it also reduces the leakage current during the pre-charge phase [2].

However, the speed of operation is reduced compared to the footless domino circuit due the stacking effect [4].

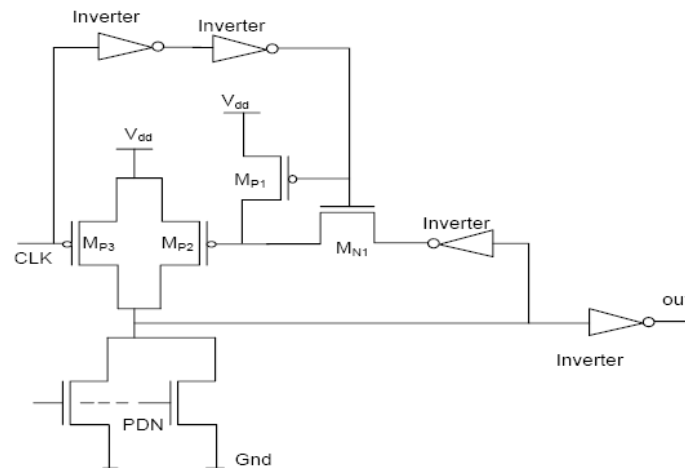


Figure 2. High speed Domino Logic Circuit [8]

2.1 High speed domino logic (HSD)

In high speed domino logic [8] shown in Figure 2, the keeper control circuit is based on delayed clock and the state of the output node. During the beginning of evaluation phase, when clock is HIGH, transistor M_{P3} is in the cut-off region and the keeper M_{P2} is initially OFF due to the delay introduced by the buffer circuit. In this manner, the contention between the evaluation network and keeper circuit is reduced and it enhances the discharge characteristics of the dynamic node. After the delay introduced by the buffer circuit, transistor M_{P1} turns OFF. At this point, the keeper circuit operation is based on the state of the output node which is controlled by M_{N1} transistor. If the dynamic node is discharged to ground, M_{P2} is OFF and it does not retain the dynamic node state HIGH. On the other hand, when the dynamic node remains HIGH, M_{P1} is ON and retains the dynamic node HIGH [3].

2.2. Controlled-Current Comparison-based Domino Logic

In the current comparison-based domino (C3D) circuit depicted in Figure 3, the current at node A and node B are compared and based on results of comparison, the state of dynamic node is determined and the effective voltage swing is reduced [9]. This makes the power consumption to be reduced and it also offers improved noise immunity along with reduced power consumption in high fan-in gates.

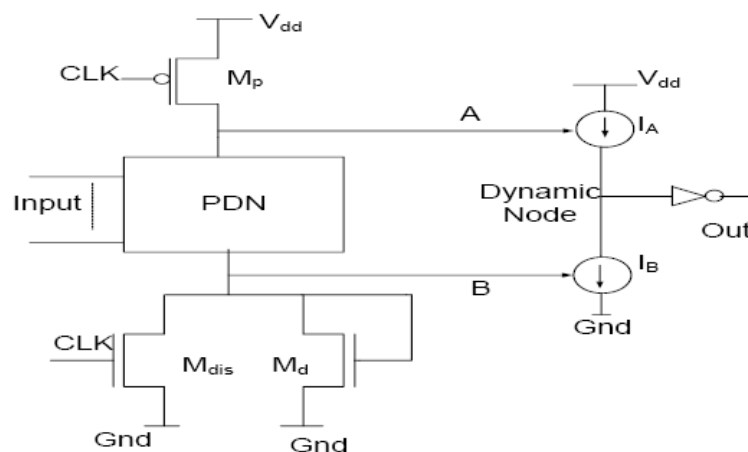


Figure 3. Controlled-Current Comparison based domino logic [9]

3. Manchester Carry Chain Adder

Adder is an important part of any Arithmetic and Logic Unit (ALU). As the number of bits required for addition increases, the power and delay increases and the performance efficiency reduces [10-12]. Furthermore, the major drawback incurred by the adder structure is its latency and the Manchester Carry Chain (MCC) eliminates this problem [13]. Figure 4 shows the high speed domino implementation for the carry generation circuit and Figure 5 depicts the carry propagation circuit. The generate bit g_i (Figure 4) and propagate bit p_i (Figure 5) are computed based on the inputs x_i and y_i initially and then, based on the state of previous carry bit, the sum and carry bits of the current stage are computed. This reduces the computation time and hence this process offers higher speed of operation [14].

In MCC adder, carry is generated, propagated and absorbed is given in Eq.1 and 2.

$$g_i = x_i \cdot y_i \quad (1)$$

$$p_i = x_i \oplus y_i \quad (2)$$

Since the carry recurrence is from the previous carry network, it is referred as Manchester carry chain adder [15, 16]. Carry recurrence is given as indicated in Eq. (3).

$$C_{i+1} = g_i + c_i \cdot p_i \quad (3)$$

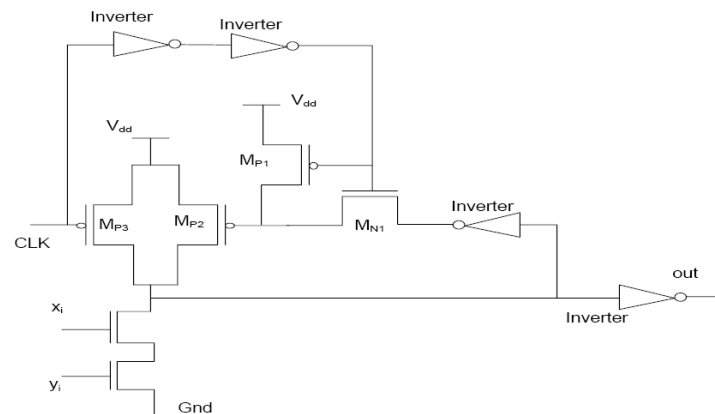


Figure 4. High speed Domino implementation for the carry generation (g_i) circuit

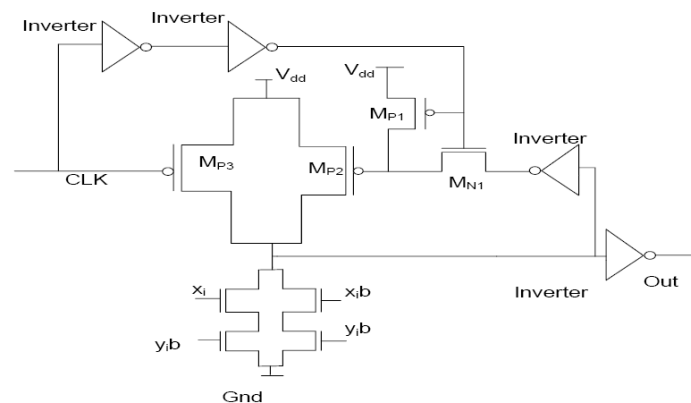


Figure 5. High speed Domino implementation for carry propagation (p_i) circuit

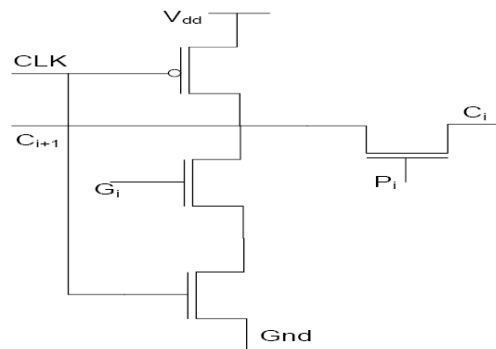


Figure 6. Manchester Carry Chain – 1-bit adder

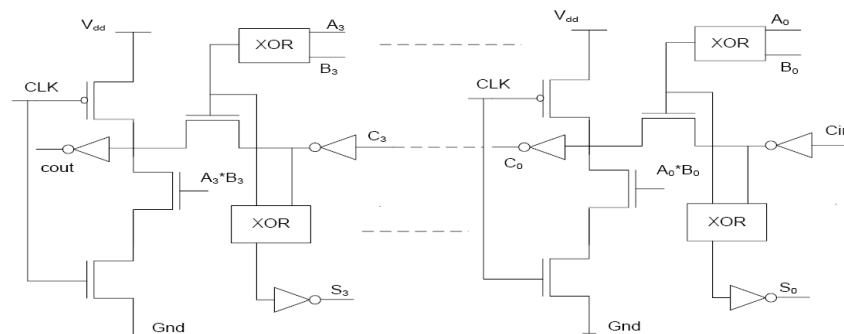


Figure 7. 4-bit Manchester Carry Chain adder without keeper

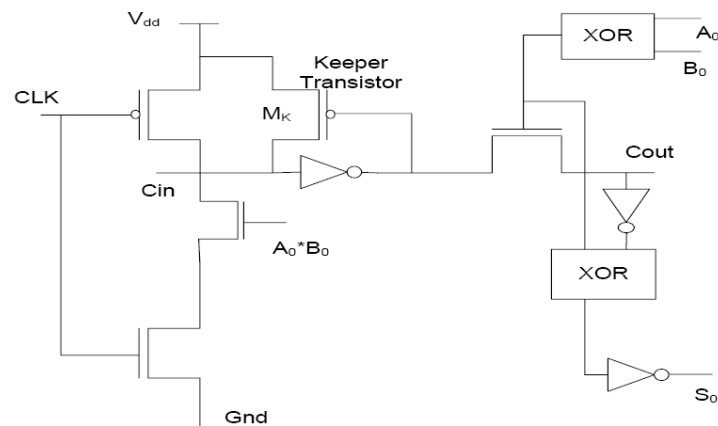


Figure 8. Manchester carry chain 1-bit adder with keeper

Figure 6 shows a single bit CMOS based Manchester Carry Chain adder where g_i and p_i is used in the computation of c_i . Figure 7 shows the 4-bit Manchester Carry Chain adder without the addition of keeper circuit. In the topology shown, four number of MCC 1-bit adder are cascaded and final C_{out} is obtained at the output node between PMOS and NMOS. The sum bit S_0 is obtained at the XOR gate's output. Figure 7 illustrates the process of the computation of c_{i+1} and propagation of the bit to next stage of the 4-bit MCC adder, where depending on the p_i and g_i value, the c_{i+1} is computed and propagated to the next stage. Figure 8 shows the Manchester carry chain using 1-bit adder with keeper device connected. Manchester carry chain 1-bit adder using HSD is shown in Figure 9. The delayed enabling of the keeper circuit during the initial evaluation phase in HSD enhances the discharge of the dynamic node in a faster pace and facilitates high speed operation.

4. Simulation and Analysis

The simulations of 8-bit OR gates with various domino logic topologies have been performed in the same simulation setup using Cadence® EDA tools and 180nm technology library. Hence, the comparison among the counterparts becomes justifiable. Table 1 depicts the speed and power metrics of various domino topologies against each other. Furthermore, a 1-bit MCC adder has been designed using HSD topology along with the conventional domino logic styles.

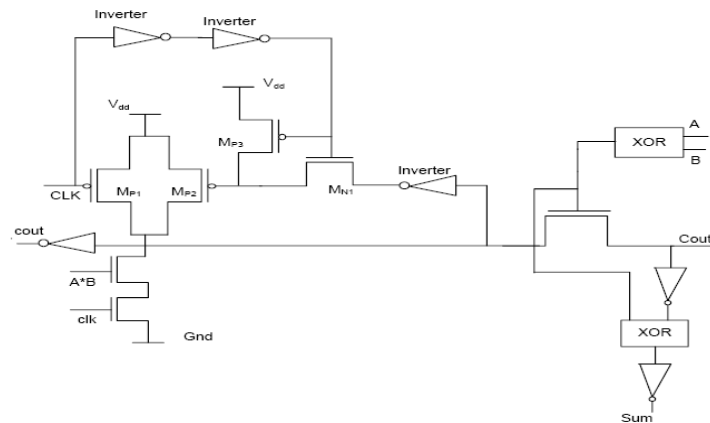


Figure 9. Manchester carry chain 1-bit adder with HSD

It can be observed from Figure 10 that high speed domino offers reduced delay of 43.9ps and leakage power value of 77.82pW while using it as a 1-bit MCC adder design. This structure incurs the minimum delay and uses reduced power. In the proposed 8-bit HSD MCC Adder, the power consumption of the circuit is reduced to 596.6μW. The delay of the circuit is negligible with respect to the delay of 8-bit Conventional MCC adders. Leakage power has reduced up to 2.162μW where Conventional MCC adder with keeper circuit and without keeper circuit has 3242μW and 1600μW. In all aspects, MCC adder using High Speed Domino logic is the fastest and most power efficient topology. The layout of 1-bit MCC adder is performed and is shown in Figure 11, and the parasitic RC are extracted to carryout post-layout simulation.

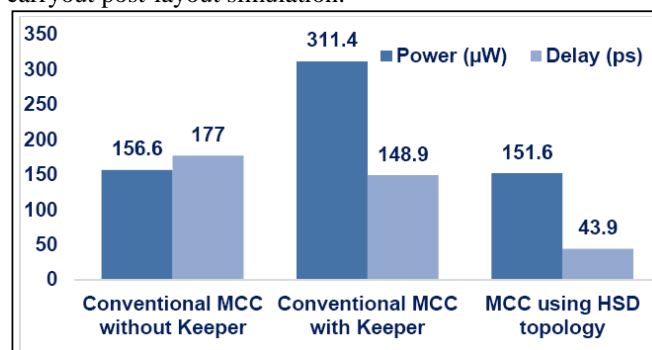


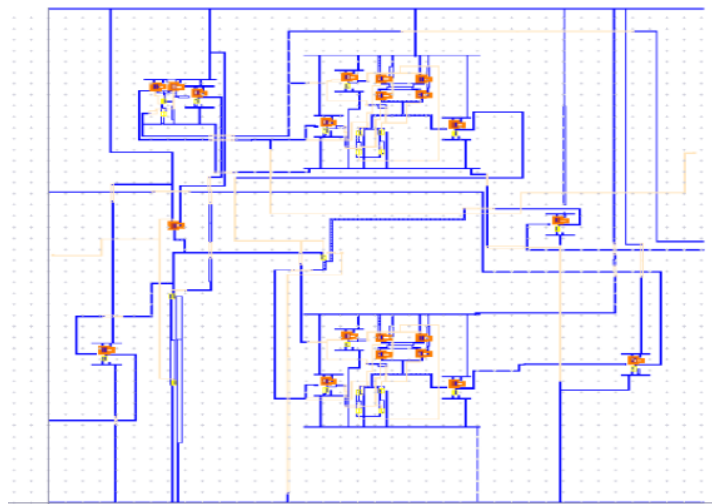
Figure 10. Analysis of 1-bit MCC Adder

Table 1. Analysis of 8-bit OR gate using various domino logic topologies

S. No.	Topology	Power (μW)	Delay (ps)	PDP (aJ)
1	Footer Domino	59.06	79.64	4703.53
2	Footless Domino	169.1	25.12	4247.8
3	High speed domino	19.56	69	1349.64
4	Controlled Current Comparison Domino	181.05	346.7	62770.03

Table 2. Analysis of 8-bit MCC adder

S.no.	Topology	Power (μ W)	Delay (ps)	Leakage Power (μ W)	PDP (fJ)
1	Conventional MCC without Keeper	9*105	30000	3242	27000
2	Conventional MCC with Keeper	9276	119.3	1600	1106.63
3	MCC using HSD topology	596.6	139.7	2.162	83.34

**Figure 11.** Layout of MCC 1-Bit adder

5. Conclusion

In this paper, comparison of an 8-bit OR gate is performed for various domino logic topologies. The simulation of a 1-bit Manchester Carry Chain adder and an 8-bit MCC adder is performed with 180nm technology node library. The simulation results demonstrate High Speed Domino logic offers reduced delay values of 43.9ps and 139.7ps for a 1-bit adder and 8-bit MCC adder respectively. It is observed that the PDP of the 8-bit MCC adder using High Speed Domino logic is 92.46% less compared to the 8-bit MCC adder using conventional domino logic circuit.

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