A Partially Static High Frequency 18T Hybrid Topological Flip-Flop Design for Low Power Application

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***Abstract*—In this brief, an extremely low power true $1-\phi$ clocking flip-flop is proposed using eighteen transistors only. The flip-flop is a synchronous bistable element that stores single-bit information. To design this Master Slave (MS) type architecture, topological, logical, and adaptive coupling techniques are employed. The minimum number of transistors are maintained by using above techniques, which comprises of complementary pass transistor logic and static complementary MOS logic. It also offers low power, a low delay that speeds up the flip-flops, and low complexity by reducing the transistor count. The proposed circuit is implemented using Cadence Virtuoso and compared with the five other reported logic structures of flip-flops. The proposed hybrid logic architecture has showed the highest percentage, i.e., 49.73% improvement in terms of power as compared to LRFF. It also improved the delay and energy efficiency (EDP). The Monte Carlo simulation has been performed for C to Q Delay for 20K samples. By reducing the number of PMOS transistors, the total area of the proposed flip-flop reduces by a minimum of 9.49% in comparison to state of the art work. The proposed circuit can work properly within a frequency range upto 1 GHz. It is also compared with reported 18T TSPC flip-flop.**

***Index Terms*—Switching activity, CMOS, low power, flip-flop, Monte Carlo complementary pass transistor.**

I. Introduction

THE BASIC storage element extensively used in digital system designs is a flip-flop. The flip-flop is extensively used in low power electronics applications such as smartphones, mobiles, tablets, and other hand-held devices. For long battery life, each device should have low power consumption. At the same time for fast processing speed, delay of the memory units should also minimum [1], [2]. In digital hardware circuits, the clock system itself consumes 20% to 40% of the total power consumption of the Integrated Circuit (IC) [3]. The flip-flop designs undergoing continuous improvements by implementing multiple low power techniques.

The Set Reset flip-flop (SRFF) is the conventional flip-flop, and Transmission Gate flip-flop (TGFF) [4] is the most widely used industry standard flip-flop shown in Figure 1. The major problem with these designs is the clock overloading [5], [6]. These flip-flop logic structures consist of two clock signals, i.e., *CLK* and $\overline{CLK}$ respectively. These signals not only increase the workload of the clock signal but also increases the number of the transistors. In the overall design structure due to the extra circuitry required for generating the *CLK* and $\overline{CLK}$ signals [1], [7]. The outcome of which, a significant increase in dynamic power losses, even at low data switching activity. Nowadays, the cost of production and chip area are also the major concerns for the VLSI industry. Every field of this digital world demands device that has low cost and compact. Hence minimizing the silicon area occupied by processors is a crucial consideration.

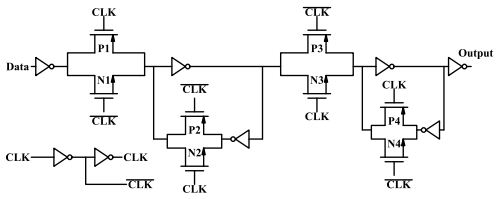

Fig. 1. CMOS circuit of TGFF [4].

Low power flip-flop techniques are used to avoid the extra load on clock signal. The flip-flop design logic such as True Single Phase Clocking (TSPC) has been developed with the intention to alleviate clock load. Because, as the clock load increases, power consumption also increases even when the input remains static [7], [8], [9], [10]. Application Specific Integrated Circuit (ASIC) and Real-Time Embedded system demands low power and high-speed flip-flops. The technology scaling also leads to an increase in demand of new flip-flop designs operated at lower voltage [2], [11].

In this brief, a hybrid logic is used for flip-flop design. The proposed flip-flop structure addresses the significant improvement in (1) Clock to Q delay when compared with the existing M-S flip-flops. (2) This work doesn't have clock overloading problem also, that helps in reduction in power consumption. (3) Reduction in the PMOS transistor count, that reduces the delay and area as well as the power of the overall circuit. (4) Lowering the overall complexity. All the results were obtained at 65nm UMC CMOS technology at room temperature using Cadence Virtuoso at 0.7 V supply voltage and a maximum clock frequency of 1 GHz. Moreover, Monte

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Carlo simulation of Clock to Q delay for the proposed and 18TSPC [7] flip-flop is presented.

II. Review of Flip-Flops Topologies

In order to evaluate the basics of flip-flops, some existing flip-flop designs are reviewed [8]. The conventional SR flip-flop and currently used TGFF designs have additional circuitry for generating the clock signal [14]. The TGFF suffers from higher clock loading problem since, only a single clock is used to drive 12 transistors. The consequence of clock overloading is a considerable amount of hike in power consumption. To alleviate the power consumption of flip-flop designs such as Adaptive Couple flip-flop (ACFF) [6], Topologically Compressed (TCFF) [1], and Logic Structure Reduction flip-flop (LRFF) [3] have been reported.

In ACFF design unlike the conventional SRFF design, a differential latch is used to achieve TSPC operation. Here transmission gate is replaced by pass transistors and two-level restoring (LR) circuits. Each LR circuit having one NMOS and one PMOS in parallel. Only 4 transistors are driven by the clock out of 22 transistors [9]. The ACFF slave latch suffers from data conflict problem. As switching activity increases, it decreases even more.

By replacing the master of SRFF by a multiplexer, we can reduce the clock loading and leads to a TSPC FF design named as (TCFF) in [1]. Through topologically compressed scheme, power dissipation reduces due to a single clock signal used. The TCFF also reduced the transistor count with respect to SRFF.

The LRFF is the enhanced version of TCFF and it consists of a complementary pass transistor logic (CPL) structure. This splits the discharging path of the slave in TCFF into two paths [12]. The CPL structure consists of a pass transistor having clock as input to the gate terminal and node 2/node 3 as the sink. In slave side there is two charging path that consists of two pass transistor with CPL structure. It helps in charging the node 4 and node 5 to logic high "1".

A single edge implicit pulse-triggered level-converting flip-flop with a conditional clock technique (CC-LCFF) was reported. This is suitable for low-power, non-critical paths with Dual-VDD [13].

III. Proposed Flip-Flop Design

For achieving lower delay, decreasing the circuit complexity and optimizing the power consumption, we have topologically and logically reduced the number of the transistor especially PMOS transistor. Due to the low mobility of the PMOS transistors, we have reduces the continuous 2 PMOS (i.e., in ACFF) transistors in the same path from VDD to GND. This leads to reduction in delay of the proposed flip-flop. Moreover, the proposed design consumes lesser area as compared to LRFF, due to low circuit complexity. Figure 2 shows our proposed design, named as a Hybrid flip-flop (HFF). Since, it comprises logic reduction and balance clock as well. The proposed hybrid structure consists of both LRFF and ACFF that meet the requirements by using only 18 transistors. The hybrid topological structure consists of 4 pass transistors (P2, P3, N6 and N7),

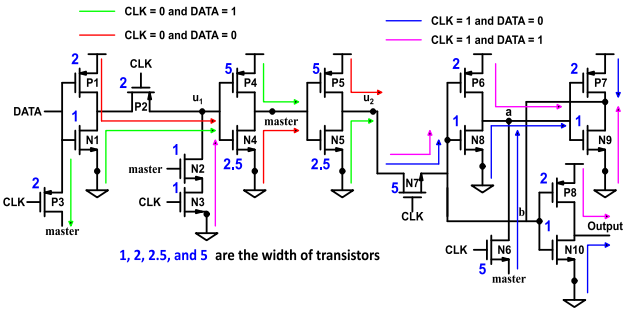

Fig. 2. CMOS circuit of proposed work.

two NMOS to hold data in master transistors and 6 inverters. Among the four pass transistors, one pair of pass transistors behaves as an auxiliary transistor (AT) in order to deliver weak 0 or Strong 1. Other pair of pass transistor behaves as a current booster (CB).

A. Data Latching Cases

1) Case (Data = 0 and Clock = 0): When CLK = 0 and DATA = 0, P1, P2, and N4 transistors will be in ON state, that makes node "u1" to be equal to 1. But "master" node and node u2 will not deliver any data to slave latch, because transistors N6 and N7 are OFF. Hence slave will hold its previous value at the output node. In this condition transistor P3, behaves as an AT since it passes weak 0 at the "master" node. The transistor P2, behaves as current booster because it passes strong 1 that conforms the logic 0 at master node.

2) Case (Data = 0 and Clock = 1): When CLK = 1 and DATA = 0, transistors N6 and N7 will be in ON state. The data stored at the "master" node and node u2, feeds to slave nodes "a" and "b", via N6 and N7 respectively. This provides the data at the output through the slave. When master node output is 0, N6 is a CB, as it passes strong "0" at node "a". At the same time N7 is an AT, as it passes weak "1" at node "b".

3) Case (Data = 1 and Clock = 0): When CLK = 0 and DATA = 1, transistors N1, P2 and P4 will be in ON condition. That pulls node u1 and u2 to logic "0", while master node retains the data at logic "1". The slave will hold its previous value at the output node. In this condition transistor P2, behaves as an AT, as it passes weak 0 at node u1. Where as transistor P3, behaves as a CB, as it passes strong 1 at master node.

4) Case (Data = 1 and Clock = 1): When CLK = 1 and DATA = 1 logic at the master node will be transferred to slave similar to the above case as CLK = 1. When the master node output is at logic "1", N7 behaves as a CB, as it passes strong "0" at node "b". At the same time N6, behaves as an AT, as it passes weak "1" at node "a".

IV. Experimental Results

A. Output Waveform and Internal Node Voltage of HFF

Figure 3 indicates internal node voltages of the proposed Hybrid flip-flop, in which all nodes are static except node u1. The node voltage of u1 introduces small fluctuations but, logic remains at the same level hence circuit is partially static. The

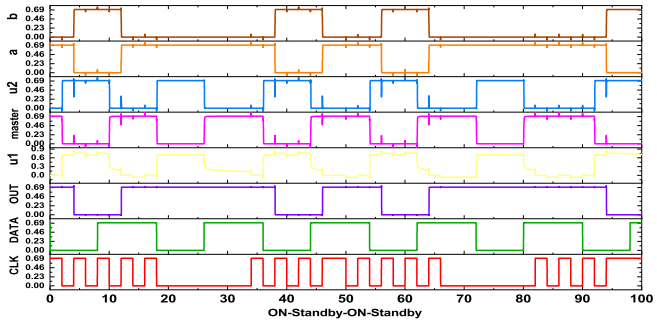

Fig. 3. Running condition of HFF in the ON-Standby-ON mode in random data and clock input with clock frequency 250 MHz at 0.7 V.

maximum peak of glitch at node u2 is $\approx 12.58\%$ while voltage required to turn on the next transistor is $\approx 43.71\%$. This is too higher than the peak glitch value. So, these glitches will not affect flip-flop operation.

To compensate these fluctuations, transistors P4/N4 and P5/N5 have aspect ratio of 5W/2.5W. All the nodes are providing rail to rail swing. The rise time of the CLK and Data is taken as 10 ps for static timing analysis. The change in output is occurring at every rising edge of the clock pulse. The output node, "a", and "b" are always static.

B. Restoration From the ON-Standby-ON Mode

The clock signal is suspended perpetually, when it is in the standby mode. This work is a partially static flip-flop, it might undergo in voltage deterioration in the standby mode because of floating node in the circuit. Recommencing of clock signal is the wakeup mode, and loading of flip-flop with entirely a new input data. So that, the flip-flop can restart its operation instantly and employ in any logic transitions immediately after restarting the clock signal. There is no need of signal recovery time to restart its operation. To validate the claim, a simulation setup is created for input data. This simulation process starts with five clock cycles normally. Afterwards, six clock cycles for a standby mode, and the clock signal is recommenced again for a fresh input data setting. The simulated output waveforms are depicted in Figure 3. The proposed Hybrid flip-flop has been simulate at a supply voltage of 0.7 V.

C. Leakage Power, Delay and Frequency vs Power Relation

Figure 4(a) depicts the leakage power consumption in terms of average power in the standby mode. This is performed for different possible combinations of clock and input logic of Master-Slave latch [CLK, D (M/S)]. When CLK = 0, Master will process the data and slave will hold the previous output. When CLK = 1 Master will hold and slave will process the Master's output. Therefore only two combinations exist for CLK = 1 and four for CLK = 0. The proposed circuit consumes 23.847 nW of avg. power in standby mode which is more than TGFF. All other reported master-slave flip-flops are having more leakage power consumption. This work has lowest power consumption, but the leakage power is inferior to the conventional TGFF.

Clock to Q delay and Data to Q delay is minimum with respect to the existing flip-flop designs as indicated in Figure 4(b). Since, PMOS's have been removed from the slave of the LRFF and TCFF. Due to this the timing performance of the proposed work meets the demand of the VLSI technology. The TCFF and LRFF are better circuits in terms of C to Q delay and logic applied to reduce the transistor count.

Figure 4(c) depicts that the proposed HFF circuit has the lowest power consumption among all other different flip-flops designs. As observed from the plot, when the frequency varies from 1 MHz to 1 GHz. Initially, power is linearly increasing but after the 100 MHz, power consumption is minimum. All the other designs are behaving similar to the proposed one except SRFF and TGFF. Because, both uses *CLK* and $\overline{CLK}$ in their operation that results continue to increase in power.

Table I tabulated the feature comparison of various existing data retention flip-flop designs at the frequency 500 MHz and supply voltage at 0.7 V. The number of transistors in the proposed HFF circuit is eighteen. This is least among the existing different flip-flop techniques. A comparison is made at the data switching activity of 12.5%. It shows the lowest power consumption and the lowest layout area among all existing M-S flip-flops. Since, it has a lesser number of PMOS transistors than LRFF and ACFF.

D. Variation of Power With Supply Voltage

The power consumption level for different supply voltages ranging from 0.5 V to 1 V is in Figure 5(a). The HFF is working properly at this voltage range, and it has lowest power consumption among state of art work. This is due to the critical path of the proposed flip-flop consists of lesser number of transistors. This is achieved by the Removal of PMOS from the circuit without affecting the functionality.

E. Process Corner and Switching Activity

Figure 5(b) depicts the comparison of different corners of all existing with the proposed flip-flops. Our design leads at each process corners (TT, SS, SF, FS, FF). Process corners analysis shows the reliability of the flip-flop.

The comparison is made at a switching activity of 12.5%, supply voltage of 0.7 V, and 27°C. It is observed that, HFF is the most power-efficient circuit. The comparison is made at varying data 8 times, 4 times, 2 times, 1 time and 0 time for 8 active high clock pulses for switching activity factor of 100%, 50%, 25%, 12.5% and 0%. The proposed design is having 51.11%, 37.3%, 36.54%, 35.079%, and 37.33% of power saving at switching activity respectively as compared to the LRFF circuit in Figure 5(c). The SRFF and TGFF have poorest power consumption because, the *CLK* and $\overline{CLK}$ generation circuit also consume power. All other reported flip flops are using CLK only. Hence remaining flip-flops have approximately similar but increasing power consumption for the range of 200 MHz to 1 GHz. Figure 5(d) shows Energy-Delay-Product (EDP) vs Technology scaling plot to investigate energy efficiency of the proposed work with [7]. It is observed that our proposed design is energy efficient at 65 nm, 40 nm and fin-FET (18 nm). Moreover, at 28 nm the EDP is marginally higher due to more leakage as compare with [7].

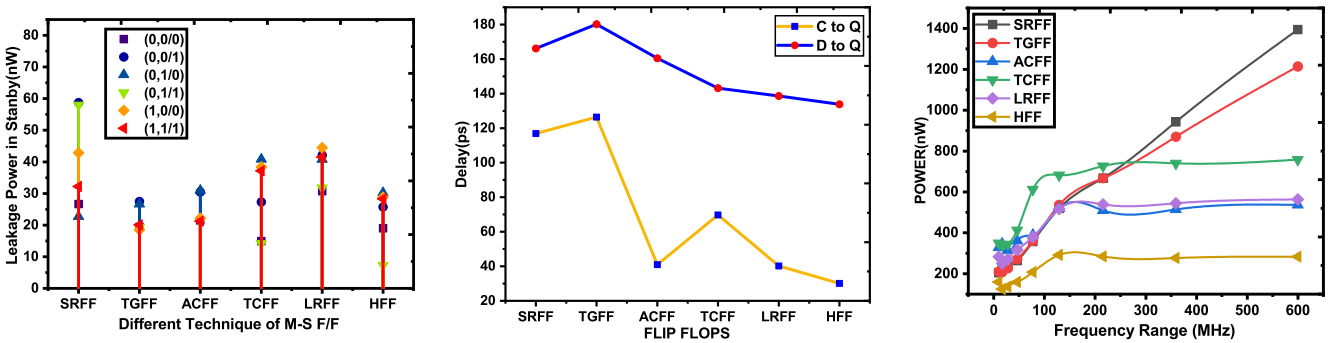

Fig. 4. (a) Leakage power comparison in standby mode. Each line in the graph of different colour is showing different mode. (b) C to Q and D to Q Delay variation of different flip-flops. (c) Frequency versus Power plot.

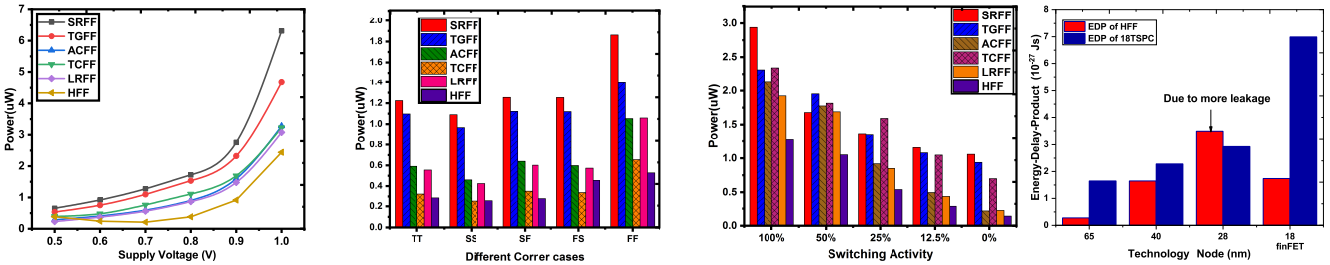

Fig. 5. (a) Power consumption of HFF at different power supply voltages. (b) Process corner analysis in terms of power of different flip-flops.(c) Power comparison of different flip-flops at different switching activity. (d) Energy-Delay-Product vs Technology Node.

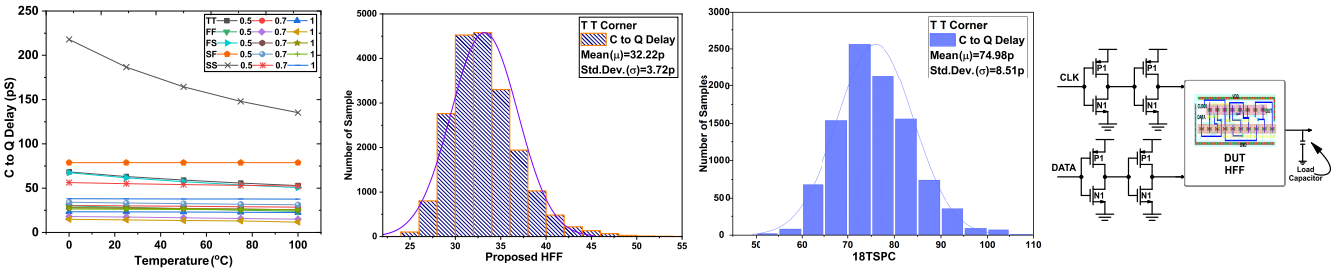

Fig. 6. (a) HFF PVT analysis 0.5 V, 0.7 V and 1 V, Temperature 0, 25, 50, 100 degree. (b) Monte Carlo simulation of C to Q delay for 20K samples of Proposed HFF (c) 20K samples of 18TSPC at 27°C. (d) Test Circuit.

TABLE I
OBSERVATION OF DIFFERENT FLIP-FLOP CIRCUITS AT 500 MHz/@0.7 V/@27°C/TT CORNER AND 65NM TECHNOLOGY NODE

FF Designs	SRFF(Conv.)	TGFF[14]	ACFF[6]	TCFF[1]	LRFF[3]	**This work**	18TSPC[7][a]	**This work**[a]
Transistors	30	24	22	21	19	18	18	18
Layout Area (um^2)	63.36	37.56	35.67	31.26	30.16	26.03	28.76	26.03
Setup Time (ps)	49.12	53.71	119.5	73.24	88.37	103.6	61.7	103
Hold Time (ps)	-23.12	-18.62	-49.78	-29.3	50.21	-57.8	-24	-57
Clock to Q Delay (ps)	116.9	126.4	40.98	69.77	40.17	31.19	76.3	32.2
Data to Q Delay (ps)	166.1	180.1	160.5	143.1	138.6	134.8	137.8	135.3
Avg. power (uW)	1.277	1.099	0.594	0.760	0.561	0.282	0.284	0.272
EDP_{CQ} ($10^{-}27Js$)	17.418	17.443	0.995	3.699	0.905	0.272	1.652	0.281
EDP_{DQ} ($10^{-}27Js$)	35.229	35.659	15.3	7.59	10.783	5.237	5.392	4.985

[a] 25^{O} C and supply voltage of 0.6 V at same node 65nm.

For the static timing analysis, the setup time and hold time are calculated. By taking, data hold time as infinite for setup time, and setup time as infinite for hold time. The setup time and hold time for the proposed circuit is 103 pS and −57 pS as in Table I. The setup time of the proposed FF is lower than the ACFF and hold time is nearly equal to SRFF. The proposed flip-flop circuit has improved setup and hold time.

F. Process Voltage Temperature (PVT)

To check the robustness of the proposed flip-flop in all physical conditions, the PVT analysis is performed, as shown in Figure 6(a). In this work all the process corners (TT SS SF FS FF) with respect to temperature ranges from 0°C to 100°C, while the voltage ranges from 0.5 V to 1.0 V have been used. It is observed from the PVT variation, the proposed flip-flop

is working properly in the respective range of process voltage and temperature.

G. Comparison at Same Node 65nm

The 18TSPC flip-flip is the best circuit among the reported works. In this brief we have followed same environment as in [7], for the better comparison. In the Table I, column 8 and 9 tabulates that our propose circuit is superior than 18TSPC [7]. Since, there is no redundant ON transistor in HFF as compared to the 18TSPC (when CLK = 1, D = 0 and CLK = 1, D = 1). This work has more setup time than 18TSPC and less hold time. At the same time Clock to Q delay is much smaller than [7]. Moreover, the proposed work is also 5% better in terms of power consumption. From the layout, it is observed that the HFF takes 9.77% less area than 18TSPC.

The Monte Carlo simulation for Clock to Q delay has been performed for 20K samples at 27°C for HFF and 18TSPC [7] in Figures 6(b) and 6(c) respectively. Standard deviation (σ) and Mean (μ) values of [7] are 8.51 ps and 74.98 ps respectively. Standard deviation (σ) and Mean (μ) values of HFF are 3.72 ps and 32.22 ps respectively. The percentage yield is 99.73%, i.e., more than 98 percent confidence level. Hence the proposed work is outperformed as compared to 18TSPC [7].

H. Test Circuit and Layout of the Proposed Flip-Flop

The model test setup for flip-flop is depicted in Figure 6(d). The input signals are provided by passing through two similar inverters. The size of the inverter is determined to be 0.4/0.2 for PMOS over NMOS. The first inverter is used to establish the slew rate (i.e., the rise time and fall time delays). The next inverter is employed to driving stage of the proposed flip-flop design, and its power is taken into consideration for measurement. Since, this flip-flop have pass-transistor logic at the input stage, which draws the power directly from the driving logic rather than VDD. For a fair comparison, this power loss must be included. The output of the flip-flop was loaded with a 10 fF capacitor load.

This flip-flop consists a temporary contention path in the slave circuits which was eliminated, by using the transistors of higher width. The transistors N6 and N7 as well as P4, N4, P5, and N5 have higher width. This maintains the flow, from master to slave side. because correct path should always wins the fight, for the correct operation. Hence, the proposed flip-flop is successfully achieved contention free operation. To support the proper operation of this work, process voltage and temperature (PVT) variation has been performed. Moreover, for reliability Monte Carlo simulation has also performed.

The layout of the proposed HFF is shown inside the test circuit in Figure 6(d). The standard cell layout area of the proposed flip-flop is least among all other flip-flops designs. As proposed HFF circuit has more number of NMOS transistors as compared to PMOS transistors, so occupies least area. It is observed from the Table I, that HFF has lesser area of 36.14%, 15.11% and 9.49% as compared the ACFF, LRFF, and 18TSPC respectively.

V. Conclusion

In this brief, a new flip-flop is designed by using 18 transistors. For the proposed work, we have considered following parameters, which are C to Q delay, reduction in PMOS transistor count, no clock overloading, and lowering circuit complexity. The proposed circuit outperformed by 52.52%, 62.89%, and 49.73% in terms of power consumption as compared to ACFF, TCFF and LRFF respectively. In terms of leakage power our circuit excelled by 4.20%, 19.27% and 39.75% when compared with ACFF, TCFF, and LRFF respectively. It also excels in performance at different supply voltages, frequency range and does not have clock overloading. All the parameter taken for this work have been successfully addressed. The proposed design is also compared with the 18T TSPC FF. In which we are getting comparable results and in some comparison, proposed circuit excels over 18T TSPC and hence proves the efficiency.

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