Delta Sigma Modulators for Fractional-N Phase Locked Loops

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***Abstract*—Delta Sigma Modulators can be used to design Fractional-N Frequency Sythesizers. In the project, different topologies of Delta Sigma Modulators have been discussed. These topologies have been designed in Cadence Virtuoso in 65nm TSMC technology. Hardware synthesizable code of these topologies haven been written in Verilog, and output obtained in Oscilloscope using Zedboard.**

I. Introduction

Block diagram of a typical Phase-Locked Loop (PLL) frequency synthesizer is shown in Fig 1. The feedback in the PLL drive output frequency f_{PLL} towards Nf_i where N is the frequency division achieved by the Frequency Divider. This divider can achieve only integer division. So, for frequency division, we need to design circuits to provide inputs to dual or multi-modulus frequency dividers such that on average fractional division occurs.

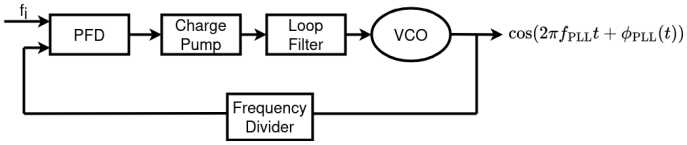

Fig. 1: Phase Locked Loop

This was initially done using accumulator(Fig 2) and the method was called pulse swallowing. The carry output of the accumulator is such that the average value of its output is $\frac{K}{2^k}$ where K is the input to the accumulator and k is the number of bits of the accumulator. If we use a dual modulus divider which divided by n+1 when the carry output is 1 and n otherwise, the average frequency division achieved is

$$f_{av} = N + \frac{K}{2^k} \tag{1}$$

In this project, the use of Delta Sigma Modulators for fractional-N Frequency Division has been explored.Hardware synthesizable verilog code for these modulators have been done and tested in Zedboard using Xilinx Vivado. Using peripheral module(PMOD) in the Zedboard, the output has been obtained in oscilloscope. The different topologies haven also been designed in 65nm Technology in Cadence Virtuoso using a high speed low power hybrid adder using Manchester Carry Chain.

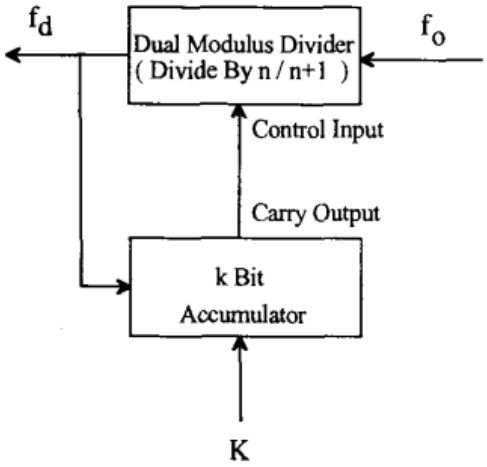

Fig. 2: Digital Accumulator [2]

The different topologies of Delta Sigma Modulators implemented are:-

1) First order Delta Sigma Modulator
2) Second order Delta Sigma Modulator
3) Mash 1-1-1 Delta Sigma Modulator

II. Adder Implementation

A Hybrid Adder containing Carry Look-Ahead and Carry Select Adder blocks have been used. The block diagram of the adder is shown in Fig 3. The generate and propogate blocks produce generate G_i and propogate P_i signals corresponding to bits A_i and B_i respectively by AND and XOR respectively implemented in domino logic. Using these, the first level 4-bit carry look ahead(Fig 4) block implemented using Manchester Carry Chain generates group generate $G_{i+3:i}$ and $P_{i+3:i}$ using which the second carry look ahead block(Fig 5) generates carry inputs to Carry select adder. This is also implemented using Manchester Carry Chain. The carry select adder of 4-bits(Fig 6) implemented again using Manchester Carry Chain have been used. They produce carry outputs corresponding to input carry '1' as well as '0'. Then, based on carry from second carry look ahead block, one of the output is selected using multiplexer(Fig 7 (a)). Finally, the carry C_{i-1} from Carry Select Adder is XORed with propogate signal P_i to get the

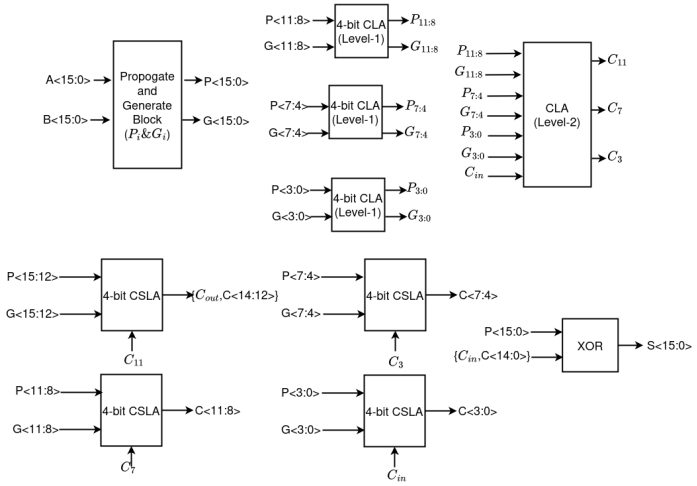

Fig. 3: Low Power High Speed Hybrid Adder

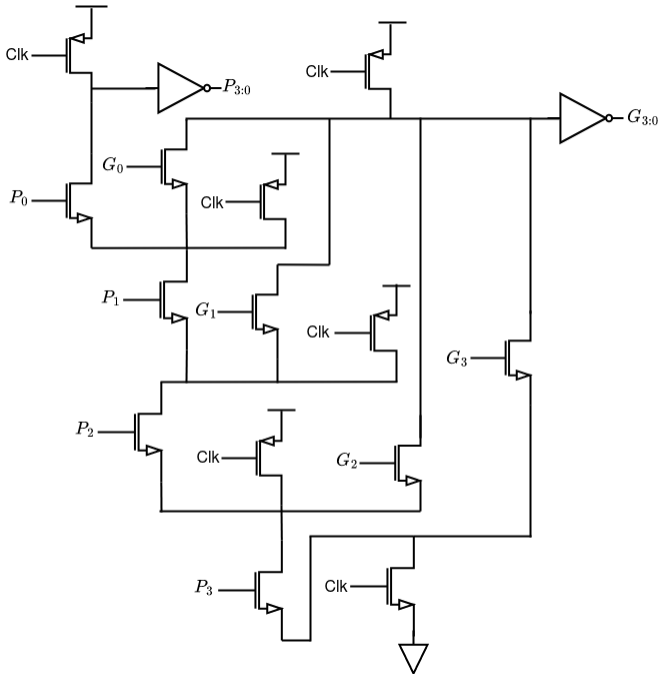

Fig. 4: 4-bit Carry Look-Ahead Adder

sum bit. This XOR is implemented with multiplexer(Fig 7(b)) rather than domino logic as output of propogate is generated much earlier than that of Carry Select Adder. Due to this, the output will be incorrect in cases where P_i and C_{i-1} are both '1'.

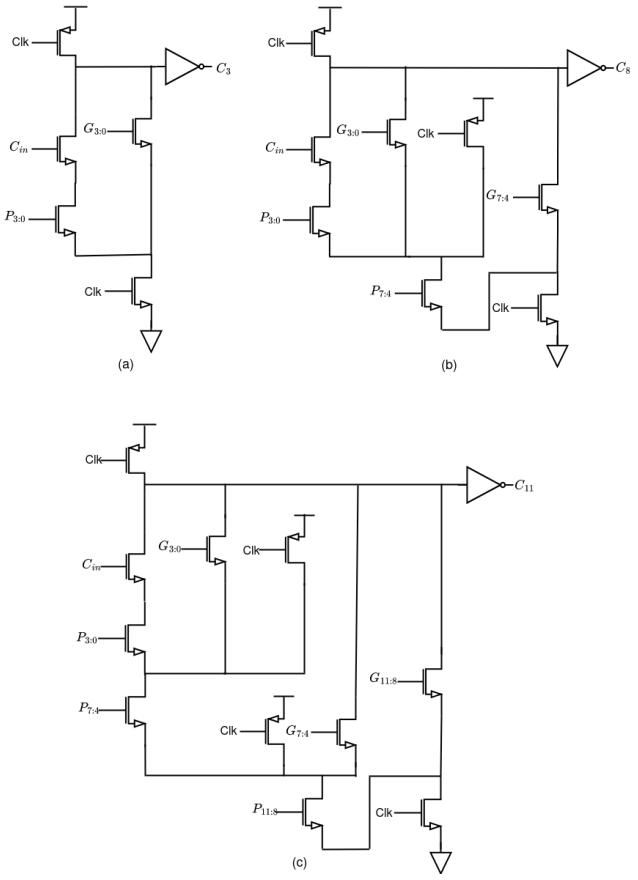

Fig. 5: Level-2 Carry Look-Ahead Adder Block

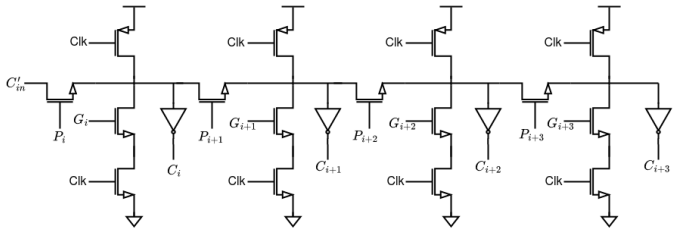

Fig. 6: 4-bit Carry Select Adder

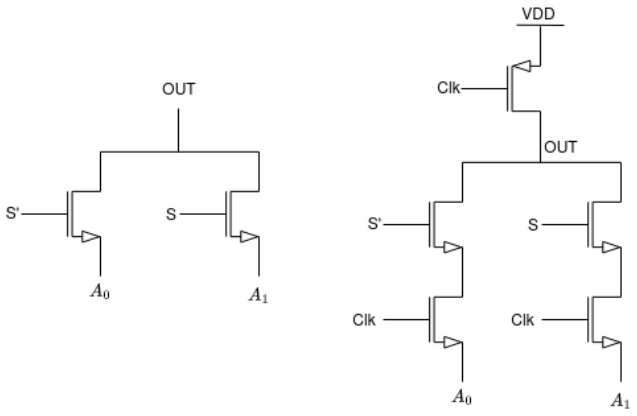

Fig. 7: Multiplexer

III. Flip-Flop implementation

The flip-flop has been designed to be a negative edge triggered flip-flop as shown in Fig 8.

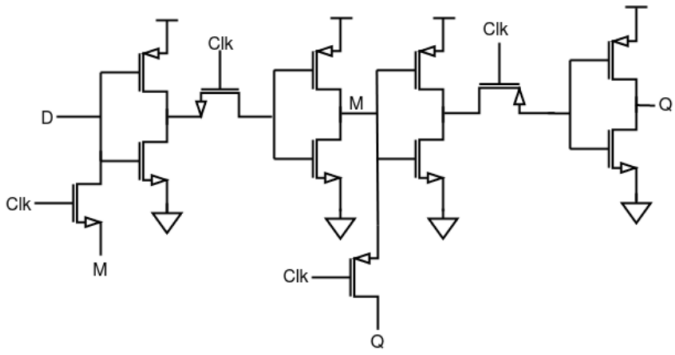

Fig. 8: Negative edge Triggered Flip-flop

IV. First Order Delta Sigma Modulator

Block Diagram of First Order Delta Sigma Modulator is shown in Fig 9.

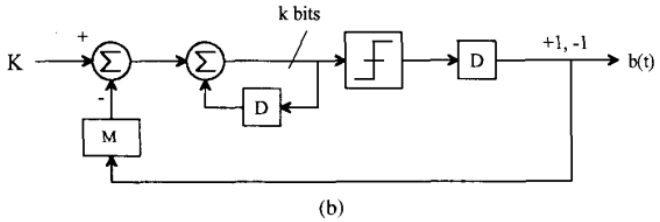

Fig. 9: First Order Delta Sigma Modulator [2]

When the output of the accumulator is negative, it is steered to the positive value by adding a positive number K+M and when the output of the accumulator is positive, it is steered to a negative value by adding a negative number K-M. This poses some restriction on the value of M and K. The output of the topology has been observed to be periodic. Let N, be the total cycles after which the output repeats itself. Let n_1 be the number of cycles for which output is negative and n_2 be the number of cycles for which output is positive. When output is positive, the frequency division of the dual modulus divider is n+1 and when the output is negative, let it be n. Let initial output of the accumulator be 0. From these, two equations emerge.

$$n_1 + n_2 = N \tag{2}$$

$$n_1(K+M) = n_2(M-K) \tag{3}$$

On solving we get,

$$n_1 = \frac{N(M-K)}{2M} \tag{4}$$

$$n_2 = \frac{N(M+K)}{2M} \tag{5}$$

So, the average frequency division will be

$$f_{av} = \frac{n_1(n) + n_2(n+1)}{N} = n + \frac{K+M}{2M} \tag{6}$$

The verilog implementation of first order Delta Sigma Modulator has been given inputs to get a division ratio of n+0.2. On substituting in formula, we get K=-3,M=5. The simulation has been run for 5000 cycles and number of cycles when output is 0 is calculated and plotted(Fig 10).

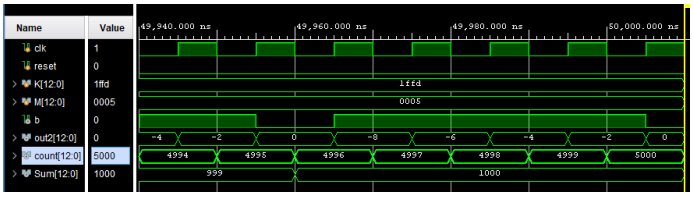

Fig. 10: First Order Delta Sigma Modulator Verilog Output

Number of cycles when output is 0 is 1000. So, the required average has been achieved.

The cadence implementation of this has been run using the 16-bit hybrid adder discussed in section II and the flip-flop in section III to get an average of 0.61. For this M=50,K=11 has been given as inputs. The simulation has been run for 200 cycles and the output has been plotted(Fig 11).

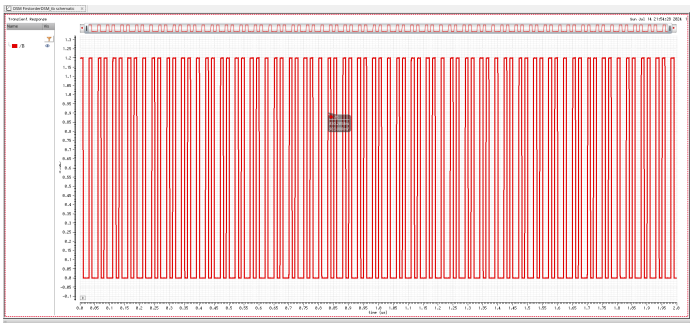

Fig. 11: First Order Delta Sigma Modulator Cadence Output

The average value of the output has been measured in cadence and found to be 479.1m. Normalized with respect to '1' and '0' is .39925 which is approximately 80 cycles, though the desired number of cycles of '1' was 78. The slight discrepancy maybe due to rise and fall time as well as inaccuracy of average measurement by cadence. Based on the average measured by cadence, the frequency division achieved is 0.6. Since the simulation has been run for only 200 cycles, the number of cycles when output is 1 is counted manually and is 78 which is the desired number. The average measured has some errors due to the reasons mentioned above.

Due to the feedback in the first order Delta Sigma Modulator, it has stability issues. In order to reduce this, we use Higher Order Delta Sigma Modulators. These also lead to shifting of quantization noise to higher frequencies which will be better filtered out by the loop filter in the frequency synthesizer.

V. Second Order Delta Sigma Modulator

In the second order Delta Sigma Modulator(Fig 12, we have two accumulators, and their outputs have been added. The final output of the second order Delta Sigma Modulator is the carry output of this adder.

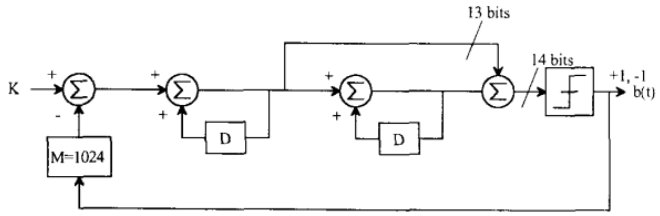

Fig. 12: Second Order Delta Sigma Modulator [2]

Assuming the same formula for the average frequency division achieved as derived in the case of first order Delta Sigma Modulator, the verilog and cadence implementation has been tested for the same average values $\frac{1}{16}$ and 0.61 respectively. The corresponding plots are shown in Fig 13 and Fig 14 respectively.

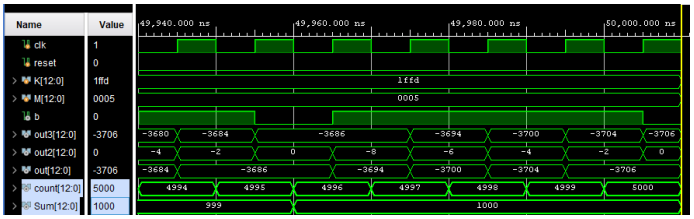

Fig. 13: Second Order Delta Sigma Modulator Verilog Output

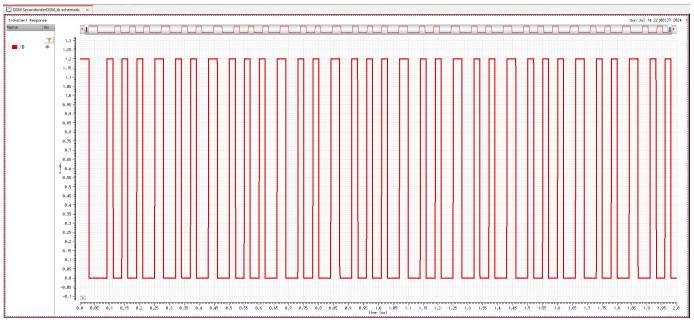

Fig. 14: Second Order Delta Sigma Modulator Second Output

In the verilog implementation, the output is 0 for a total of 1000 cycles and the required average is achieved. In the cadence implementation, the average value of the output is found to be 472.5m which on normalizing is .39375. The output is 1 for a total of around 79 cycles. So, average frequency division achieved is .605.

Increasing the order does reduces the stability issues, but does not remove it. To get performance similar to higher order Delta Sigma Modulators without the stability issues, we use MASH Delta Sigma Modulators.

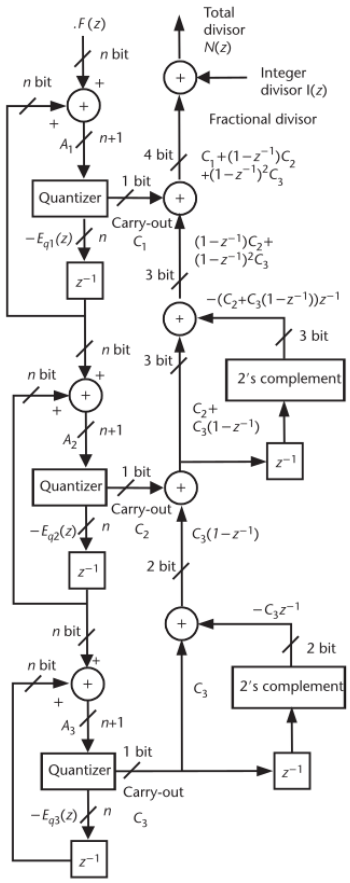

Fig. 15: Mash 1-1-1 Delta Sigma Modulator [1]

VI. Mash 1-1-1 Delta Sigma Modulator

Mash Delta Sigma Modulators work by feeding the quantization noise from one stage to another. Then some computations are done on the carry outputs of the accumulators. Block diagram of Mash 1-1-1 Delta Sigma Modulator is shown in Fig 15. The output of Mash 1-1-1 Delta Sigma Modulator is a 4-bit output in its signed 2's complementary form. For some input K, the average value of output achieved is $K/2^k$ where k is the number of bits of the adder used in the design.

The FPGA implementation of Mash 1-1-1 Delta Sigma Modulator has been simulated using 4-bit accumulator to achieve a average value of $\frac{3}{8}$. For this input K=6 is given. The corresponding plot in Vivado and oscilloscope is shown in Fig 16 and Fig 17 respectively.

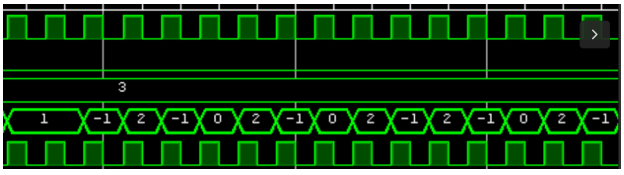

Fig. 16: Mash 1-1-1 Delta Sigma Modulator Verilog Output

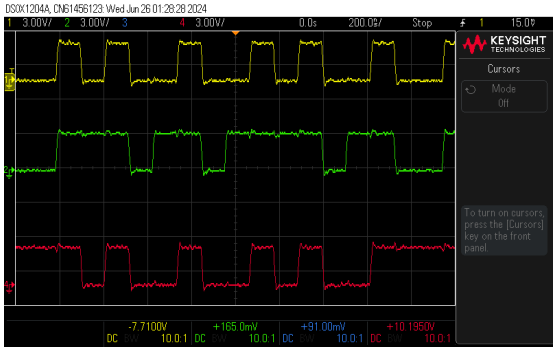

Fig. 17: Mash 1-1-1 Delta Sigma Modulator FPGA Oscilloscope Output

The output is periodic and repeating itself every 16 cycles. The sum of output in each clock cycle across these 16 cycles is 6. So, the required average is achieved.

Using the 16-bit hybrid adder and flip-flop in section II and section III respectively, the cadence design of Mash 1-1-1 Delta Sigma Modulator has been done. The simulation has been done to achieve an average value of 0.5645. For this input K closest to 0.5646 $\times 2^{16}$ is given which is 36992(16'h9080). The 4-bit output has been converted to its signed 2's complementary representation using calculator in cadence. The individual bits and signed decimal form are plotted in Fig 18. The average value of the signed decimal form is calculated in cadence and observed to be 0.5611.

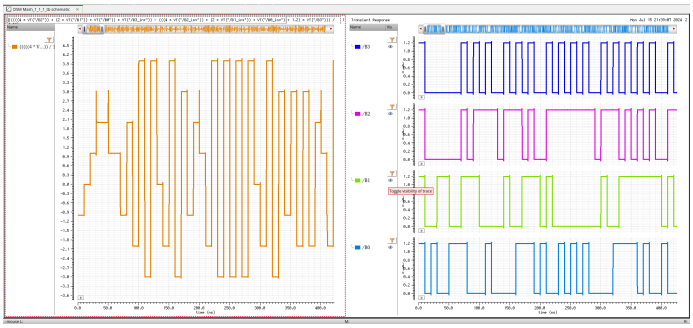

Fig. 18: Mash 1-1-1 Delta Sigma Modulator Cadence Output

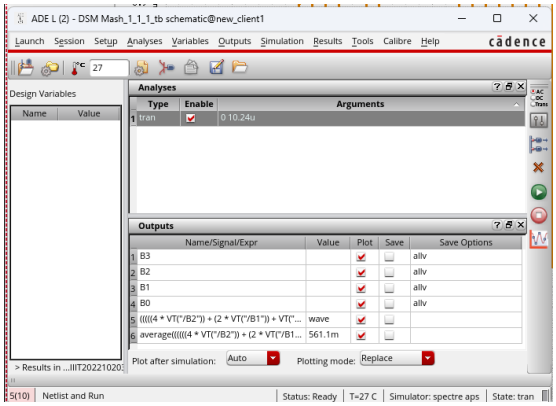

Fig. 19: Mash 1-1-1 Delta Sigma Modulator Cadence Average

Here, the discrepancy could be caused due to reasons mentioned for other topologies but additionally, the design has a settling time of 7 cycles due to delays introduced on the adders other than accumulator as without the delay, there were problems in cascading their outputs.

REFERENCES

[1] Foster Dai, Calvin Plett, and John Rogers. 2006.

[2] Tom Riley, Miles Copeland, and Tad Kwasniewski. "Delta-Sigma Modulation in Fractional-N Frequency Synthesis". In: *Solid-State Circuits, IEEE Journal of* 28 (June 1993), pp. 553–559. DOI: 10.1109/4.229400.