Design and Analysis of ALU

Project Report -VLSI Design(EC6.201)

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1 Introduction

The project deals with design and analysis of ALU which does that can perform a 4-Bit addition,subtraction,comparison and ANDing.The functionality of the logic has been verified using Verilog.The circuit has been designed in Ngspice.Layout has been done in magic.Delay analysis has been done postlayout and critical path as well as maximum delay possible in the circuit has been found.Comparison has been done between prelayout and postlayout results.

2 Verilog

2.1 Design

In Verilog,modules have been made for two to four decoder,enable,fulladder,addersubtractor,comparator and andblock.
The two to four decoder takes in the two select lines and returns 4 outputs only one of which will be logic HIGH depending on the selectlines.

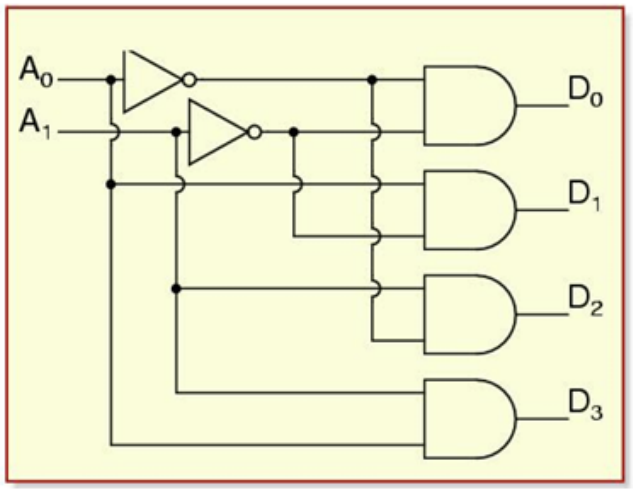


Figure 1: Two to four decoder

These along with the two 4-bit numbers are fed to the enable block which will pass the input through if its Enable input is 1 and otherwise makes all its output bits LOW.

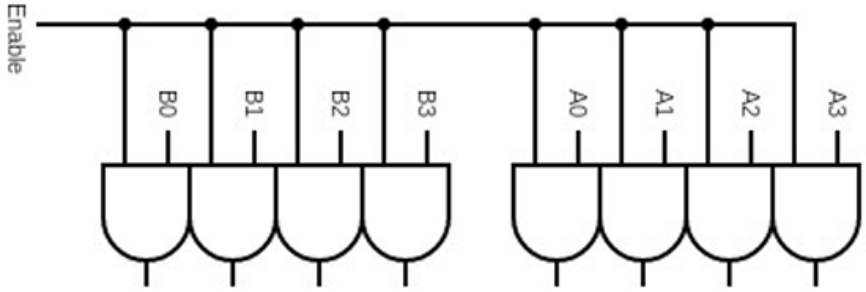


Figure 2: Enable-Block

Three enable blocks have been used which will feed its output to adder-subtractor ,comparator and andblocks.The enable corresponding to adder-subtractor will pass the input when we want to add or subtract(D0+D1=HIGH) and the output of other enables will be 0.Similarly,other cases will happen as well.So,Output of only of the enable block will not be 0(Can be all 0's if input is 0 already) and it will perform the corresponding operation.The output of all other blocks will be 0.

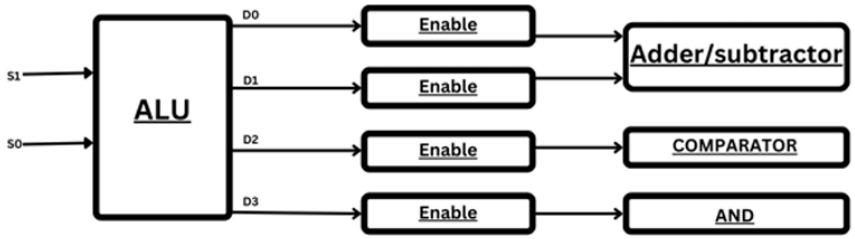


Figure 3: ALU Block Diagram

The operation corresponding to each combination of select lines S1,S0 are as follows:

S1	S0	operation
0	0	Add
0	1	Subtract
1	0	Compare
1	1	And

Figure 4: Select lines

The adder-subtractor has been designed using fulladders in cascade and depending upon the modulating input M which is given as S0,it will perform

addition and subtraction respectively.

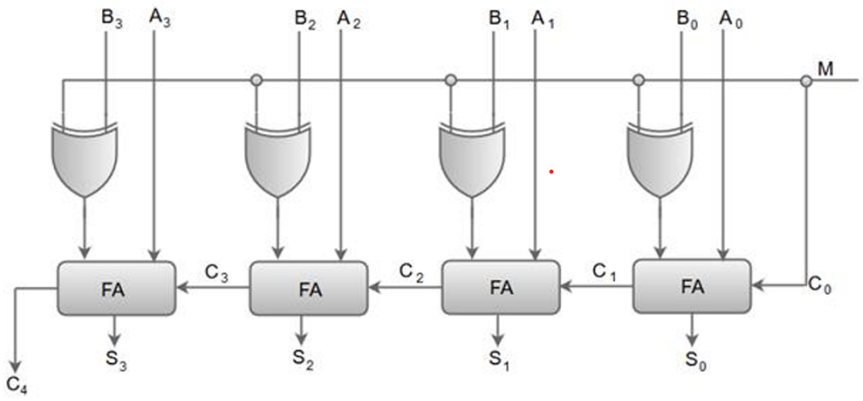


Figure 5: 4 bit adder-subtractor

The comparator returns three output,equal,lesser and greater depending upon whether A=B,A>B or A<B.This has been designed using logical thinking.

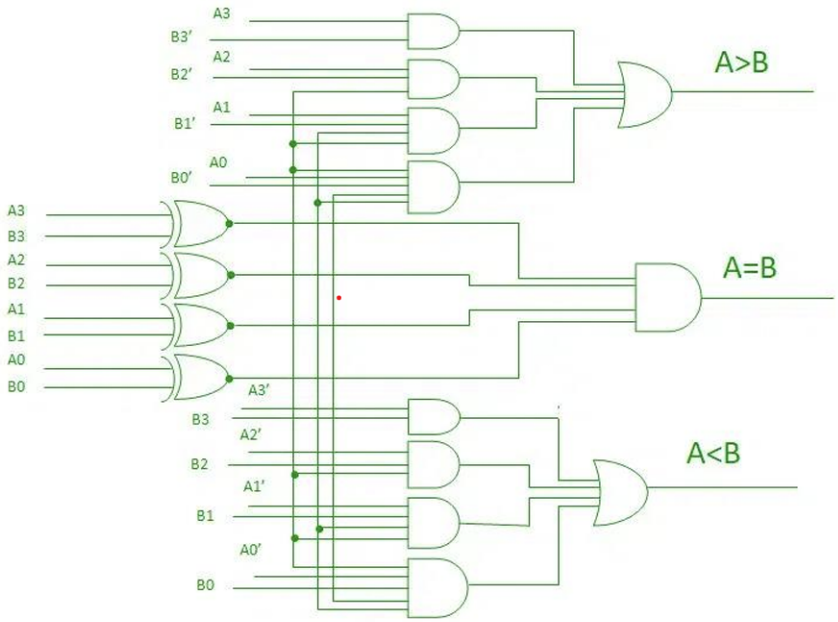


Figure 6: Comparator

The andblock performs and operation between the corresponding bits of the input.

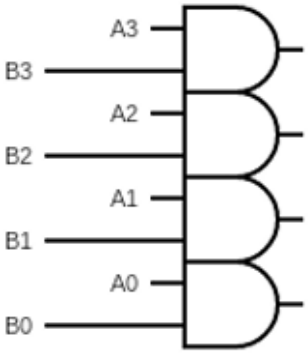


Figure 7: And-Block

At the end,some additional operations are done to make sure,that except the output of the block that we have selected,rest all are 0's.

2.2 Plots

The output in Verilog for a sequence of input has been plotted by by giving one combination of Select lines at a time to check functionality of the circuit.

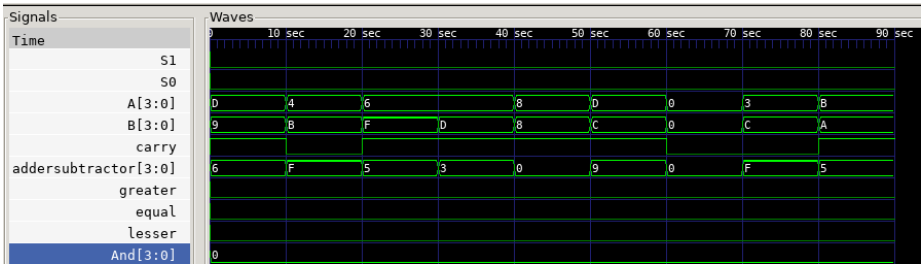


Figure 8: 4-bit Adder:Verilog Output

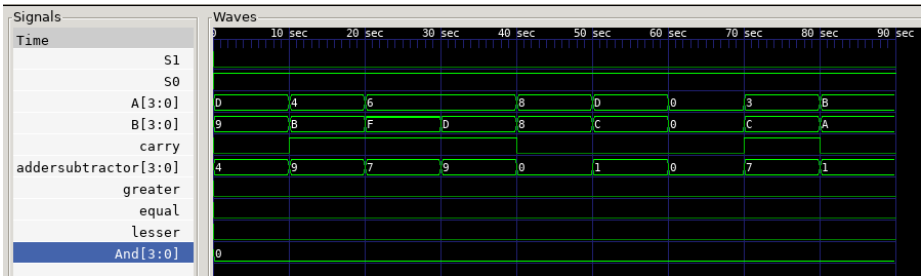


Figure 9: 4-bit Subtractor:Verilog Output

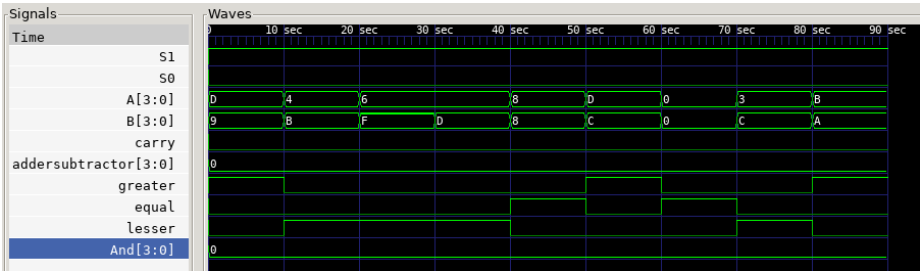


Figure 10: Comparator:Verilog Output

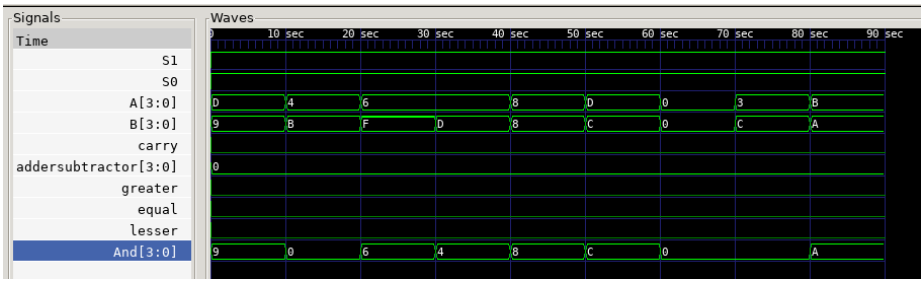


Figure 11: And-Block:Verilog Output

On the basis of the plots,the functionality of the design has been verified.

3 Ngspice

3.1 Design

In Ngspice,the required logic gates that have been used for making the individual blocks have been first made using NMOS and PMOS transistors.Then using these gates,subckt files have been made similar to the modules in Verilog.Rest of the Design is more or less similar to in Verilog.

3.2 Plots

Same input has been given and Select lines have been changed to get the following plots:

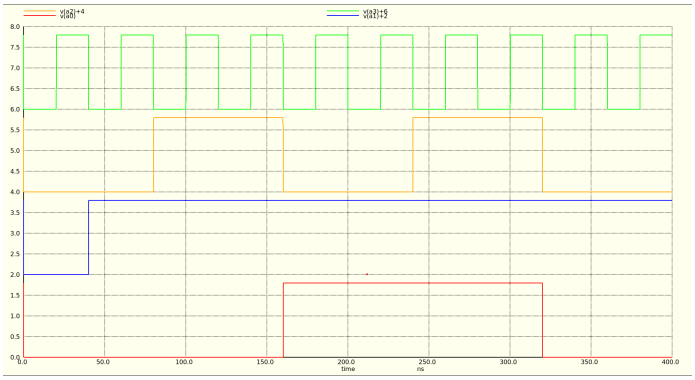


Figure 12: Input A:Ngspice

Figure 13: Input B:Ngspice

Figure 14: 4 bit Adder:Ngspice Output

Figure 15: 4 Bit Subtractor:Ngspice Output

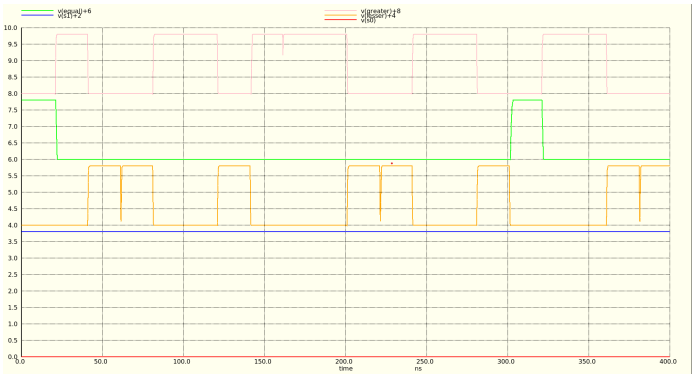


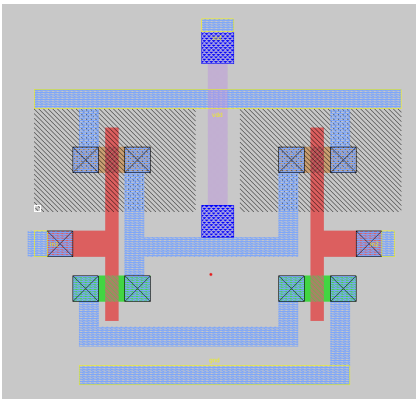
Figure 16: Comparator:Ngspice Output

Figure 17: And-Block:Ngspice Output

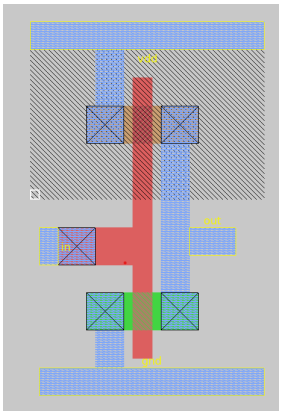
4 Magic

4.1 Design

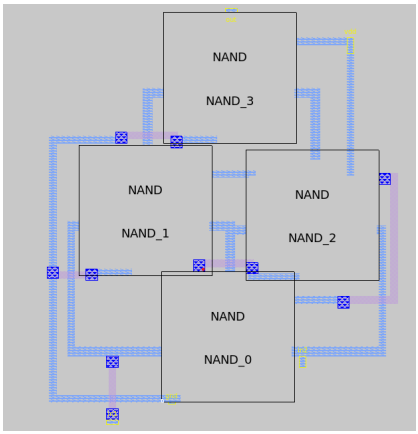
The layout for the same circuit is done in magic.Basic logic gates like NAND,NOR have been made in magic using the different materials.These have then been used to make other logic gates like XOR which can be made using 4 NAND gates.



(a) NAND:Magic



(b) Inverter:Magic



(c) XOR:Magic

Other gates of higher number of inputs have also been made to make the task easier. These have been imported as modules using 'getcell' to make the different blocks -two to four decoder,enable,fulladder,4-Bit adder-subtractor,comparator and and-block as well as other logic gates.These blocks have then been imported and connected accordingly to get the final ALU layout.

4.2 Final Layout

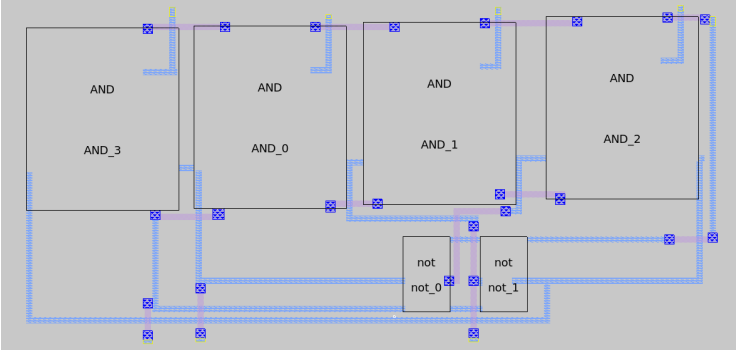


Figure 19: Two to four decoder:Magic

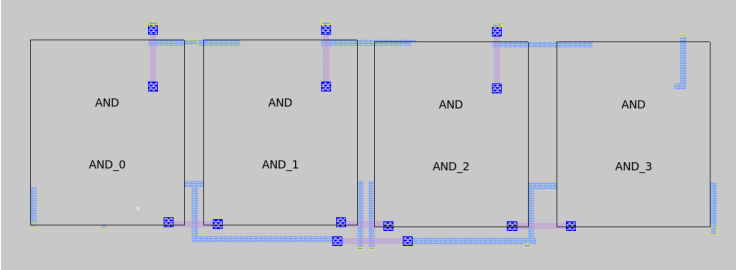


Figure 20: Enable(1-Input):Magic

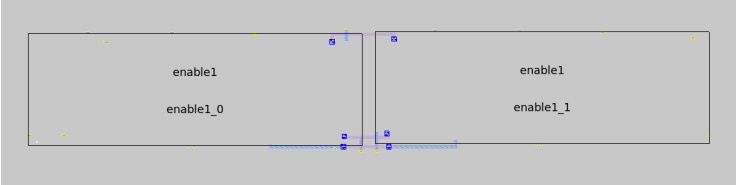


Figure 21: Enable-Block:Magic

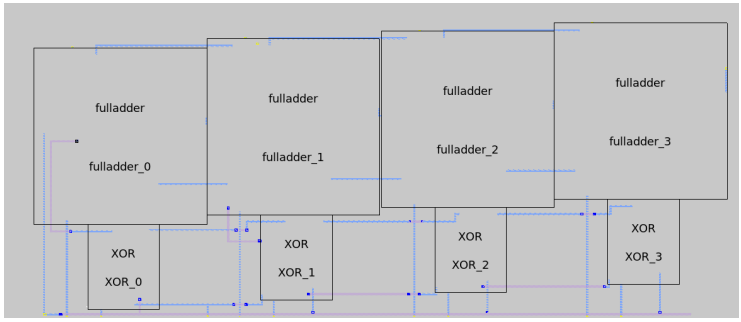


Figure 22: Adder-subtractor:Magic

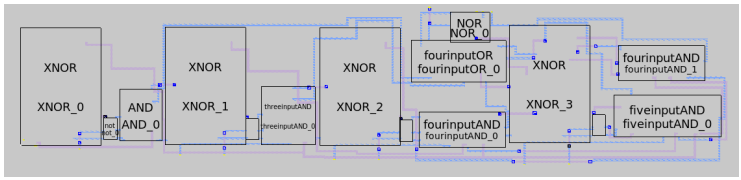


Figure 23: Comparator:Magic

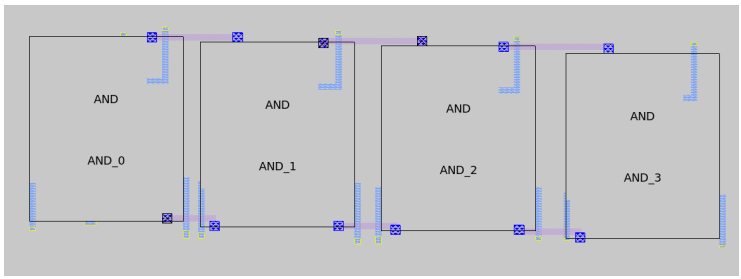


Figure 24: And-Block:Magic

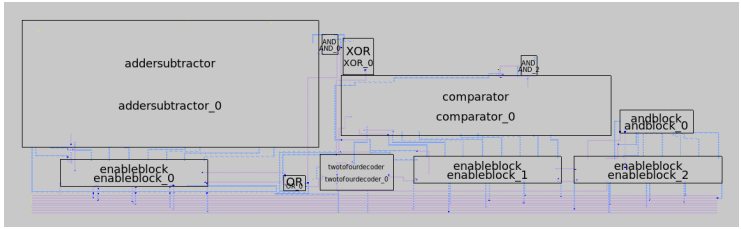


Figure 25: ALU:Magic

Note:"enable1" refers to enable which takes only one set of inputs(A or B).

4.3 Plots

Same input sequence has been given as that of ngspice and Select lines are changes to get the output of different blocks.The following plots are obtained:

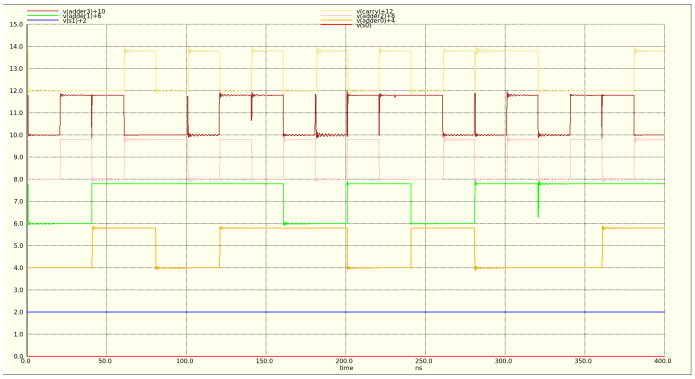


Figure 26: 4 bit Adder:Magic Output

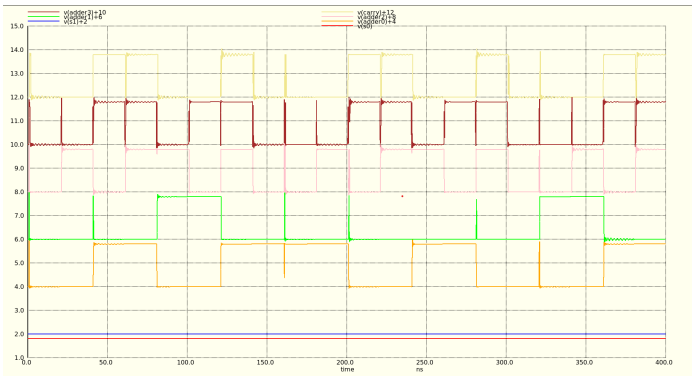


Figure 27: 4 Bit Subtractor:Magic Output

Figure 28: Comparator:Magic Output

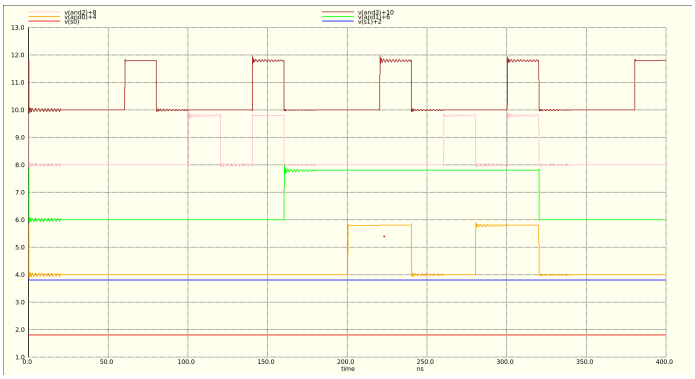


Figure 29: And-Block:Magic Output

5 Delay Analysis

Theory After the input changes,the output does not change instantaneously.There is a delay in between.The design consists of large number of gates and interconnections.The signal will take sometime to propogate through them and cause a change in output.Each of these gates will have its own delay to change its output due to parasitic capacitance due to its structure.There might be an additional delay as output measurement due to load capacitance as well.

The Path along which the circuit has maximum delay is called the Critical patb of that digital Circuit.

5.1 Approach

Time delays are measured using .measure command in ngspice.We can set trigger(trig) of an input such as RISE or FALL and it will measure the time for target(targ) which might be the RISE or FALL of an output. A Python script has been used to calculate the delay of each input corresponding to each output.For this,depending on the block,the input sequence as well as the trigger and target has been set using Python to measure rise time as well as fall time of the output.Delay is the average of the rise and fall time.The delays are then dumped into a text file. Note:Seperate scripts have been made for each of the operations.

5.2 Delay Analysis:Post-layout

From inspection of the text files,the maximum delay corresponding to each output Post-layout: article

Output	Delay
Adder-Carry	7.71609×10^{-10}
Adder-3	6.52962×10^{-10}
Adder-2,	6.70626×10^{-10}
Adder-1	6.61924×10^{-10}
Adder-0	6.65062×10^{-10}
Subtractor-Carry	1.61439×10^{-9}
Subtractor-3	1.31773×10^{-9}
Subtractor-2	1.12388×10^{-9}
Subtractor-1	1.07463×10^{-9}
Subtractor-0	9.86257×10^{-10}
Equal	8.64716×10^{-10}
Greater	6.96348×10^{-10}
Lesser	8.31908×10^{-10}
And-3	2.24720×10^{-10}
And-2	2.0748×10^{-10}
And-1	2.12752×10^{-10}
And-0	2.06822×10^{-10}

Table 1: Delay Analysis

The maximum delay is 1.61439×10^{-9}.This is achieved between B0 and Carry.So,the Critical path is:

B0–>enable–>Subtractor–>**Subtractor-Carry**

5.3 Delay Analysis:Pre-layout

Similar analysis has been done with Pre-layout: article

Output	Delay
Adder-Carry	1.23707×10^{-9}
Adder-3	1.12313×10^{-9}
Adder-2,	1.12314×10^{-9}
Adder-1	1.12313×10^{-9}
Adder-0	1.12315×10^{-9}
Subtractor-Carry	2.60495×10^{-9}
Subtractor-3	2.20723×10^{-9}
Subtractor-2	2.012357×10^{-9}
Subtractor-1	1.81971×10^{-9}
Subtractor-0	1.62853×10^{-9}
Equal	1.68721×10^{-9}
Greater	1.29742×10^{-9}
Lesser	1.27445×10^{-9}
And-3	4.93164×10^{-10}
And-2	4.93164×10^{-10}
And-1	6.68611×10^{-10}
And-0	2.98966×10^{-10}

Table 2: Delay Analysis

The maximum delay is 2.60495×10^{-9}.This is achieved between B0 and Carry.So,the Critical path is:

B0–>enable–>Subtractor–>**Subtractor-Carry**

5.4 Comparison

We observe that the delay measure prelayout is more.This is because the 100f capacitor placed in the output takes time to recharge.Also,the ngspice code is not optimized.While making gates for higher inputs,the 2 input gates were used rather making it using transistors which was done in Magic. The Maximum delay is observed to be between input B0 and Carry in both pre-layout and post-layout.

6 Conclusion

The Circuit designed is functioning correctly.Design has been done in Ngspice and Layout has been extracted and its functionality verified.The maximum delay and Critical path of the Circuit has been found.