(Following Paper ID and Numbers to be filled in your Answer books)

Paper ID: | | | | | | |

Roll No: | | | | | | | | | | |

B.Tech

EXAMINATION, 2015-16

Subject: Switching Theory & Logic Design **Code: NEC304**

[Time: 3 Hours] **[Total Marks: 100]**

SECTION-A

Q.1 Attempt all parts. All parts carry equal marks. Write answer of each part in short. (2 x 10=20)

(a) Find 9's & 10's complement of the following decimal numbers: 24,681,234 & 63,32,5600.
(b) Explain 8421 codes and Self-Complementing codes.
(c) What are signed binary numbers? Explain.
(d) What do you mean by Don't Care conditions in digital circuits?
(e) What is the difference between a De-multiplexer and a Decoder?
(f) What do you mean by Sequential Circuits?
(g) What is the difference between SRAM and DRAM?
(h) What are Gray codes?
(i) What is the difference between Static-0 and Static-1 Hazards?
(j) Convert the following to the other canonical form: F(x,y,z) = $\sum m(2,4,6,7)$

SECTION-B

Note: Attempt any 5 questions from this section. (10 x 5=50)

Q.2 Simplify the following logic function using Quine McClusky minimization technique and realize the simplified expression using universal gate

$$F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$$

Q.3 What is the difference between Ring and Johnson Counters? Explain with example.

Q.4

Derive the state table and state diagram for the sequential circuit shown below:

Q.5 An asynchronous circuit is described by excitation function: $Y = x_1x_2' + (x_1 + x_2')\, y$

and output function: z=y

i. Derive the transition table and output map;
ii. Implement the circuit with a NOR latch.

Q.6 Design a 3-bit Odd Parity Generator. Also design a 2-bit Magnitude Comparator.

Q.7 Design a Decimal Adder using binary parallel adders.

Q.8 What is the difference between Synchronous and Asynchronous counters? Design a MOD-16 Asynchronous UP/DOWN counter.

Q.9 Implement the following three Boolean functions with a PLA and PAL:

$F_1(A,B,C) = ? (0,1,2,4)$

$F_2(A,B,C) = ? (0,5,6,7)$

F3(A,B,C) = ? (0,3,5,7)

SECTION-C

Note: Attempt any 2 questions from this section. (15 x 2=30)

Q.10 (i) Draw the logic diagram of the following product of sum expression:

Y = (x1+x2')(x2+x3)

Show that there is a static -0 hazard when x1 and x3 are equal to 0 and x2 goes from 0 to 1. Find a way to remove the hazard.

(ii)Explain Races in asynchronous sequential circuits. What is the difference between Critical and Non-Critical Races?

Q.11 (i) Implement Full Adder using two 4x1 MUX.

(ii) Tabulate the truth table for an 8x4 ROM that implements the following four Boolean functions:

A(x,y,z) = ?m(1,2,4,6)

B(x,y,z) = ?m(0,1,6,7)

C(x,y,z) = ?m(2,6)

D(x,y,z) = ?m(1,2,3,5,7)

Q.12 (i) Explain Universal Shift Register in detail.

(ii) Convert D Flip-Flop into JK Flip-Flop.