

Experiment No. :- 1

Objective :- Verification and interpretation of truth table for AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates.

Components :- IC 7408 (AND gate), 7432 (OR gate), 7404 (not gate), 7400 (NAND gate), 7402 (NOR gate), 7486 (XOR gate).

Apparatus :- Prototyping board (breadboard), DC power supply, Connecting wires.

Theory :-

Logic gates :- logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship b/w the input and the output is based on a certain logic.

There are total seven logic gates.

AND gate, OR gate, NOT gate, NAND gate, NOR gate, XOR gate, XNOR gate.

AND gate, OR and NOT gates are basic gates. NAND and NOR gates are universal gates. XOR and XNOR are special gates.

Basically logic gates are electronic circuits because they are made up of no. of electronic devices and components. Inputs & outputs of logic gates can occur only in two levels. These two levels are term HIGH and LOW

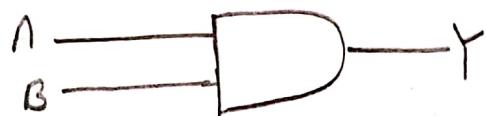
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or TRUE and FALSE, or ON AND off, or Simply

Logic diagram:-

Truth table

Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



AND gate

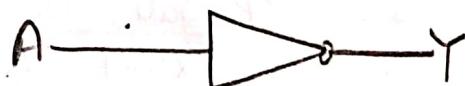
OR gate :-

Inputs		Output
A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1



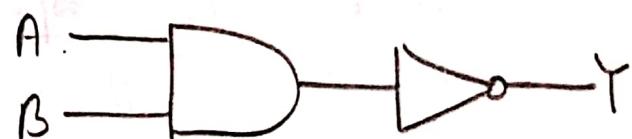
NOT gate

Input	Output
0	1
1	0



NAND gate

Input		Output
A	B	\overline{AB}
0	0	1
0	1	1
1	0	1
1	1	0



or TRUE and FALSE, or ON AND off, or simply 1 and 0. A table which lists all possible combinations of input variables and the corresponding output is called a truth table. It shows how the logic circuit's output responds to various combinations of logic levels at the inputs.

 AND gate:- It gives an output of 1 if both the two inputs are 1, it gives 0 otherwise.

OR gate:- It gives an output of 1 if either of the two inputs are 1, it gives 0 otherwise.

NOT gate:- It gives an output 1 if the input is 0 and vice-versa.

NAND gate:- It gives an output of 0 if both inputs are 1, it gives 1 otherwise.

NOR gate:- It gives an output of 1 if both inputs are 0, it gives 0 otherwise.

 XOR gate:- It gives an output of 1 if either both inputs are different, it gives 0 if they are same.

XNOR gate:- It gives an output of 1 both inputs are same and 0 if both are different.

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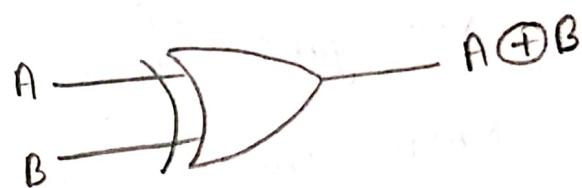
NOR gate

Input		Output
A	B	$\bar{A} + \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0



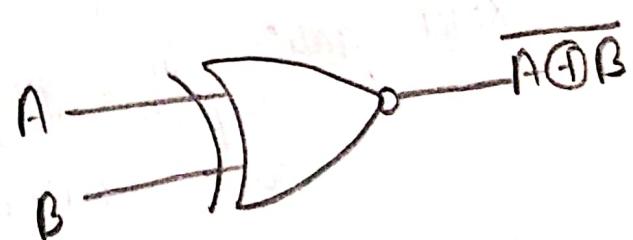
XOR gate

Input		Output
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



XNOR gate

Input		Output
A	B	$\bar{A} \oplus \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	1



Experiment - 2

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Objectives:- To design and verify Half adder and full adder using gates.

Apparatus Required:-

IC 7404, IC 7408, IC 7486, and IC 7432, patch cards and IC trainer kit.

Theory :-

Half-Adder:- It is a combinational logic circuit that performs the addition of two data bits, A and B.

Addition will result in two output bits, one of which is the sum bit S, and the other is the carry bit C.

Full Adder:- The half adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in-bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in-bit, C_{in} is called a full adder.

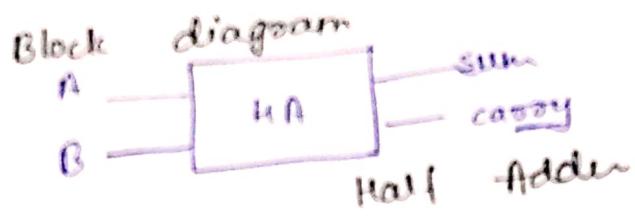
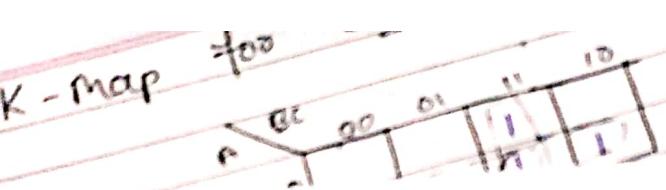
Logical Expression for Sum:-

$$= A'B'C_{in}' + A'B'C_{in} + AB'C_{in}' + AB'C_{in}$$

$$= C \cdot \text{IN}(A'B' + AB) + C \cdot \text{IN}'(A'B + AB')$$

$$= C \cdot \text{IN} \oplus R(A \oplus B)$$

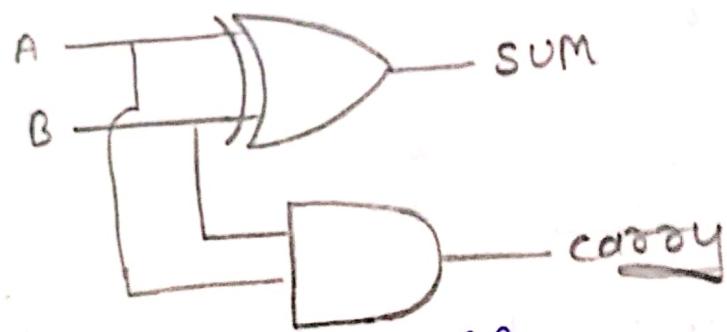
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Truth Table:-

n	B	Sum	<u>Carry</u>
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

logic diagram

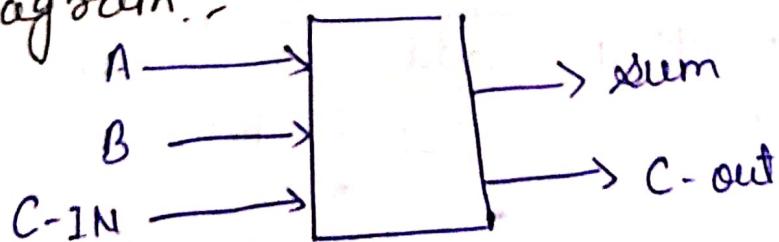


$$\text{sum} = A \oplus B$$

$$\underline{\text{carry}} = AB$$

Full Adder:-

Block diagram:-



K-map for Carry :-

A \ BC	00	01	11	10
0			1	
1	1	1	1	1

$$\text{Carry} = AB + BC + AC$$

Procedure:-

- i) Connections are given as per circuit diagram
- ii) Logical inputs are given as per circuit diagram.
- iii) Observe the output and verify the truth table.

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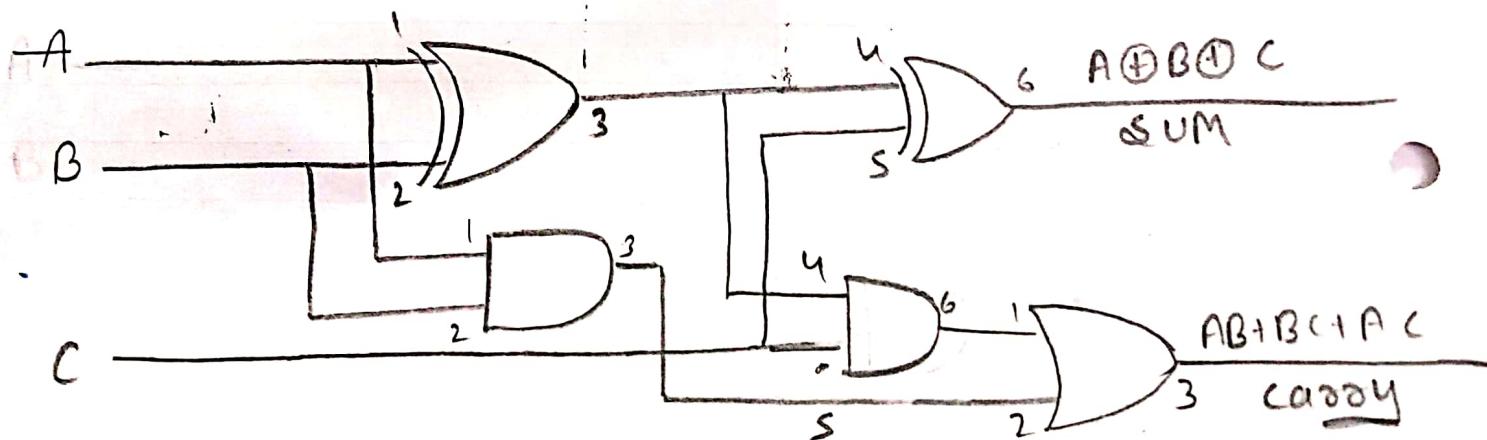
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Truth Table

Inputs			Output	
A	B	C-IN	Sum	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean expression



EXPERIMENT - 63

Objectives:- Design and implementation of Multiplexer and Demultiplexers.

Equipments & Components Required:-

IC 7404, IC 7408, IC 7486, and IC 7432, path cards and IC Trainer kit.

Theory :-

Multiplexer :- It is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines.

Since there are 'n' selection lines, there will be 2^n possible combination of zeroes and ones.

So, one each combination will select only one data input. Multiplexer is also called as MUX.

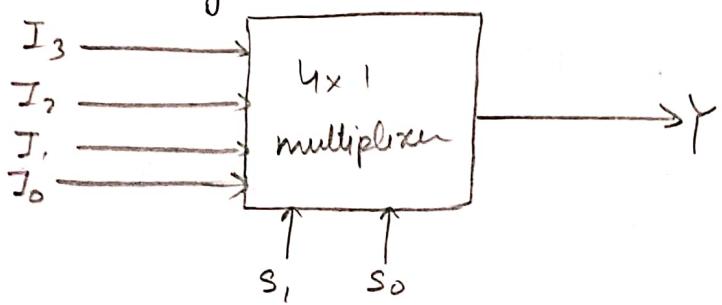
Multiplexers are classified into four types:-

- a) 2-1 multiplexer (1 selected lines)
- b) 4-1 multiplexer (2 selected lines)
- c) 8-1 multiplexer (3 selected lines)
- d) 16-1 multiplexer (4 selected lines)

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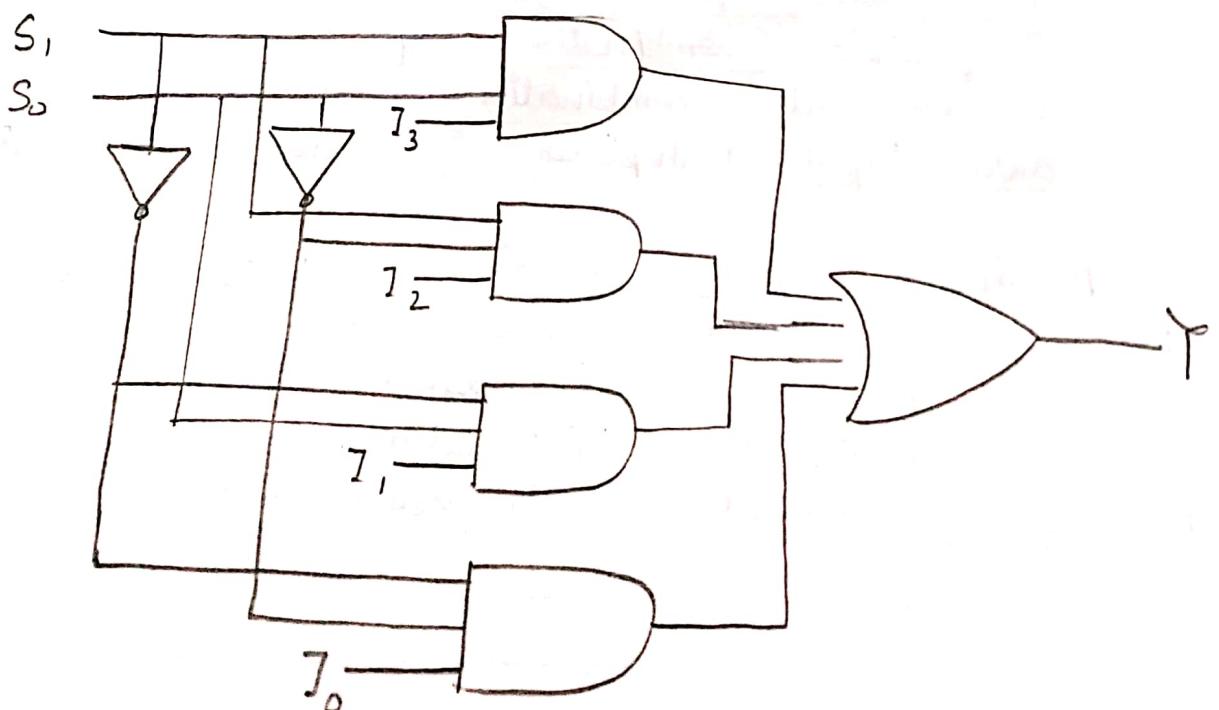
Block diagram of 4x1 Multiplexer



Truth table

Selection lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Circuit diagram



1) 4×1 Multiplexer

4×1 multiplexer has four data inputs I_3, I_2, I_1 , & I_0 , two selection lines S_1 & S_0 and one output Y . The block diagram of 4×1 multiplexer is shown in fig.

One of those 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. Truth table of 4×1 multiplexer is shown in table.

From the truth table, we can directly write the Boolean function for output Y as

$$Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$$

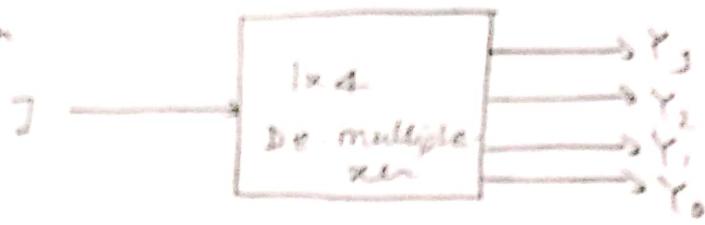
De-Multiplexer:- It is a combinational circuit that performs the reverse operation of input will be connected multiplexer. It has single input ' n ' selection lines and max. of 2^n outputs. The input will be connected to one of these output based on the values of selection lines.

Since there are ' n ' selection lines, there will be 2^n possible combination of zeroes and ones. So, each combination can select only one output. De-multiplexer is also called as De-Mux.

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input 1, two selection
Y₃, Y₂ & Y₁

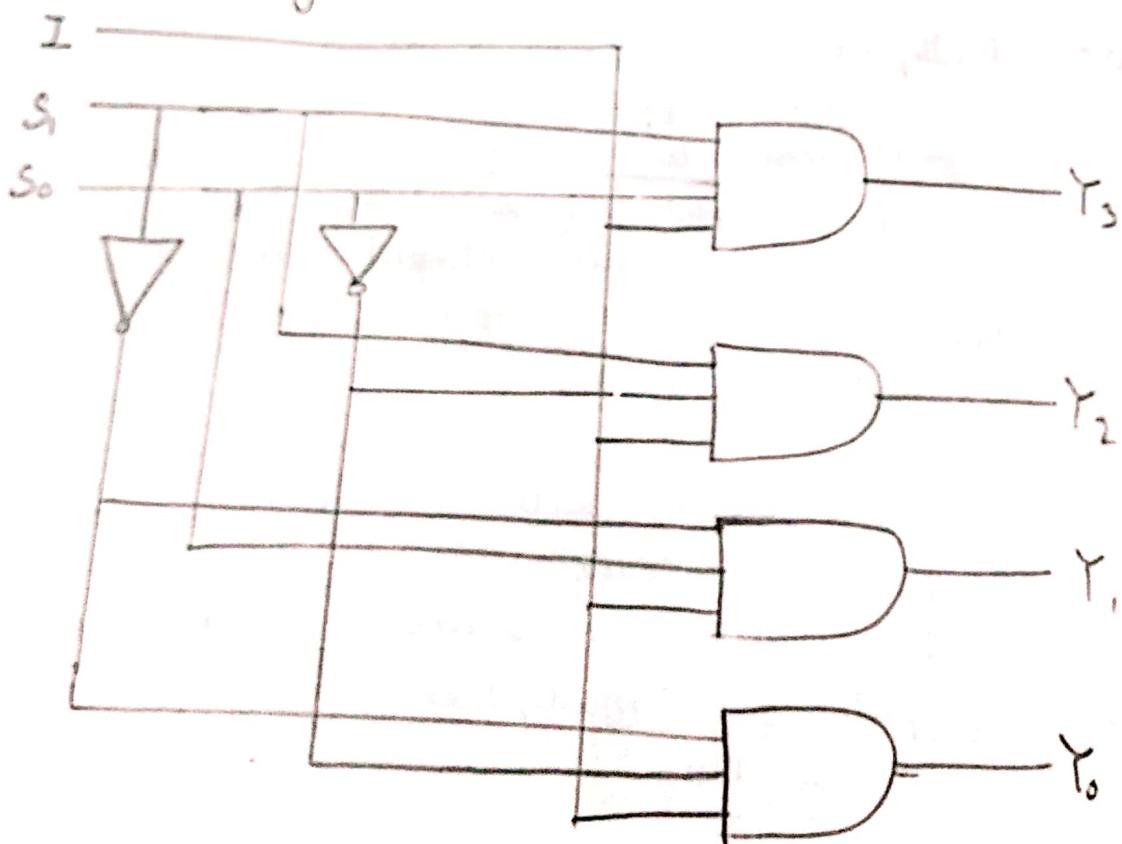
1x4 Demultiplexer Block Diagram



Truth table

Selection Inputs		Outputs			
S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Circuit Diagram



1x4 De-Multiplexer

1x4 De-multiplexer has one input I, two selection lines, S_1 & S_0 and four outputs Y_3 , Y_2 , Y_1 & Y_0 .

The single Input 'I' will be connected to one of the four outputs Y_3 to Y_0 based on the values of selection lines S_1 & S_0 . The truth table of 1x4 is shown in fig.

From the truth table, we can directly write the Boolean function for each output as

$$\text{from the } Y_3 = S_1 S_0 \quad Y_2 = S_1 \bar{S}_0 \\ Y_1 = \bar{S}_1 S_0 \quad Y_0 = \bar{S}_1 \bar{S}_0$$

Procedure :-

- 1 Check for the proper working of the gate.
- 2 Connect the circuit as per circuit diagram
- 3 Verify it with the truth table

Result 1:- Study of 4x1 multiplexer and verified the truth table

Result :- Study of 1x4 demux and verified the truth table.

Precaution :-

- 1 All the connection should be tight
- 2 Always connect the ground first and then connect Vcc.
- 3 All IC's should checked before starting the experiment.
- 4 The kit should be off before change the connection

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EXPERIMENT - 04

Objective:- Implementation and verification of decoder using logic gates.

Apparatus:- Digital trainer kit, IC 7408 (AND gate), 7404 (NOT gate) and connecting wires., and

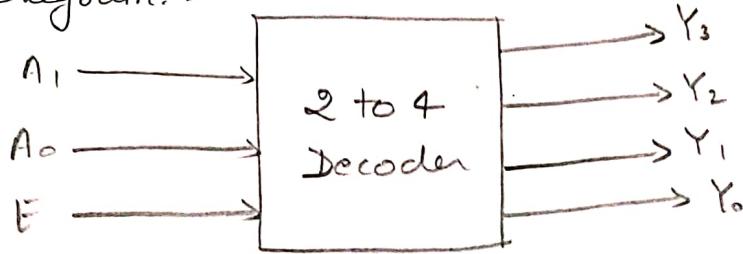
Decoder:- The combinational circuit that changes the binary information into 2^n output lines is known as Decoders. The binary information is passed in the form of N input lines. The output lines define the 2^n bit code for the binary information. In simple words, the Decoder performs the reverse operation of the Encoder. At a time, only one input line is activated for simplicity. The produced 2^n bit output code is equivalent to the binary information.

2 to 4 line decoder:-

In the 2 to 4 line decoder, there is a total of three inputs, i.e. A_0 and A_1 and E and four outputs i.e., Y_0 , Y_1 , Y_2 , and Y_3 . For each combination of inputs, when the enable 'E' is set to 1, one of these four outputs will be 1. The block diagram and the truth table of the 2 to 4 line decoder are given below.

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Block Diagram:-



and

Truth Table:-

Enable	Inputs		Outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	1
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

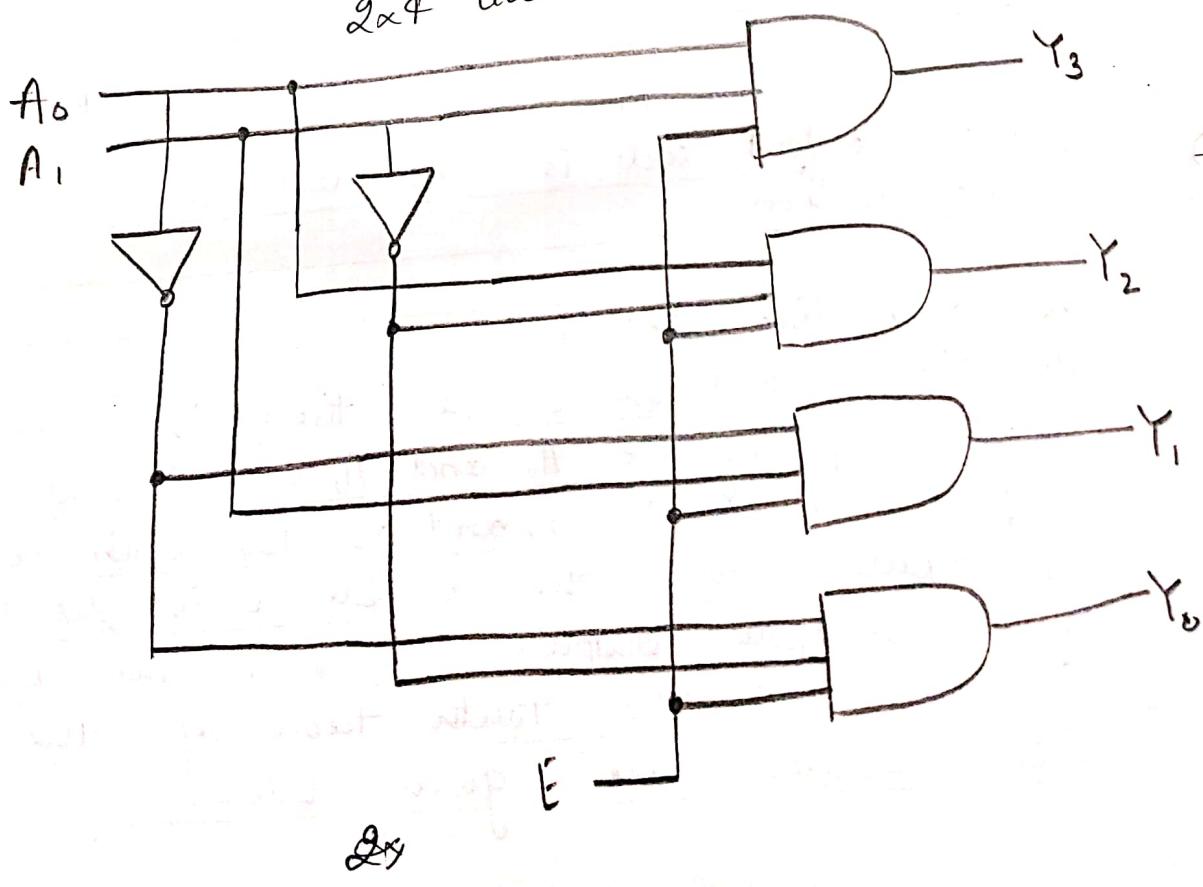
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2x4 line decoder



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The logical expression of the term Y_0, Y_1, Y_2 , and Y_3 is as follows:-

$$Y_3 = E \cdot A_1 \cdot A_0$$

$$Y_1 = E \cdot A_1 \cdot A_0$$

$$Y_2 = E \cdot A_1 \cdot A_0$$

$$Y_0 = E \cdot A_1 \cdot A_0$$

Result:- Truth tables of Decoder is verified

Precautions:-

All connection should be made neat and tight.

while making connections main voltage should be kept switched off.

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EXPERIMENT- 05

Objectives:- Implementation and verification of Encoder, using logic gates.

Apparatus:- Digital trainer kit, 7432 and connective gates.

Encoders:-

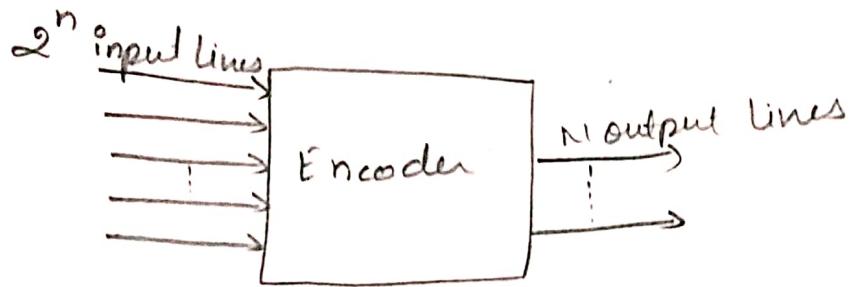
The combinational circuits that change the binary information into N output lines are known as Encoders. The binary information is passed in the form of 2^n input lines. The output lines define the N -bit code for the binary information. In simple words, the Encoder performs the reverse operation of the Decoder. At a time only one input line is activated for simplicity. The produced N -bit output code is equivalent to the binary information.

4 to 2 line Encoder:-

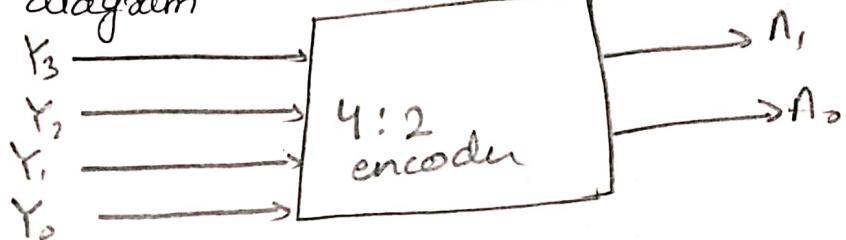
In 4 to 2 line encoder, there are total of four inputs, i.e. $\gamma_0, \gamma_1, \gamma_2$ and γ_3 and two outputs, i.e. A_0 and A_1 . In 4-input lines, one input line is set to true at a time to get the respective binary code in the output side. Below are the block diagram & the truth table.

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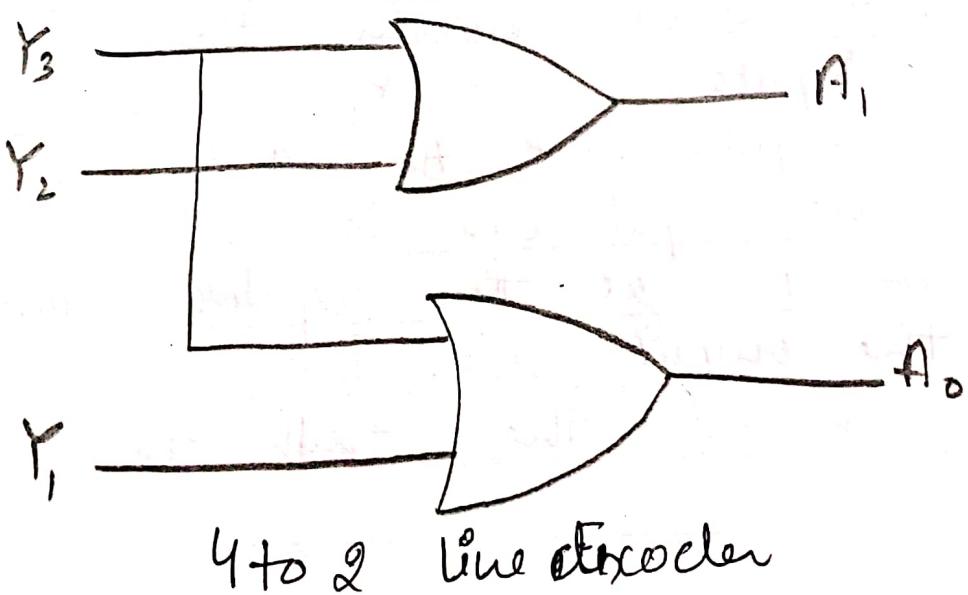


Block diagram



Truth table

Inputs				Outputs	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1



The logical expression of the term A_0 and A_1 is as follows -

$$A_1 = Y_3 + Y_2$$

$$A_0 = Y_3 + Y_1$$

Result:- Truth table of Encoder is verified.

Precautions:-

- 1) All connections should be made neat & tight
- 2) While making connections main voltage should be kept switched off.

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