ust What are the classifications of sequential circuits?

ans Sequential circuits are of two types:-

(a) Asynchronous sequential circuits:- It is also known as clocked circuit. It works in the absence of clock signal. In asynchronous circuits the state of the device can change at any time in response to changing inputs.

(b) Synchronous sequential circuits:- It is also known as a. ___ . It ~~works~~ triggered in the presence of clock signal. In synchronous sequential circuits, the state of the device changes only at discrete times in response to a clock signal.

doubt

us-2- What is the operation of D flip-flop?

Ans The D flip-flop is the most important flip-flop from other clocked types. It ensures that at the same time, both the inputs, i.e. S & R, are never equal to 1.

It has a single input "D" used in place of the "Set" input and for compulsory "Reset" input the inverter is used.

thus, $S = D$ and $R = \sim D$ (complement of D

Qus-3 what is flip-flop?

Ans A flip-flop is a device which stores a single bit of data. It maintains a state until directed by input to change the state. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.

Qus-4 Define Race around Condition:

Ans When the S and R inputs of an SR flip-flop is at logical 1 and then the input is changed to any other condition, then the output becomes unpredictable this is called the race around condition.

Ans A race around condition is the condition of an electronics, software or other system where the system's substantive behavior is dependent on the sequence or timing of other controllable events. It becomes a bug when one or more of the possible behaviours is undesirable.

Qus-5 Flip-Flop	Latch
1. Flip-Flop utilizes an edge triggering approach.	Latch follows a level triggering approach.
2. The clock signal is present.	The clock signal is absent.

3. It is sensitive to the applied input and the clock signal	3. Latches are sensitive to the applied input singl only when enabled.
4. It has slow operating speed.	4. It has fast operating speed.
5. Flip-flop performs synchronous operations. i.e it works on clock signals.	5. latches perform asynchronous operations. i.e it doesn't work based on the time signal.
6. It requires more power	It requires comparatively low power.

Q-6 Define Propagation Delay.

Ans Propagation delay is the time duration taken for a signal to reach its destination, it is caused by the time it takes for a signal to travel through a medium.

$$\text{Propogation delay} = \frac{d}{s}$$

where d = distance
s = wave propogation speed.

In ~~wireless~~ wireless communication,
$s = c$ i.e the speed of light.

Que-7:- What is master slave flip-flop..

Ans A type of clocked flip flop consisting of clocked master and slave elements that are clocked on complementary transitions of the clock signal.

Here the master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion. i.e. if the master is positive edge-triggered, then the slave is negative edge triggered & vice-versa.

Qus:- Explain the shift registers:-

Ans Shift register is a group of flip-flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.
They share a single clock signal, which causes the data stored in the system to shift from one location to the nent.

Ques 9:- What are the applications of flip-flops?

1) Data Transfer:- It is the process of transferring the data from one register to another register.

2) Counters:- Counters are the digital circuits which are used to count the number of events. These are nothing but a series of flip-flop arranged in a definite manner.

GOOD WRITE

the mapping (a+b)+

3. Event-Detectors:- Event deetectors are the circuits which aid in determining the occurence of a particular event. Flip-flops are well-known to preserve their state until the apperance of a suitable condition at their inputs, which means they can act as event-detectors.

4. D-flip-flop can be used to create delay-lines which are used in digital signal processing systems.

5. The variation in the output voltage can be avoided by connecting a RS flip-flop b/w the switch and the digital circuit to act as a switch debouncer.

Qu-10: What is state diagram?

Ans: A state diagram is used to represent the condian of the system or part of the system at finite instances of time. It's behavioral diagram and it represents the behaviour using finite state transition.

(11) Write the truth table of clocked T-flip flop?

→

T	Qn	Qn+1	
0	0	0	Unchanged/hold
0	1	1	Unchanged/hold
1	0	1	Toggle
1	1	0	Toggle

(12) How many types of Registers are there?

→ (1) serial - In / serial - out
   (2) serial - 0 In / Parallel - out
   (3) Parallel - in / serial - out
   (4) Parallel - in / Parallel - out

(13) Define different types of latches?

A latch is a special type of logical circuit. The latches have low and high two stable states. Due to these states, latches also refer to as bistable - multivibratoss. A latch is a storage device that holds the data using the feedback lane. The latch stores 1 - bit until the device set to I

(14) Write the differences b/w synchronous and assynchronous counters?

Synchronous

Asynchronous

(1) In synchronous, all flip flops are triggered with same clock simultaneously.

(1) In asynchronous, all flip flops are triggered with diff. clock not simultaneously.

(2) In synchronous counter, propagation delay is less

(2) In asynchronous counter, there is high propagation delay

(3) Synchronous counter is faster than asynchronous counter in operation.

(3) Asynchronous counter is slower than synchronous counter operation.

(4) Synchronous counter is also called parallel counter.

(4) Asynchronous counter is also called serial counter.

(5) Synchronous counter will operate in any desired count sequence

(5) Asynchronous counter will operate only in fixed count sequence (OD I DOWN)

(6) Synchronous counter dcefquino

(6) Ex:- Ring counter, Johnson counter

(6) Ex:- Ripple up counter, Ripple DOWN counter

(15) Define flip-flop and various types of flip-flop?

Ans:- Flip-Flop is a circuit that maintains a state until directed by input to change the state. A basic Flip-flop can be constructed using four-NAND or four NOR-gates.

* Types of flip flop are:-

(1) RS flip Flop:- The R-S flip-flop is used to temporarily hold or store information until it is needed. A single R's flip flop will store one binary digits, either a 1 or a 0.

(2) JK flip flop :- The J-K flip-flop is basically a gated SR flip-flop with the addition of a clock input circuitly that prevents the illeged or invalid output condition that can occur when both inputs s and R are equal to logic level '1'

(16) explain the logic diagram of JK flip-flop?

→ The output of the JK flip-flop does not modify if both 'J' and 'R' are '0'. If both the inputs are '1' then the output dial to its free.
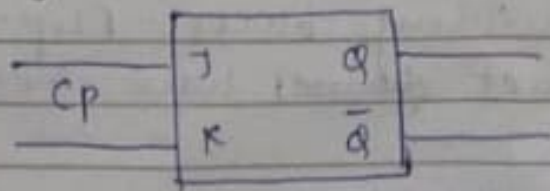
(17) Write difference between combinational & sequential circuits?

* combinational circuit:-

→ In this output depends only upon present input.
→ Speed is fast
→ It is designed easy.
→ This is time independent
→ It is easy to use and handle.
→ There is no feedback between input and output.
→ Elementary building blocks: logic gate
→ There circuit do not have any memory element.

Ex:- Encoder, decoder etc.

* Sequential circuit:-

→ In this output depend upon present as well as past input.
→ Speed is low.
→ It is not easy to use and handle.
→ This is time dependent
→ It is designed tough.
→ There exists a feedback path between input and output
→ Element building blocks:- Flip-flop
→ These circuit do not have memory element

Ex:- Flip-flop, counters

logic = 1

$Q_{n+1} = Q_n$

Negative - edge triggered

CLK

Q_A

Q_B

Q_C
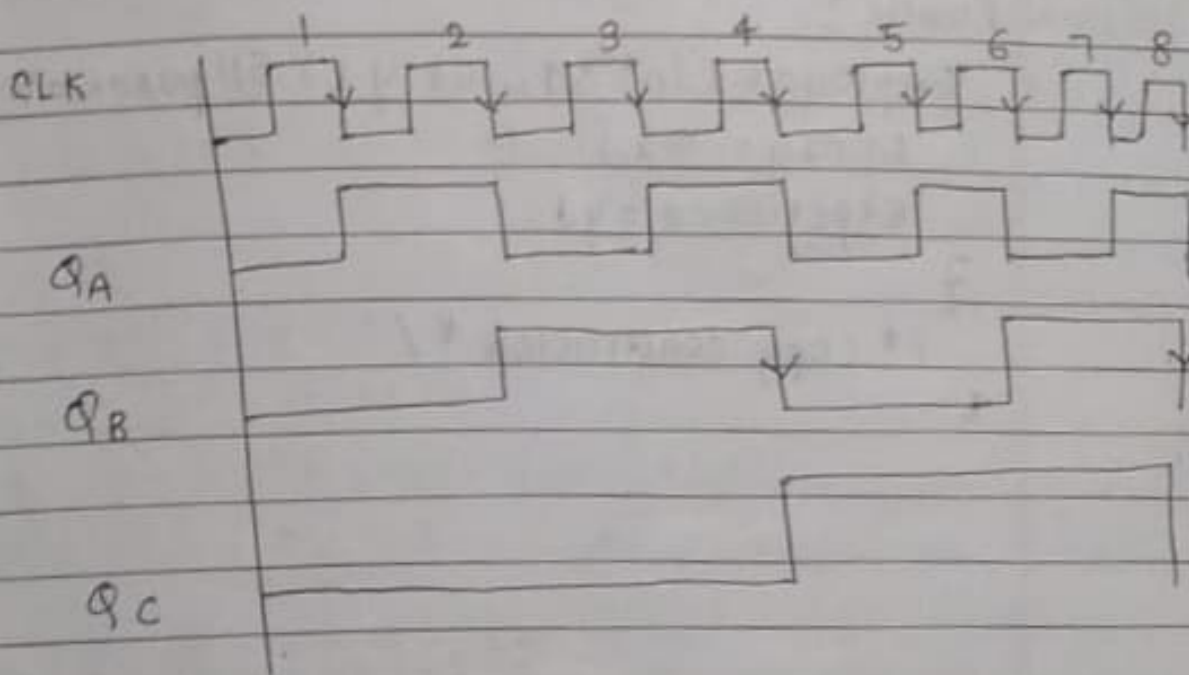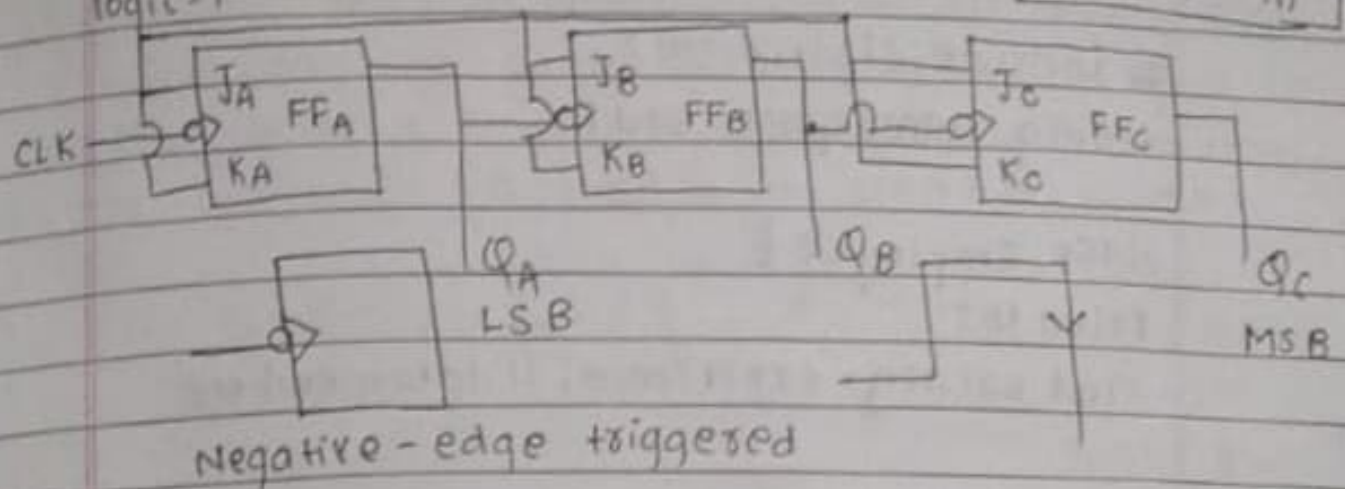
TRUTH - TABLE

CLK		Q_C	Q_B	Q_A	DECIMAL VALUE
↓	1	0	0	0	~~VALUE~~ 0
	2	0	0	1	1
	3	0	1	0	2
	4	0	1	1	3
	5	1	0	0	4
	6	1	0	1	5
	7	1	1	0	6
	8	1	1	1	7

(11) Explain the logic diagram of SR flip flop?

→ In the SR flip flop circuit, from each output to one of the other NAND gate inputs, feedback is connected. So, the device has two inputs, i.e, set 'S' and reset 'R' with two outputs Q and Q'

set Pin ——[S   Q]—— output

Reset Pin ——[R   Q']—— inverted output
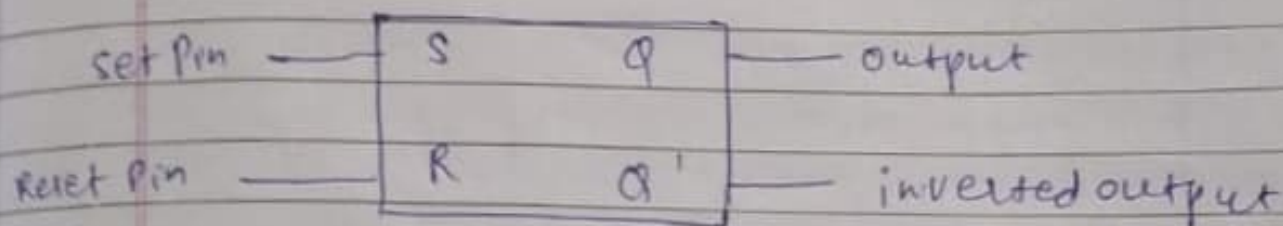
Draw and explain the operation of d flip-flop?

→ The D-flip-flop is a clocked flip-flop with a single digital input 'D'. Each time. D flip-flop is clocked, its output follows the state of 'D'. The D flip-flop has only two inputs D and CP.

D ——[D   Q]—— Q
       flip-Flop
CLK ——[Q̄]—— Q̄