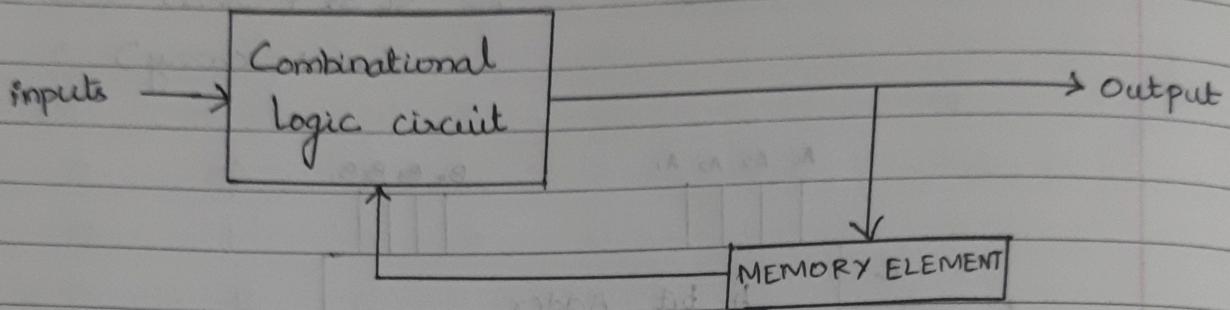


I

A sequential circuit is a logic circuit, where the output depends on the present value of the input signal as well as the sequence of past inputs.

A sequential circuit is a combination of circuits with a storage element (Memory).



Types of Sequential Circuits

The sequential circuits are classified into two types:

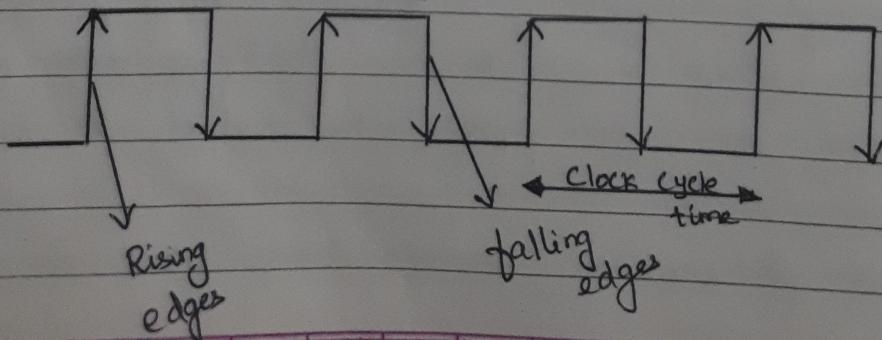
- i) Synchronous circuit
- ii) Asynchronous circuit

Sequential circuit

This type of system uses storage elements called flip-flop that are employed to change their binary value only at discrete instants of time.

Sequential circuits have a clock signal as one of their inputs.

All state transition in such circuit occurs only when the clock value is either 0 or 1 or happen at the rising or falling edges of the clock depending on the type of memory element used in the circuit.



A Clock Signal is a periodic square wave that indefinitely switches from 0 and 1 and from 1 to 0 at fixed intervals.

$$\text{Clock Frequency} = \frac{1}{\text{Clock cycle time}}$$

$$F = 1/T$$

Frequency is inversely proportional to time. So, if the time decreases, the frequency increases which in turn increases the performance of the circuit.

II LATCHES AND FLIPFLOPS

Latches and flipflop are the basic elements and these are used to store information.

Flip flop and latch can store one bit of data.

Difference between Latches and Flip Flop

LATCHES	FLIP FLOP
1. Latches are building blocks of sequential circuits and built from logic gate	Flip flop are building blocks of sequential circuits and built from latches
2. Latch continuously checks its inputs and changes its output correspondingly	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
3. Latches are sensitive to the duration of the pulse and can send or receive the data when the switch is ON	Flip flop is sensitive to a signal change. They can transfer data only at a single instant and data cannot be changed until next signal change. Ex: REGISTER

4. It is based on the enable function input. It works on the basis of clock pulses

5. It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.

It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

LATCHES

A Latch is a circuit element that alters the output based on the current input, previous input and previous output. There are 4 different types of latches.

1. SR Latch

2. D Latch

3. J-K Latch

4. T Latch

SR LATCH

It is one of the simplest electronic circuits built with two NOR gates or two NAND gates.

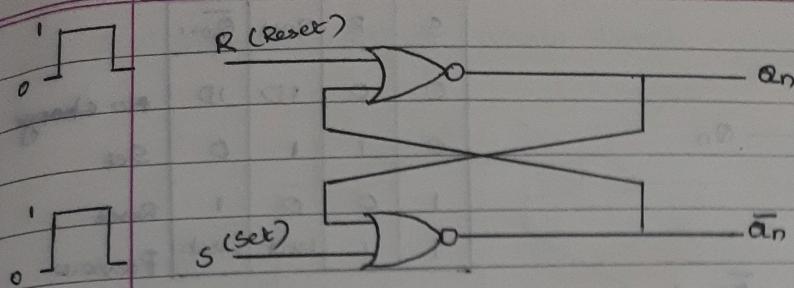
WITH NOR GATE

SR Latch have two inputs S and R. S is called Set and R is called Reset.

The S input is used to produce High on \bar{Q}_n and the R input is used to produce Low on \bar{Q}_n .

The output of SR Latch depends on current as well as previous inputs or state.

The State can change as soon as the input changes. The circuit and truth table of SR Latch is shown below:



S	R	Q_{n+1}	\bar{Q}_{n+1}	
0	0	Latch	Latch	Previous
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	undefined

The operation has to be analyzed with the 4 inputs combinations together with the 2 possible previous states. Q_n is the present state and Q_{n+1} is the next state (May be final output).

case (i) when $S=0 \quad R=0$

$$Q_{n+1} = R + \bar{Q}_n = 0 + \bar{Q}_n = Q_n \text{ (Latch / Previous State)}$$

$$\bar{Q}_{n+1} = S + Q_n = 0 + Q_n = \bar{Q}_n \text{ (Latch / Previous State)}$$

If both S and R input are Low, the output is retained as previous state. (no change state)

(ii) Case (ii) when $S=0 \quad R=1$

$$Q_{n+1} = R + \bar{Q}_n = 1 + \bar{Q}_n = Q_n \text{ (} \because \text{ it anything is 1)}$$

$$\bar{Q}_{n+1} = S + Q_n = 0 + Q_n = 1 \text{ complement}$$

If $S=0$ and $R=1$, the output Q_{n+1} is Low and it is called Reset Condition.

Case (iii) when $S=1 \quad R=0$

$$Q_{n+1} = R + \bar{Q}_n = 0 + \bar{Q}_n = Q_n = (S_0, Q_{n+1}) = 1 \text{ i.e.}$$

$$\bar{Q}_{n+1} = S + Q_n = 1 + Q_n = 0 \text{ complement (} 1 + \text{ anything is 1)}$$

If $S=1$ and R, the output Q_{n+1} is HIGH and it is called Set Condition.

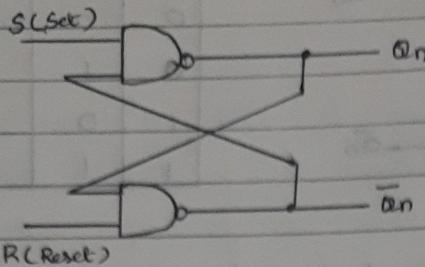
Case (iv) when $S=1 \quad R=1$

$$Q_{n+1} = R + \bar{Q}_n = 1 + \bar{Q}_n = 0 \} \text{ Indetermined Condition,}$$

$$\bar{Q}_{n+1} = S + Q_n = 1 + Q_n = 0 \} \text{ Since Complement and}$$

Regular output are same.

WITH NAND GATE



S	R	Q_{n+1}	\bar{Q}_{n+1}	
0	0	1	0	No change
0	1	1	0	Set
1	0	0	1	Reset
1	1	latch	latch	Previous

Case (i) $S=0 \quad R=0 \quad (1D)$

$$Q_{n+1} = S \cdot \bar{Q}_n = 0 \cdot \bar{Q}_n = 0 \quad \text{indetermined condition}$$

$$\bar{Q}_{n+1} = R \cdot Q_n = 0 \cdot Q_n = 0 \quad \text{Since Regular Output and complement Output are same}$$

Case (ii) $S=0 \quad R=1$

$$Q_{n+1} = S \cdot \bar{Q}_n = 0 \cdot \bar{Q}_n = 0 \quad \text{using } S=0$$

$$\bar{Q}_{n+1} = R \cdot Q_n = 1 \cdot Q_n = Q_n = 0 \quad (\text{since } Q_n=1 \text{ is complement})$$

Case (iii) $S=1 \quad R=0$

$$Q_{n+1} = S \cdot \bar{Q}_n = 1 \cdot \bar{Q}_n = \bar{Q}_n = Q_n = 0 \quad \text{using } R=0$$

$$\bar{Q}_{n+1} = R \cdot Q_n = 0 \cdot Q_n = 0 \quad \text{Complement}$$

Case (iv) $S=1 \quad R=1$

$$Q_{n+1} = S \cdot \bar{Q}_n = 1 \cdot \bar{Q}_n = \bar{Q}_n = Q_n \quad \text{Previous State / Latch}$$

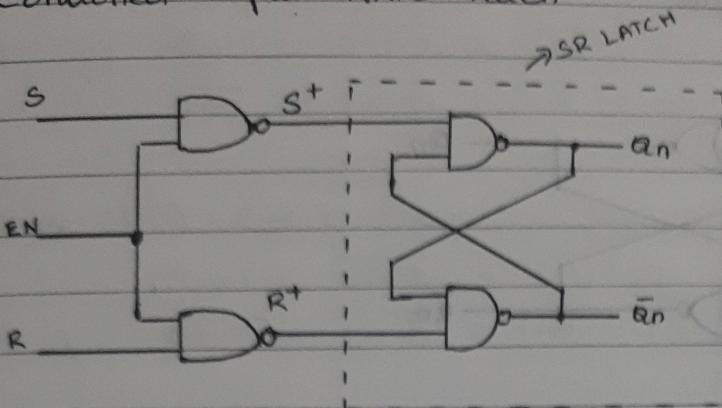
$$Q_{n+1} = R \cdot Q_n = 1 \cdot Q_n = \bar{Q}_n \quad \text{Memory}$$

The NAND gate latch requires complement of NOR gate latch. Hence it is sometimes referred as S'R' latch.

CONTROLLED INPUT LATCH

The operation of the basic SR Latch can be modified by providing an additional input signal that controls when the state of the latch can be changed by determining whether S and R can affect the circuit.

Controlled input NAND Latch



EN	S	R	Qn(t)
0	0	0	Previous state
1	0	0	Previous state
1	0	1	Reset
1	1	0	Set
1	1	1	Indetermined

Case(i) when $S=0$ $R=0$ $EN=0$

$$\begin{aligned} S^+ &= \overline{S \cdot EN} = \overline{0 \cdot 0} = 1 \\ R^+ &= \overline{R \cdot EN} = \overline{0 \cdot 0} = 1 \end{aligned} \quad \left. \begin{array}{l} \text{Previous State / Latch} \\ \text{No Change} \end{array} \right\}$$

The input (1,1) for SR Latch with NAND gate maintains the previous / memory / Latch condition / No change.

Case(ii) when $S=0$ $R=0$ $EN=1$

$$\begin{aligned} S^+ &= \overline{S \cdot EN} = \overline{0 \cdot 1} = 1 \\ R^+ &= \overline{R \cdot EN} = \overline{0 \cdot 1} = 1 \end{aligned} \quad \left. \begin{array}{l} \text{No Change State / Latch} \\ \text{Previous State} \end{array} \right\}$$

Case (iii) when $S=0$ $R=1$ $EN=1$

$$\begin{aligned} S^+ &= \overline{S \cdot EN} = \overline{0 \cdot 1} = 1 \\ R^+ &= \overline{R \cdot EN} = \overline{1 \cdot 1} = 0 \end{aligned} \quad \left. \begin{array}{l} \text{Reset Condition for SR Latch} \end{array} \right\}$$

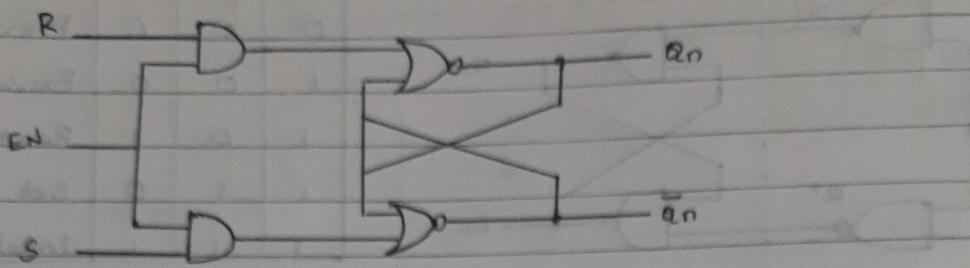
Case (iv) when $S=1$ $R=0$ $EN=1$

$$\begin{aligned} S^+ &= \overline{S \cdot EN} = \overline{1 \cdot 1} = 0 \\ R^+ &= \overline{R \cdot EN} = \overline{0 \cdot 1} = 1 \end{aligned} \quad \left. \begin{array}{l} \text{Set Condition for SR Latch} \end{array} \right\}$$

Case (v) when $S=1$ $R=1$ $EN=1$

$$\begin{aligned} S^+ &= \overline{S \cdot EN} = \overline{1 \cdot 1} = 0 \\ R^+ &= \overline{R \cdot EN} = \overline{1 \cdot 1} = 0 \end{aligned} \quad \left. \begin{array}{l} \text{Indetermined Condition} \end{array} \right\}$$

Controlled input NOR gate



The controlled input for NOR gate can be given by adding 2 AND gate
Case i) $R=0$

D LATCH (Transparent Latch)

The D latch is the simplest extension of SR latch which removes the possibility of

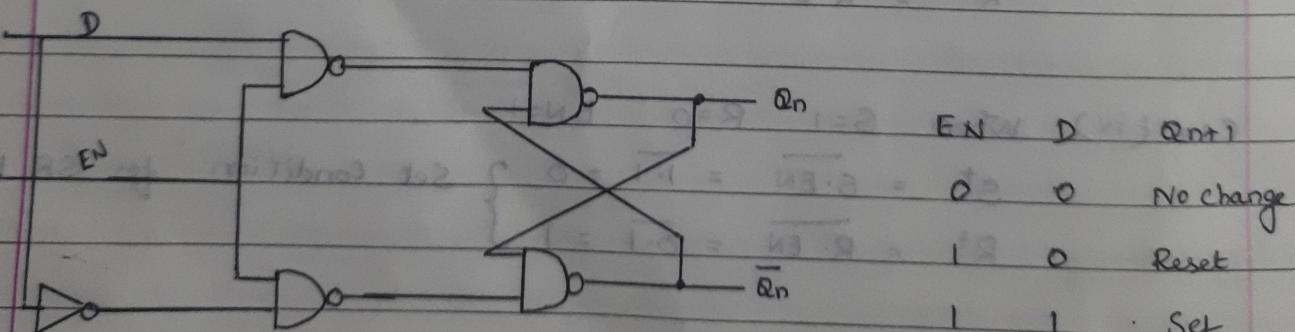
i) Indetermined input state and

ii) Reduce the number of input lines as

S & R are complement inputs. If $S=0, R=1$

it is reset and if $S=1, R=1$, it is set. So

we can reduce the I/P line by introducing an inverter (NOT gate).



Case (i) $EN=0, D=0$

$$Q_{n+1} = \overline{EN \cdot D} = \overline{0 \cdot 0} = 1 \quad \left. \begin{array}{l} \text{Previous State is} \\ \text{SR Latch (No change)} \end{array} \right\}$$

$$\overline{Q_{n+1}} = \overline{EN \cdot \bar{D}} = \overline{0 \cdot \bar{0}} = 1 \quad \left. \begin{array}{l} \text{Previous State is} \\ \text{SR Latch (No change)} \end{array} \right\}$$

Case (ii) $EN=1 \quad D=0$

$$Q_{n+1} = \overline{EN \cdot D} = \overline{1 \cdot 0} = 1 \quad \text{Reset condition}$$

$$\overline{Q_{n+1}} = \overline{EN \cdot \bar{D}} = \overline{1 \cdot 1} = 0$$

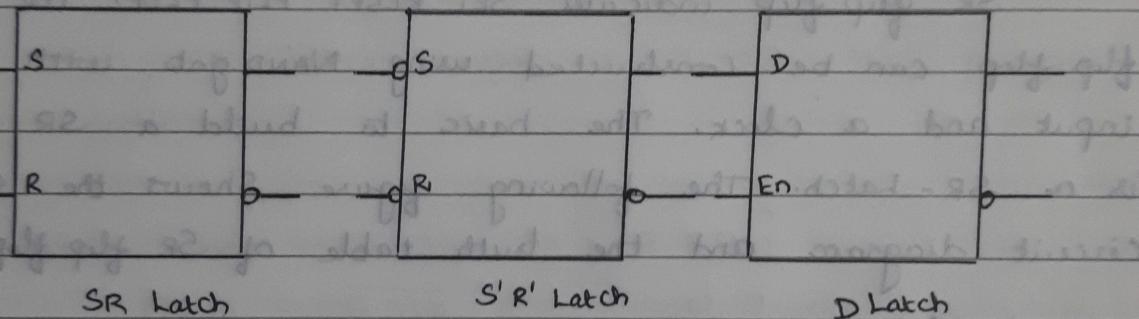
Case (iii) $EN=1 \quad D=1$

$$Q_{n+1} = \overline{EN \cdot D} = \overline{1 \cdot 1} = 0 \quad \text{Reset condition}$$

$$\overline{Q_{n+1}} = \overline{EN \cdot \bar{D}} = \overline{1 \cdot 0} = 1$$

Thus, using D-Latch the indetermined condition is eliminated while using one input line only.

Graphic Symbols for latches



A latch is designated by a rectangular block with inputs on the left and outputs on the right. The output with a bubbled symbol indicates a complement output. S'R' Latch is the latch using NAND gate.

III

FLIP FLOPS

The flip flops are built from latches and it includes an additional clock signal apart from the inputs used in the latches.

It is capable of storing the binary values i.e. 0 or 1.
There are four types of flip flops:

i) SR Flip Flop

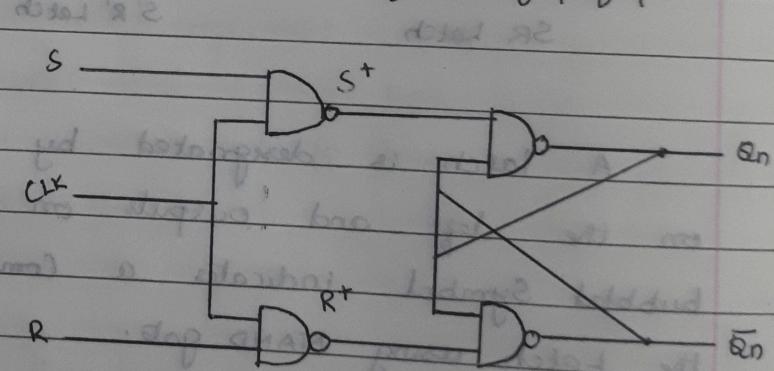
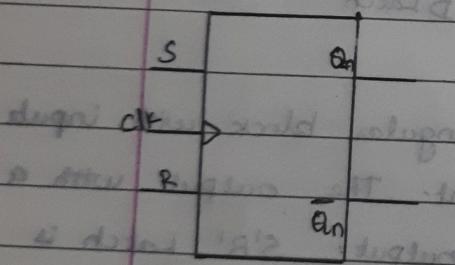
ii) D Flip Flop

iii) JK Flip Flop

iv) T Flip Flop

SR FLIP FLOP

SR flip flop indicates SET RESET FLIP FLOP. The SR flip flop can be constructed using NAND gate with controlled input and a clock. The basic to build a SR flip flop is a SR-Latch. The following figure shows the symbol, circuit diagram and the truth table of SR flip flop.



TRUTH TABLE FOR SR LATCH

S	R	Q_{n+1}	\bar{Q}_{n+1}
0	0	1	0
0	1	Set	0
1	0	0	1
1	1	Latch	Latch

TRUTH TABLE FOR SR FLIPFLOP

CLK	S	R	Q_{n+1}	\bar{Q}_{n+1}
0	0	0	No change	No change
1	0	0	No change	No change
1	0	1	0	1
1	1	0	1	0
1	1	1	1	Indetermined

Case (i) When $CLK=0$ $S=0$ $R=0$

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{0 \cdot 0} = 1 = S^+$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{0 \cdot 0} = 1 = R^+$$

When SR latch input is $(1, 1)$, the output is the
No Change / Previous State

Case (ii) When $CLK=1$ $S=0$ $R=0$

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{0 \cdot 1} = 1 \quad \text{Previous state}$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{0 \cdot 1} = 1$$

Case (iii) When $CLK=1$ $S=0$ $R=1$

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{0 \cdot 1} = 1 \quad \text{Reset}$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{1 \cdot 1} = 0$$

When SR latch input is $(1, 0)$, the output is the

Reset Condition

Case (iv) When $CLK=1$, $S=1$, $R=0$

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{1 \cdot 1} = 0 \quad \text{Set}$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{0 \cdot 1} = 1$$

When SR latch input is $(0, 1)$, the output is the

Set Condition

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{0 \cdot 1} = 1$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{1 \cdot 1} = 0$$

Case (v) When $CLK=1$ $S=1$ $R=1$

$$Q_{n+1} = \overline{S \cdot CLK} = \overline{1 \cdot 1} = 0 \quad \text{Indetermined output}$$

$$\overline{Q}_{n+1} = \overline{R \cdot CLK} = \overline{1 \cdot 1} = 0$$

When SR latch input is $(1, 1)$, the output is indetermined.

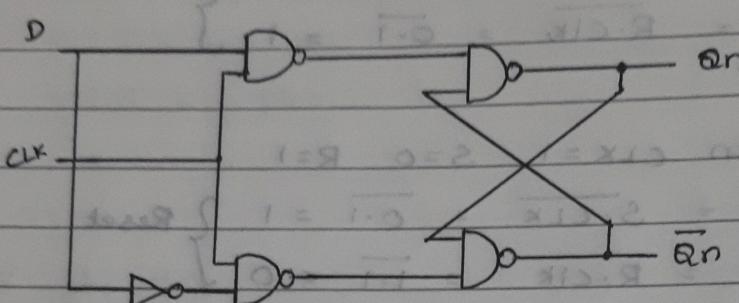
D- FLIP FLOP

D- Flip flop is the Data Flip flop. D- flip flop is designed using SR Flip flop.

In SR Flip flop there are 4 states:

- i) Set
- ii) Reset
- iii) No change
- iv) Indetermined.

If we want only Set and Reset Condition then we can go for D flip flop instead of SR Flip Flop.



TRUTH TABLE

CLK	D	Qn	Qn+1
0	0	X	0
1	1	X	1

In the above truth table, the input signal is D and 1 and the clock is in ON Condition. Qn is the present state and we don't know the value, so it is marked as X. We need to find the next state; i.e., Qn+1.

Case (i) when CLK = 1, D = 1

$$\begin{aligned} \overline{Q_{n+1}} &= \overline{D \cdot \text{CLK}} = \overline{1 \cdot 1} = 0 \\ \overline{Q_{n+1}} &= \overline{\bar{D} \cdot \text{CLK}} = \overline{0 \cdot 1} = 1 \end{aligned} \quad \left. \begin{array}{l} \text{Set condition} \\ \text{Reset condition} \end{array} \right\}$$

Case (ii) when CLK = 1, D = 0

$$\begin{aligned} \overline{Q_{n+1}} &= \overline{D \cdot \text{CLK}} = \overline{0 \cdot 1} = 1 \\ \overline{Q_{n+1}} &= \overline{\bar{D} \cdot \text{CLK}} = \overline{1 \cdot 0} = 0 \end{aligned} \quad \left. \begin{array}{l} \text{Reset condition} \\ \text{Set condition} \end{array} \right\}$$

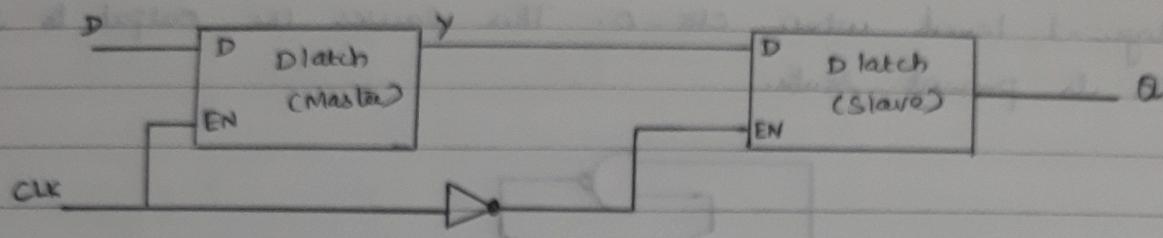
EDGE TRIGGERED D FLIP FLOP

Latches are often called Level-Sensitive because their output follows their input as long as they are enabled. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus we can have all changes synchronized to the rising or falling edge.

of the clock.

An edge-triggered flip-flop achieves this by combining in series a pair of latches.

The construction of a D flip-flop with two D latches and an inverter is shown below.



The first latch is called the Master and the second the Slave.

The circuit samples the D input and changes its output Q only at the negative edge of the synchronizing or controlling clock.

When the clock is 0, the output of the inverter is 1. The Slave latch is enabled and its output Q is equal to the master output Y.

The master latch is disabled because $\text{clk} = 0$. When the input pulse changes to logic -1 level, the data from the external D input are transferred to the master.

The Slave is disabled as long as the clock remains at the level 1, because its enable input is equal to 0.

A change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

The behavior of the master-slave flip-flop dictates that

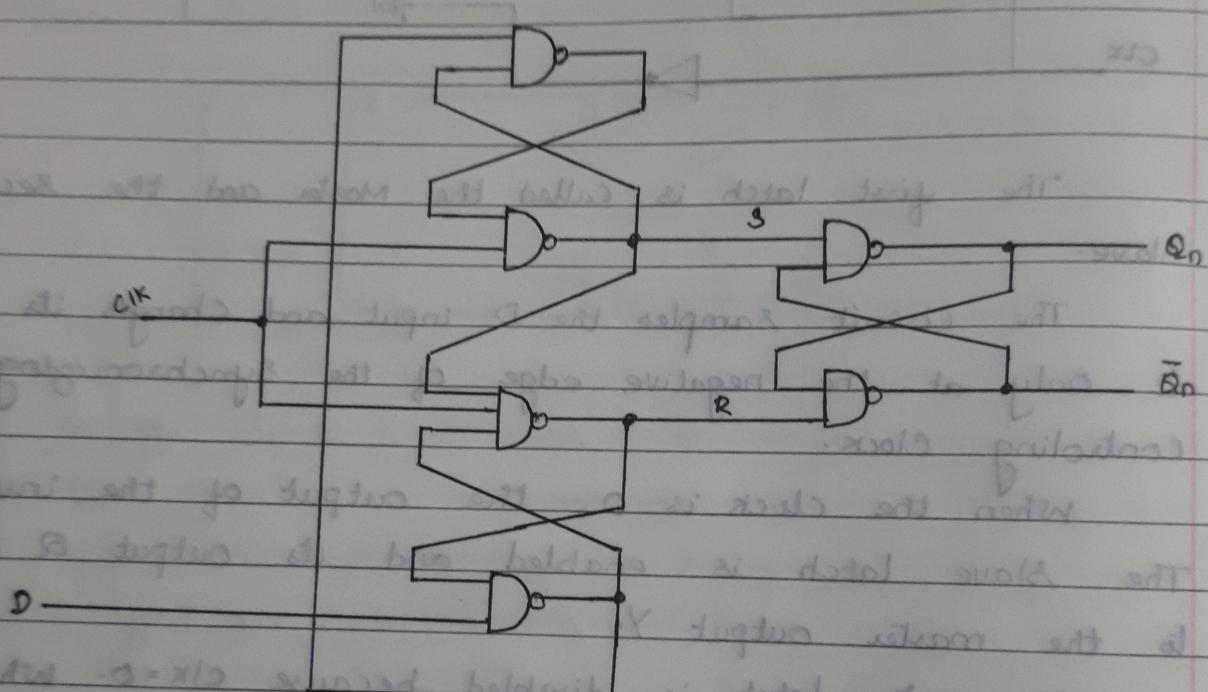
- the output may change only one
- a change in the output is triggered by the negative edge of the clock
- the change may occur only during the clock's negative level.

EDGE-TRIGGERED D Flip-flop using 3 SR latches

The two latches respond to the external D (data) and CLK (clock) inputs.

The third latch provides the output for the flip-flop.

The SR inputs of the output latch are maintained at the logic-1 level when $CLK = 0$. This causes the output to remain in its present state.



D-type positive-edge-triggered flip-flop using 3 SR latches

Input D may be equal to 0 or 1. If $D=0$ when clock becomes 1, R changes to 0. This cause the flip-flop to go to the reset state.