Cycle	Instruction Retired	Reason
1 - 2	RST	These initial cycles indicate the assertion of a reset signal (no instructions execute).
5 - 6	NONE (fill latency)	Pipeline fill time
7	lbi r0, 0	Instruction in WB (no hazards/stall)
8	lbi r5, 43	Instruction in WB (no hazards/stall)
9	lbi r6, 43	Instruction in WB (no hazards/stall)
10	lbi r7, 43	Instruction in WB (no hazards/stall)
11	ld r1, r0, 0	Instruction in WB (no hazards/stall)
12	NOP (st r5, r1, 0)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall.
13	NOP (st r5, r1, 0)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall.
14	st r5, r1, 0	Instruction in WB (no hazards/stall)
15	ld r1, r0, 2	Instruction in WB (no hazards/stall)
16	NOP (st r6, r1, 1)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall
17	NOP (st r6, r1, 1)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall.
18	st r6, r1, 1	Instruction in WB (no hazards/stall)
19	ld r1, r0, 4	Instruction in WB (no hazards/stall)
20	NOP (st r7, r1, 1)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall.
21	NOP (st r7, r1, 1)	Store instruction depends on r1 (RAW data hazard). This dependency results in a stall.
22	st r7, r1, 1	Instruction in WB (no hazards/stall)
	halt	The program halts.