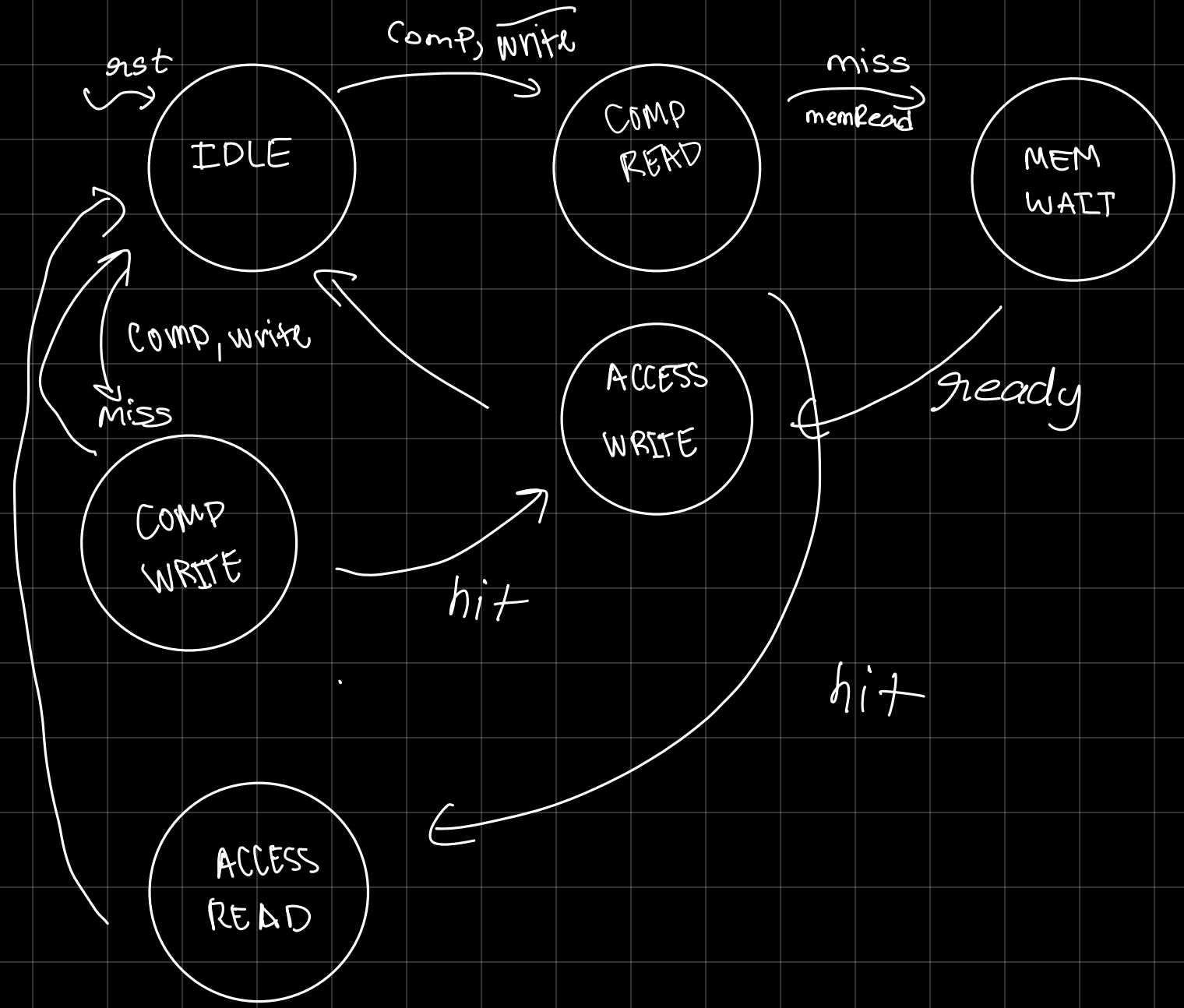
Cache FSM

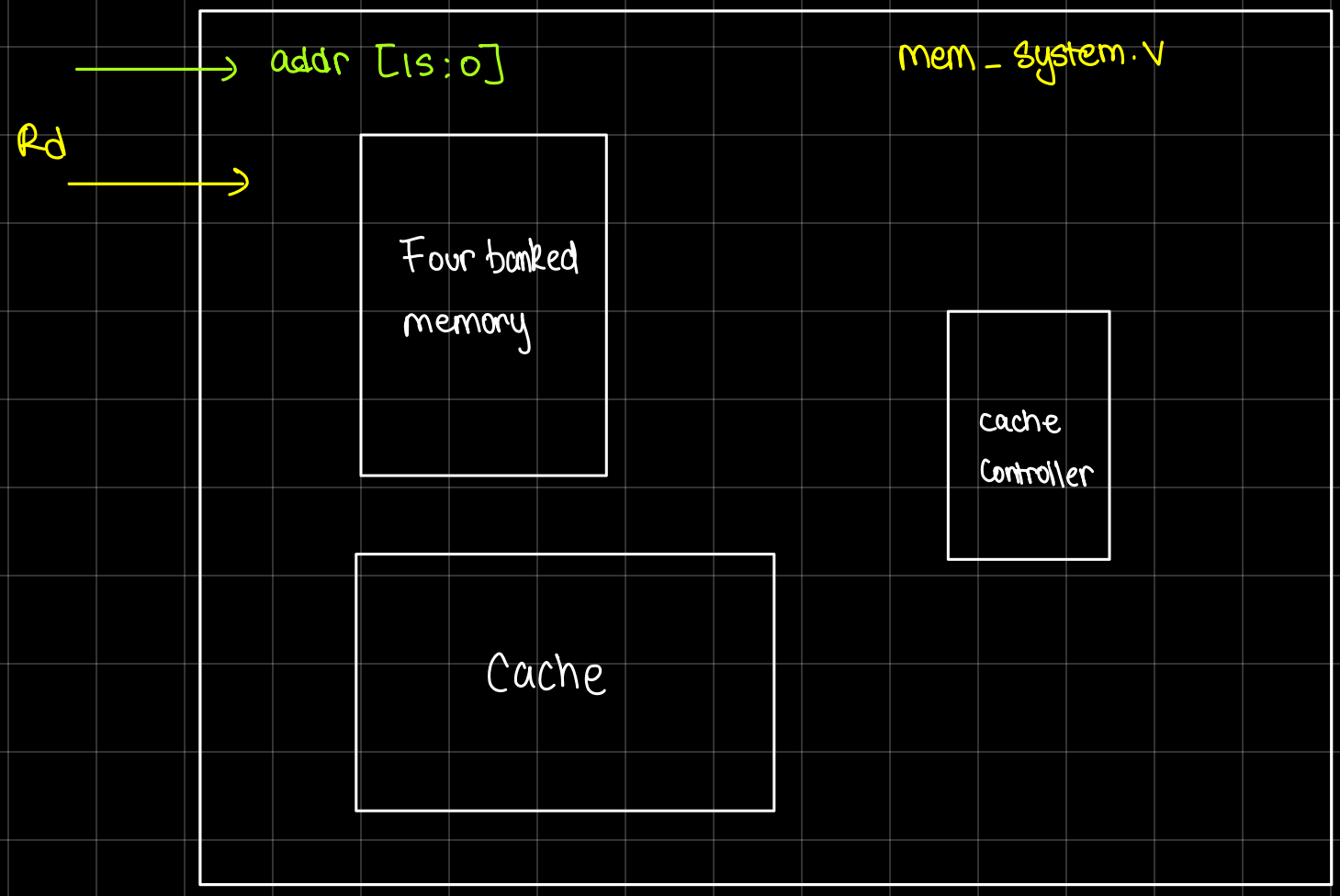
256 lines

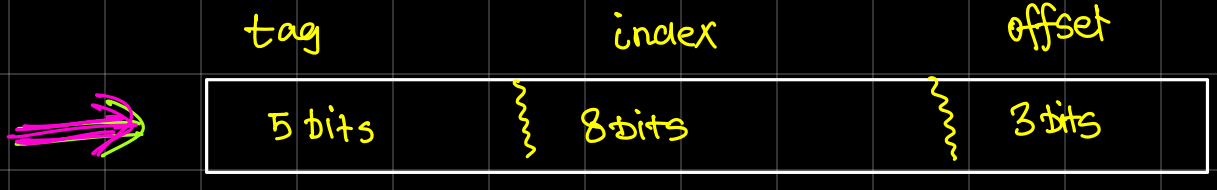
16 { 5 tag bits, 8 index bits, 3 offsets bits }

1 dirty, 1 valid

signals:
- enable
- comp
- write
- valid
- hit
- miss







16 bit addr

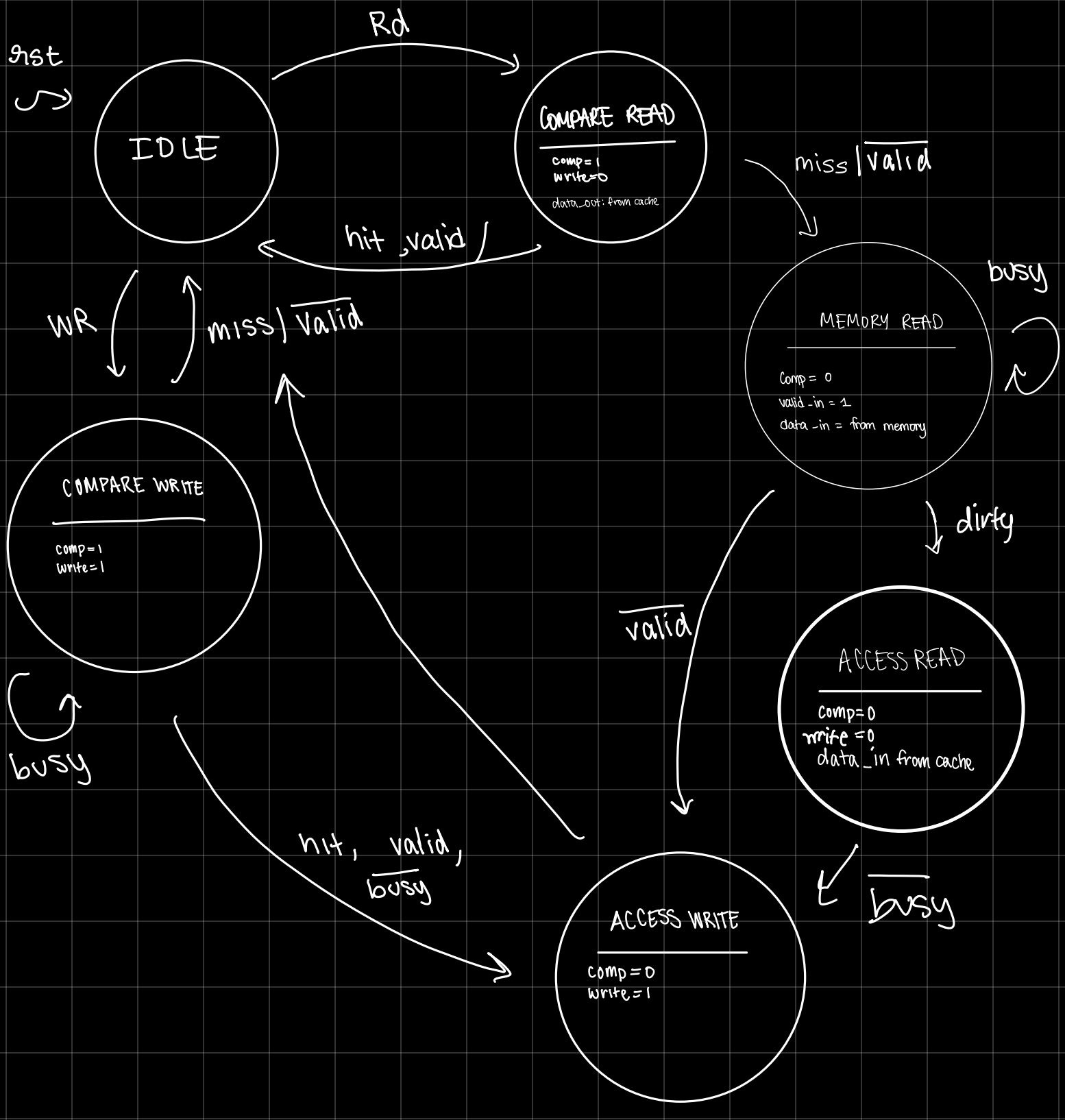
addr [15:11]

addr [10:3]

addr [2:0]

LD: RD ← Mem[ ]

ST: Mem[ ] ← RD


rst
IDLE
Rd
COMPARE READ
comp = 1
write = 0
data_out: from cache
hit, valid
miss | valid
WR
miss | valid
busy
MEMORY READ
Comp = 0
valid_in = 1
data_in = from memory
dirty
COMPARE WRITE
comp = 1
write = 1
busy
valid
ACCESS READ
comp = 0
write = 0
data_in from cache
busy
hit, valid, busy
ACCESS WRITE
comp = 0
write = 1