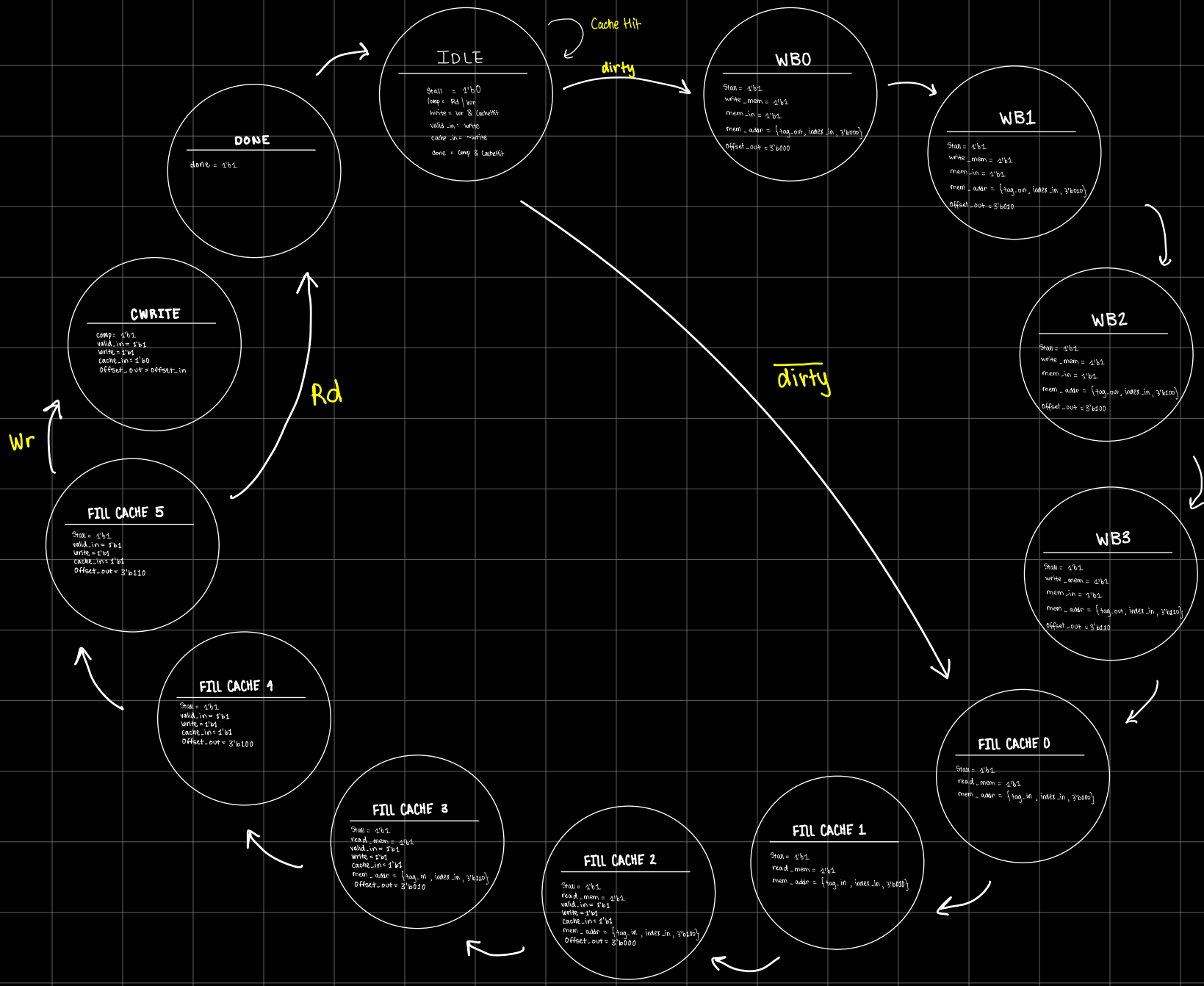
Cache Controller FSM



INPUTS

Rd

Wr

valid

dirty

hit

offset_in

tag_in

tag_out

DEFAULT OUTPUTS

comp = 1'b0

write = 1'b0

write_mem = 1'b0

read_mem = 1'b0

valid_in = 1'b0

Cache_in = 1'b0

mem_in = 1'b0

mem_addr = 16'h000

outset_out = offset_in

done = 1'b0

Stall = 1'b1

CacheHit = comp & valid & hit