

1. Motivation

The fabrication of MOSFET devices requires precise control over numerous interdependent parameters, including temperature, processing duration, chemical concentrations, optical exposure conditions, and thin-film deposition characteristics. Even small deviations in these parameters can substantially affect device performance, yield, and repeatability across a fabrication batch.

In this project, NMOS transistors were fabricated using a 42-step process. However, several key process parameters had not been fully optimized or standardized prior to fabrication, particularly gate oxide growth conditions and doping profiles. Device-to-device variability was therefore expected, and indeed observed, across the fabricated population.

Rather than optimizing a single device in isolation, this work takes a statistical approach: characterizing electrical performance across a large population of fabricated transistors on two separate chips. This enables quantitative assessment of manufacturing repeatability and highlights the dominant sources of process-induced variability.

The primary goals of this project are:

- To evaluate fabrication reliability across a population of NMOS devices on two chips.
- To quantitatively characterize electrical performance (V_{th} , I_{on} , I_{off} , R_{on} , R_{off} , I_{on}/I_{off}) at the chip level and as a function of transistor size.
- To identify statistical correlations between fabrication outcomes and electrical behavior.
- To provide data-driven insights for future process parameter optimization.
- To establish a reproducible, script-based methodology for parameter extraction from Keithley measurement data.



Chip 25 before it snapped in evaporator chamber

2. Fabrication Overview

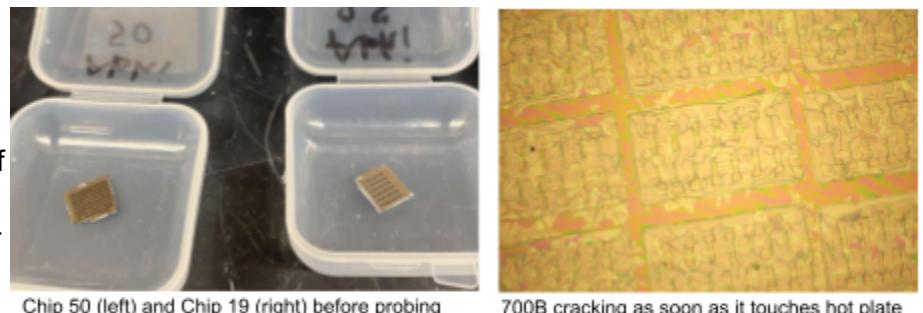
Chip 19 and Chip 50 were fabricated through the standard workflow we've learnt in class/lab:

1. Wafer preparation and cleaning (Acetone+IPA clean)
2. Photolithography patterning (spin-coat, expose, develop)
3. Spin-on dopant (SOD) application and anneal for source/drain doping
4. Metallization via aluminum evaporation
5. Contact formation and lift-off
6. Device probing with Keithley source-measure units

An important distinction between the two chips comes from the aluminum contact insulators. For Chip 19, the intended 700B spin-on silicon oxide layer was deposited and baked (Steps 25-26).

For Chip 50, due to repeated cracking issues during baking the glass, this step was modified and a hard-baked AZ photoresist was used instead of 700B. This material change might be the primary reason for the electrical performance differences observed between

the chips, including the higher threshold voltage and lower off-current on Chip 50. Since fabrication parameters were not fully standardized, these variations are treated as experimental process variables to help guide future process optimization.

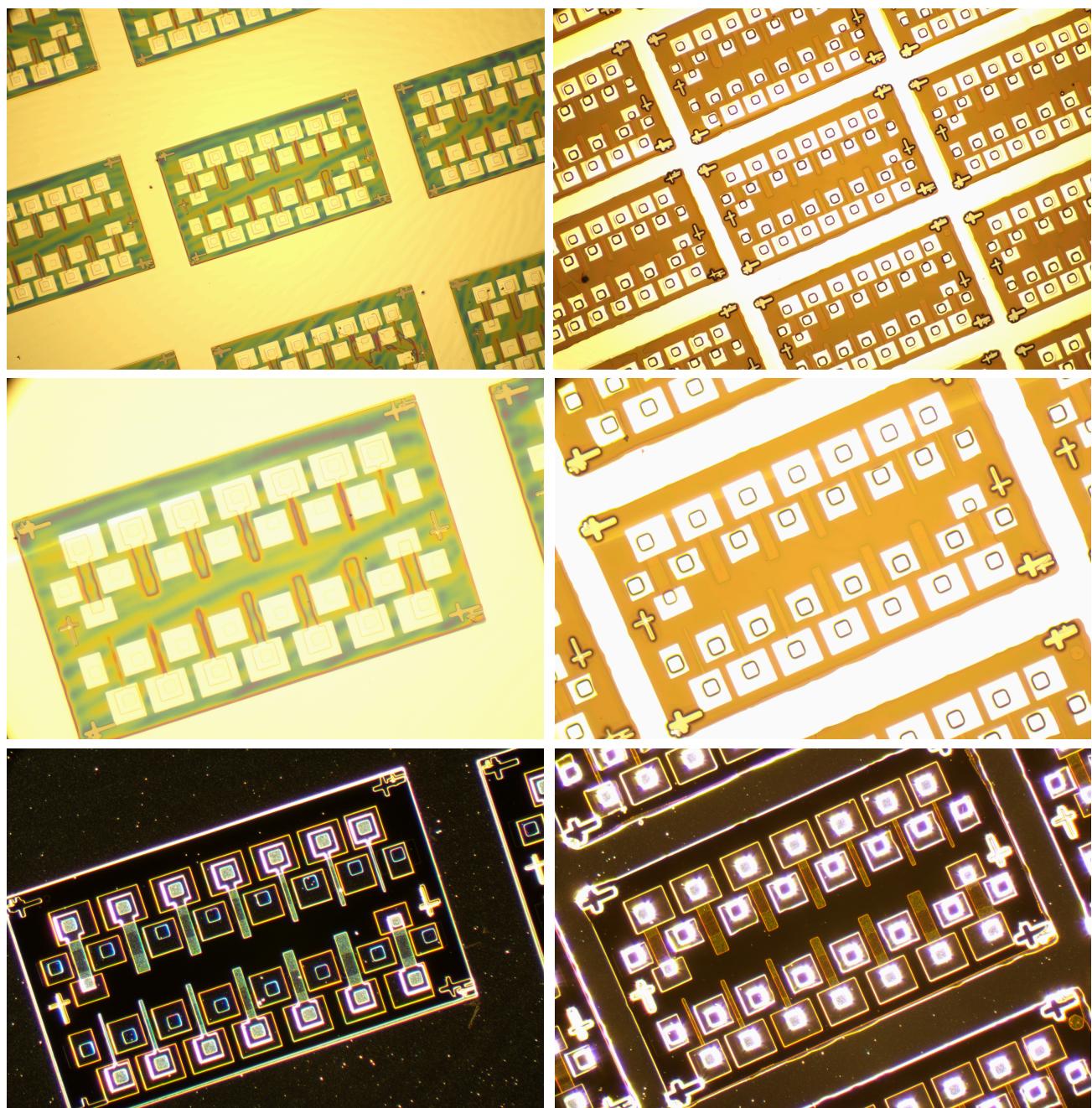


Chip 50 (left) and Chip 19 (right) before probing

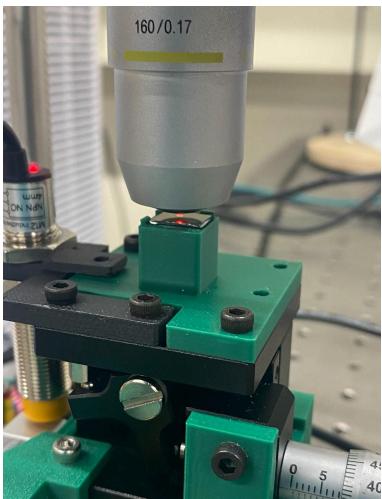


700B cracking as soon as it touches hot plate

Final chips Chip 19 (left) and Chip 50 (right). 10x, 100x, 100x dark field.



3. Fabrication Observations



3.1 Lithography

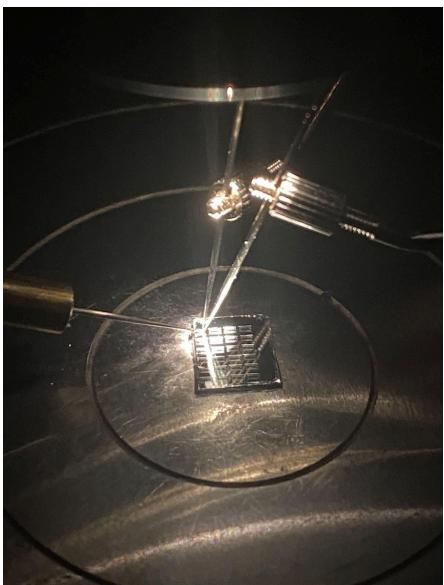
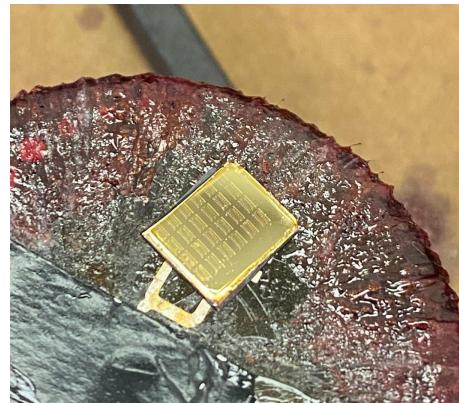
Lithography was one of the most time-intensive stages of the process, along with probing. The absence of autofocus on the stepper and only being able to see 2 alignment markers out of the 4 made accurate layer alignment difficult. Misalignment between the gate, source, and drain patterns was observed in some devices, but overall everything looked good.

<- Chip on stepper

3.2 Chip 50 Contact Insulation Substitution (Steps 25-26)

The 700B/photoresist layer serves as an insulator between the aluminum contacts. Substituting photoresist here would not directly affect gate electrostatics or threshold voltage, but may affect the resistance of the Al-Si contacts. The observed difference in V_{th} between Chip 19 and Chip 50 therefore requires further investigation and cannot be attributed to a change in gate dielectric properties.

Photoresist spun-on after aluminum evaporation ->



3.3 Contact and Probe

Probe contact resistance appeared inconsistent during testing, small adjustments to probe placement sometimes transformed noisy or non-ideal I-V traces into clean NMOS curves. This sensitivity to probe positioning suggests that contact resistance at the probe-metal interface is a significant source of measurement variability, rather than intrinsic device variability alone. 6 out of 100 probes were excluded from analysis due to breakdown behavior or anomalous readings, likely caused by gate damage from probe needle contact during early testing runs.

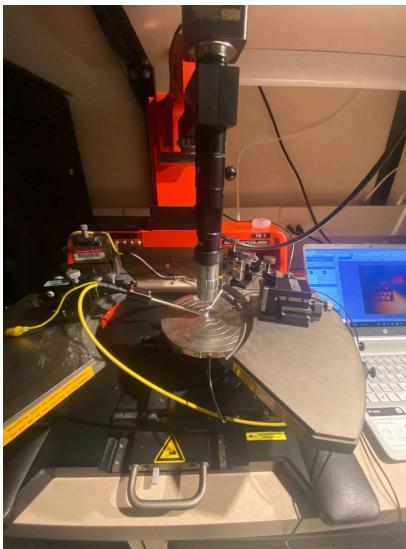
<- Chip 19 on probe station; needles on gate, source, drain

4. Project Status Table

The table below summarizes all deliverables across the three checkpoints. Status is indicated for each deliverable at each checkpoint.

Checkpoint	Deliverable	Status
Checkpoint 1	Fabricate ≥ 100 NMOS transistors	✓
	Probe ≥ 100 transistors	✓
	Count NMOSFETs attempted	✓
	Identify visually correct devices (microscope)	✓
	Identify working NMOSFETs (valid IV behavior)	✓
	Yield calculation (all categories)	✓
	Threshold voltage extraction	✓
	On current / resistance (G-D, S-D)	✓
	Off current / resistance (G-D, S-D)	✓
	On/off current ratio	✓
Checkpoint 2	Chip-level statistics by FET size	✓
	Probe all transistors (verification pass)	NA
	Measure CV curves	NA
	Extract parameters from IV + CV	NA
	Yield statistics (IV + CV)	NA
	Literature & process review	NA
Checkpoint 3	Identify fabrication improvements	NA
	Implement process changes	NA
	Fabricate ≥ 100 new transistors	NA
	Probe all fabricated devices	NA
	Collect IV curves	NA
	Collect CV curves	NA
	Extract parameters & yield statistics	NA

5. Methodology



5.1 Measurement Setup

Electrical characterization was performed using a Keithley source-measure unit (SMU). Each transistor was tested as a three-terminal device, with the source and bulk tied together and held at ground. The gate voltage (V_{gs}) was stepped from 0 V to 6 V in 1 V increments, while the drain voltage (V_{ds}) was swept from 0 V to 6 V at each gate bias. This generated a family of I_d - V_d curves (output characteristics) for each device. One hundred transistors were probed in total: 50 on Chip 19 and 50 on Chip 50. The devices span seven NMOS transistor sizes (gate lengths of 5 μm through 30 μm) across eight spatial pattern positions on each chip.

5.2 Parameter Extraction

Python scripts were written to parse all Keithley .xls output files and extract the following parameters automatically:

Threshold Voltage (V_{th}):

V_{th} was extracted using the linear extrapolation method applied to the transconductance curve at a reference drain voltage. At each gate voltage step, the drain current at the reference drain voltage ($V_{d_ref} = 5 \text{ V}$) was found, the transconductance $gm = dI_d/dV_{gs}$ was computed, and the gate voltage at which the linear extrapolation of the I_d - V_{gs} curve intersects zero current was taken as V_{th} . V_{th} was extracted at four drain biases ($V_d = 0.2 \text{ V}, 1 \text{ V}, 5 \text{ V}, 10 \text{ V}$) to assess drain-induced threshold variation. The $V_d = 5 \text{ V}$ value is used as the primary V_{th} reference in all statistical analyses.

On Current (I_{on}) and On Resistance (R_{on})

I_{on} is defined as the drain current at the maximum gate voltage ($V_{gs} = 6 \text{ V}$) and the reference drain voltage ($V_{ds} = 5 \text{ V}$). R_{on} is computed as V_{ds}/I_d at the same bias point: $R_{on} = 5 \text{ V} / I_{on}$.

Off Current (I_{off}) and Off Resistance (R_{off})

I_{off} is defined as the drain current at $V_{gs} = 0 \text{ V}$ and the reference drain voltage ($V_{ds} = 5 \text{ V}$). $R_{off} = 5 \text{ V} / I_{off}$.

On/Off Current Ratio

The I_{on}/I_{off} ratio is computed directly from the extracted I_{on} and I_{off} values: $I_{on}/I_{off} = I_{on} / I_{off}$. This is a number that quantifies the switching contrast of the transistor.

5.3 Quality Control

After automated extraction, each device's I-V graph was inspected visually. Devices exhibiting breakdown behavior, non-monotonic curves not consistent with NMOS operation, or clearly anomalous parameter values were flagged and excluded from statistical averages. Six devices out of 100 were excluded on this basis, leaving 94 valid devices in the final dataset.

5.4 Statistical Analysis

For each parameter, mean and standard deviation were computed both at the chip level (Chip 19 vs. Chip 50) and at the FET size level (NMOS 1–7). It should be noted that the gate dielectric (a 20 nm thermally grown SiO_2 pre-deposited on the wafer) is identical for both chips, so the chip-level comparison does not isolate a gate dielectric difference. The size-dependent analysis

reveals how transistor gate length affects device behavior, notably the expected decrease in I_{on} and increase in R_{on} with increasing channel length.

5.5 Parameter Formulas and Sample Calculations

This section presents every formula used for parameter extraction and then applies each formula to a real device from the dataset to show exactly how the numbers in the results tables were produced. Two example devices are used: NMOS 1, Pattern 2, Chip 19 (a Chip 19 representative) and NMOS 1, Pattern 1, Chip 50 (a Chip 50 representative). Both were measured at $V_{ds} = 5$ V reference.

5.5.1 On Current (I_{on})

I_{on} is the drain current measured when the transistor is fully on, at maximum gate voltage and the reference drain voltage:

$$I_{on} = I_d(V_{gs} = 6 \text{ V}, V_{ds} = 5 \text{ V})$$

This value is read directly from the Keithley sweep data at the $V_{gs} = 6$ V row and the $V_{ds} = 5$ V column.

Chip 19 example: $I_{on} = 18.57$ mA

Chip 50 example: $I_{on} = 3.277$ mA

5.5.2 Off Current (I_{off})

I_{off} is the residual leakage current when the transistor is nominally off, gate grounded, drain biased:

$$I_{off} = I_d(V_{gs} = 0 \text{ V}, V_{ds} = 5 \text{ V})$$

This is read from the $V_{gs} = 0$ V row in the same sweep data.

Chip 19 example: $I_{off} = 65.14 \mu\text{A}$ (6.514×10^{-5} A)

Chip 50 example: $I_{off} = 0.969 \mu\text{A}$ (9.691×10^{-7} A)

5.5.3 On Resistance (R_{on})

R_{on} is derived from Ohm's law at the on-state bias point. It represents the total series resistance in the conducting channel including contact resistance:

$$R_{on} = V_{ds} / I_{on} = 5 \text{ V} / I_{on}$$

Chip 19: $R_{on} = 5 \text{ V} / 18.57 \times 10^{-3} \text{ A} = 269.3 \Omega$

Chip 50: $R_{on} = 5 \text{ V} / 3.277 \times 10^{-3} \text{ A} = 1525.7 \Omega$

5.5.4 Off Resistance (R_{off})

R_{off} is Ohm's law at the off-state bias point. A high R_{off} indicates the channel is effectively blocking current when the gate is grounded:

$$R_{off} = V_{ds} / I_{off} = 5 \text{ V} / I_{off}$$

Chip 19: $R_{off} = 5 \text{ V} / 6.514 \times 10^{-5} \text{ A} = 76,755 \Omega$ (76.8 kΩ)

Chip 50: $R_{off} = 5 \text{ V} / 9.691 \times 10^{-7} \text{ A} = 5,159,597 \Omega$ (5.16 MΩ)

5.5.5 *Ion/Ioff Ratio*

The on/off current ratio is the primary figure of merit for digital switching. It quantifies how many orders of magnitude the device current changes between its on and off states:

$$\text{Ion/Ioff} = \text{Ion} / \text{Ioff}$$

$$\text{Chip 19: } 18.57 \times 10^{-3} / 6.514 \times 10^{-5} = 285.0$$

$$\text{Chip 50: } 3.277 \times 10^{-3} / 9.691 \times 10^{-7} = 3381.7$$

5.5.6 *Threshold Voltage (V_{th}) Linear Extrapolation Method*

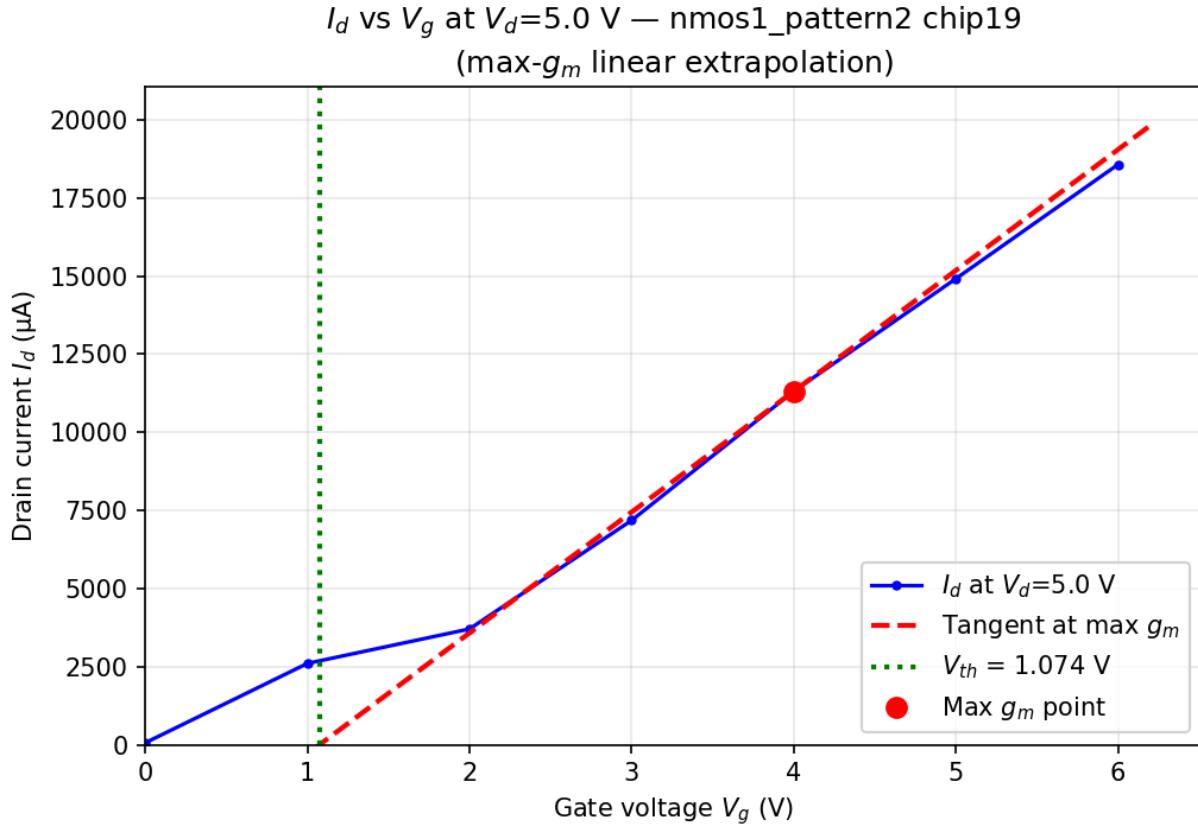
V_{th} cannot be read directly from the I-V data; it must be extracted by fitting a line to the I_d - V_{gs} transfer curve in its linear region. The procedure is:

1. From the per-gate-voltage sweep data, collect I_d at $V_{ds} = 5 \text{ V}$ for each V_{gs} step (0 V, 1 V, 2 V, ... 6 V).
2. Find the gate voltage step where transconductance $gm = \Delta I_d / \Delta V_{gs}$ is maximum. This is the steepest part of the transfer curve.
3. Fit a tangent line through that point: $I_d(V_{gs}) \approx gm_{\text{max}} \times (V_{gs} - V_{th})$
4. V_{th} is the x-intercept of this line: $V_{th} = V_{gs_at_peak_gm} - I_d_{at_peak_gm} / gm_{\text{max}}$

The per-gate-voltage data for the Chip 19 example device (nmos1, pattern2) is shown:

V_{gs} (V)	I_d at $V_{ds} = 5\text{V}$ (A)	ΔI_d (A)	$gm = \Delta I_d / \Delta V_{gs}$ (A/V)
0	6.514×10^{-5}	-	-
1	2.604×10^{-3}	$+2.539 \times 10^{-3}$	2.539×10^{-3}
2	3.707×10^{-3}	$+1.103 \times 10^{-3}$	1.103×10^{-3}
3	7.182×10^{-3}	$+3.475 \times 10^{-3}$	3.475×10^{-3}
4	1.131×10^{-2}	$+3.130 \times 10^{-3}$	3.130×10^{-3}
5	1.491×10^{-2}	$+3.602 \times 10^{-3}$	3.602×10^{-3}
6	1.857×10^{-2}	$+3.651 \times 10^{-3}$	3.651×10^{-3} (peak gm)

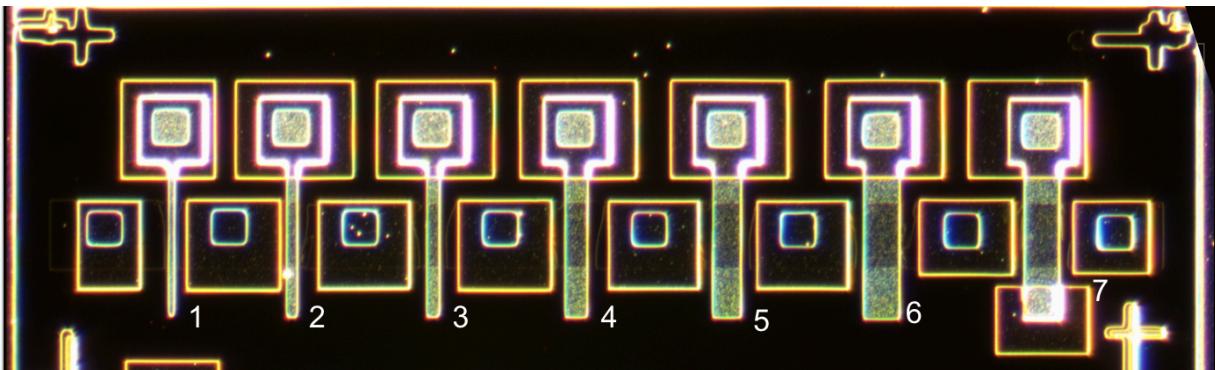
The script finds the maximum gm step (here $gm = 3.651 \times 10^{-3}$) and extrapolates the tangent line back.



6. Dataset Description

6.1 Raw Measurement Data

The raw dataset consists of 100 Keithley-generated .xls files, one per probed transistor. Each file contains Id-Vd sweep data for gate voltages from 0 to 6 V. Files are named according to the convention: nmos{1-7}_pattern{1-8}_chip{19/50}, where the nmos number encodes the gate length (NMOS 1 = 5 μ m through NMOS 7 = 30 μ m) and the pattern number encodes the spatial position on the chip.



6.2 Processed Data

A Python script parsed all raw files and generated a summary CSV (nmos_summary.csv) containing one row per functional device (94 rows) with the following columns: chip identifier,

NMOS number, pattern number, FET size label, source filename, V_{th} at four drain biases, reference drain voltage, I_{on}, I_{off}, R_{on}, R_{off}, and I_{on}/I_{off} ratio.

A second CSV (nmos_summary_per_gate_voltage.csv) contains per-gate-voltage breakdown data, allowing analysis of how drain current and resistance evolve as a function of gate bias for each device.

6.3 Graphs

Individual Id-Vd family-of-curves graphs were generated for all 94 functional transistors. Example graphs for representative devices are included in Section 8 and Section 9.

7. Fabrication and Yield Statistics

7.1 Devices Attempted

Total NMOSFETs attempted fabrication: Chip 19 was originally labeled Chip 25, but it snapped during removal from the aluminum evaporator, leaving only half of the chip usable. The total attempted fabrication count is:

$$N_{\text{attempted}} = 14 \text{ FETs/pattern} \times 68 \text{ patterns} = 952 \text{ transistors}$$

7.2 Visual Fabrication Yield

Devices were inspected under the microscope prior to electrical testing. A device was classified as visually passing if it had: (1) a continuous, unbroken gate region; (2) clearly defined and accessible source and drain contacts; and (3) no evidence of structural breaks, severe misalignment, or photoresist/metal residue bridging critical regions.

$$N_{\text{visual_pass}} = 900 \text{ transistors} \rightarrow \text{Yield_visual} = 900 / 952 = 94.5\%$$

7.3 Electrical Yield

Of the 100 devices probed (50 per chip), 94 exhibited recognizable NMOS I-V behavior: increasing drain current with gate voltage, a cutoff-to-saturation transition, and extractable parameters. Six devices were excluded due to breakdown behavior, erratic readings, or suspected gate damage from probe needle contact during early testing sessions (before probing technique was refined).

$$N_{\text{functional}} = 94 \quad N_{\text{probed}} = 100 \rightarrow \text{Yield_electrical} = 94\%$$

Post-inspection functional yield (functional yield conditioned on visual pass) will be computed in Checkpoint 2 once complete pattern mapping data is available.

8. Chip-Level Analysis

Parameter	Chip 19	Chip 50
Devices probed	50	50
Functional devices	48	46
Electrical yield	96%	92%
V _{th} @ V _d =5V (mean ± std)	1.26 ± 0.31 V	3.43 ± 0.40 V
I _{on} (mean ± std)	5.42 ± 3.40 mA	2.06 ± 0.70 mA
I _{off} (mean ± std)	71.7 ± 413.8 μA	1.70 ± 2.76 μA
R _{on} (mean ± std)	1,214 ± 733 Ω	2,696 ± 860 Ω
I _{on} /I _{off} ratio (mean ± std)	738 ± 657	6,404 ± 8,488
Dielectric	Spin on glass (SiO ₂)	Photoresist

Note: The V_{th}, I_{on}, I_{off}, R_{on}, and I_{on}/I_{off} values in this table are means computed across all 7 NMOS gate lengths together (5μm through 30μm). Because I_{on} varies strongly with gate length (a 5μm device conducts ~4.5× more than a 30μm device on Chip 19), pooling all sizes produces a large standard deviation. This is expected and does not indicate random fabrication failure. It reflects the deliberate range of device sizes tested. Per-size breakdowns are in Section 9.

8.1 Why Chip 50 Has a Higher Threshold Voltage

The reason for Chip 50's elevated threshold voltage (~3.43 V vs. ~1.26 V on Chip 19) is not yet fully understood. Since the gate dielectric is a pre-deposited 20 nm SiO₂ layer identical on both wafers, it cannot explain the V_{th} difference through a change in Cox. The process deviation at Steps 25-26 (photoresist substituted for 700B) affects the metal contact insulation layer rather than the gate stack, so a direct electrostatic explanation via dielectric properties does not apply. A more likely contributing factor may be a difference in Al-Si contact resistance or doping activation uniformity between the two chips. This will be investigated further in Checkpoint 2.

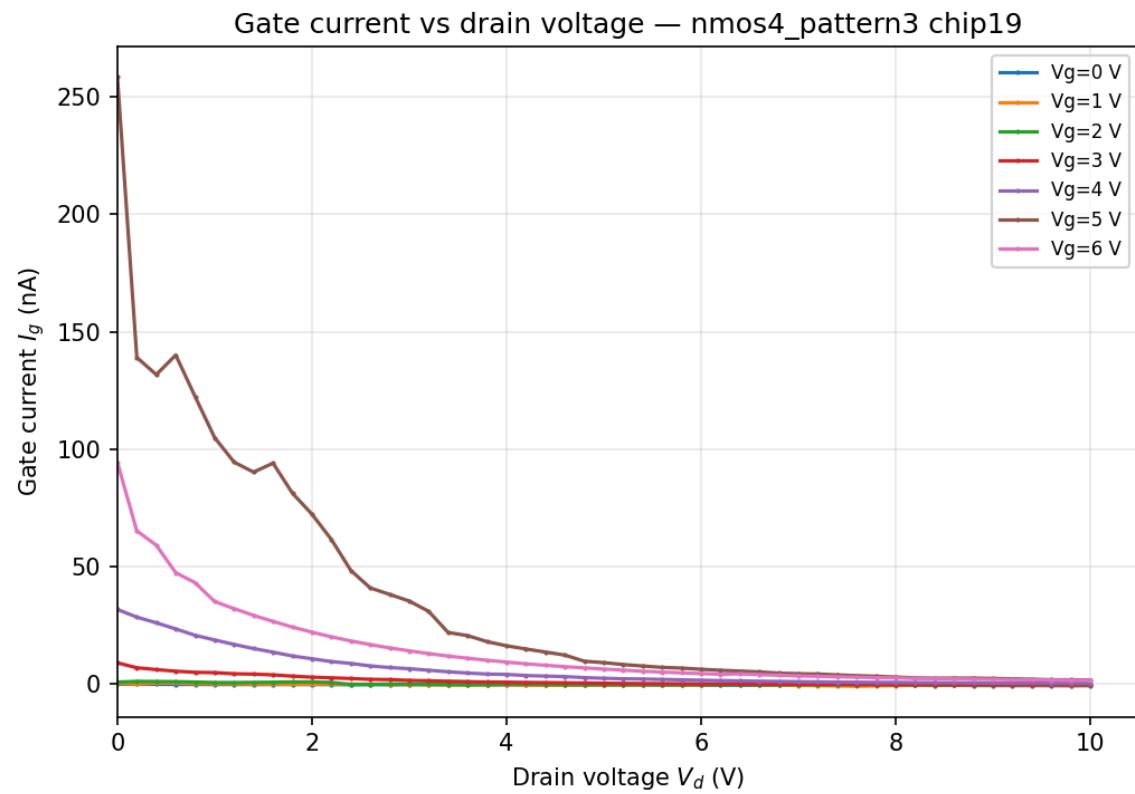
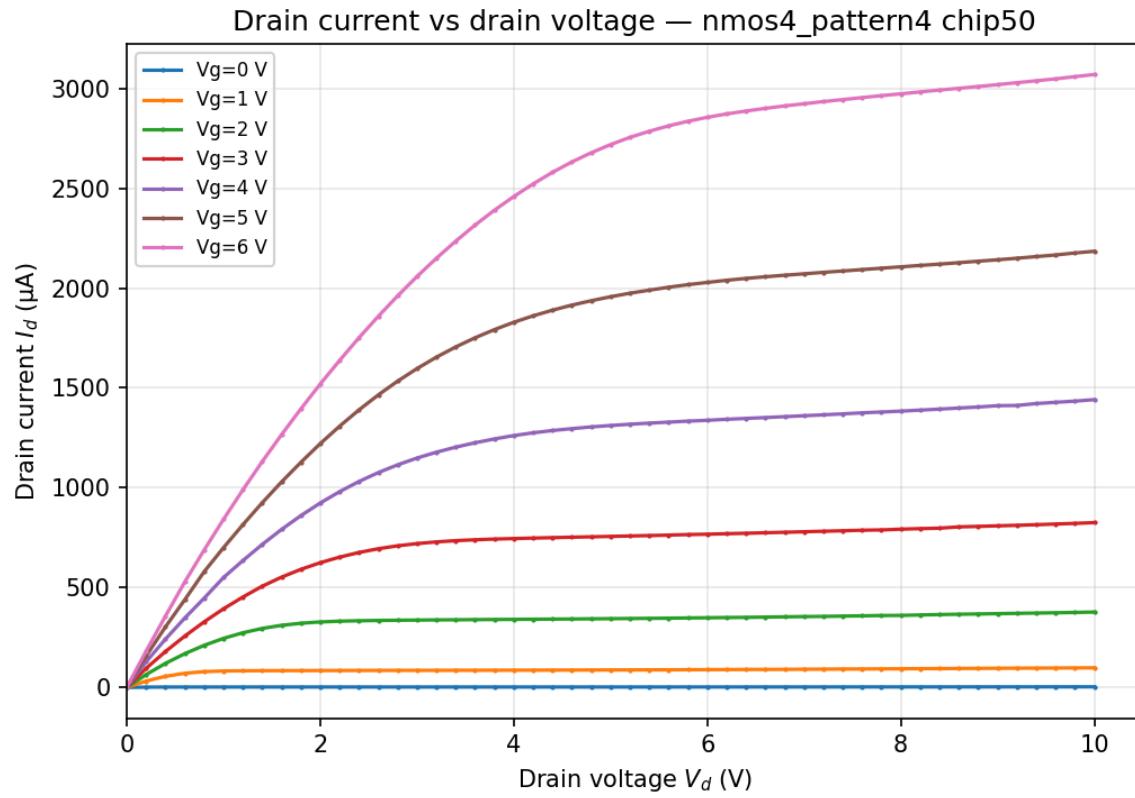
8.2 Why Chip 50 Has Lower I_{off} and Better I_{on}/I_{off}

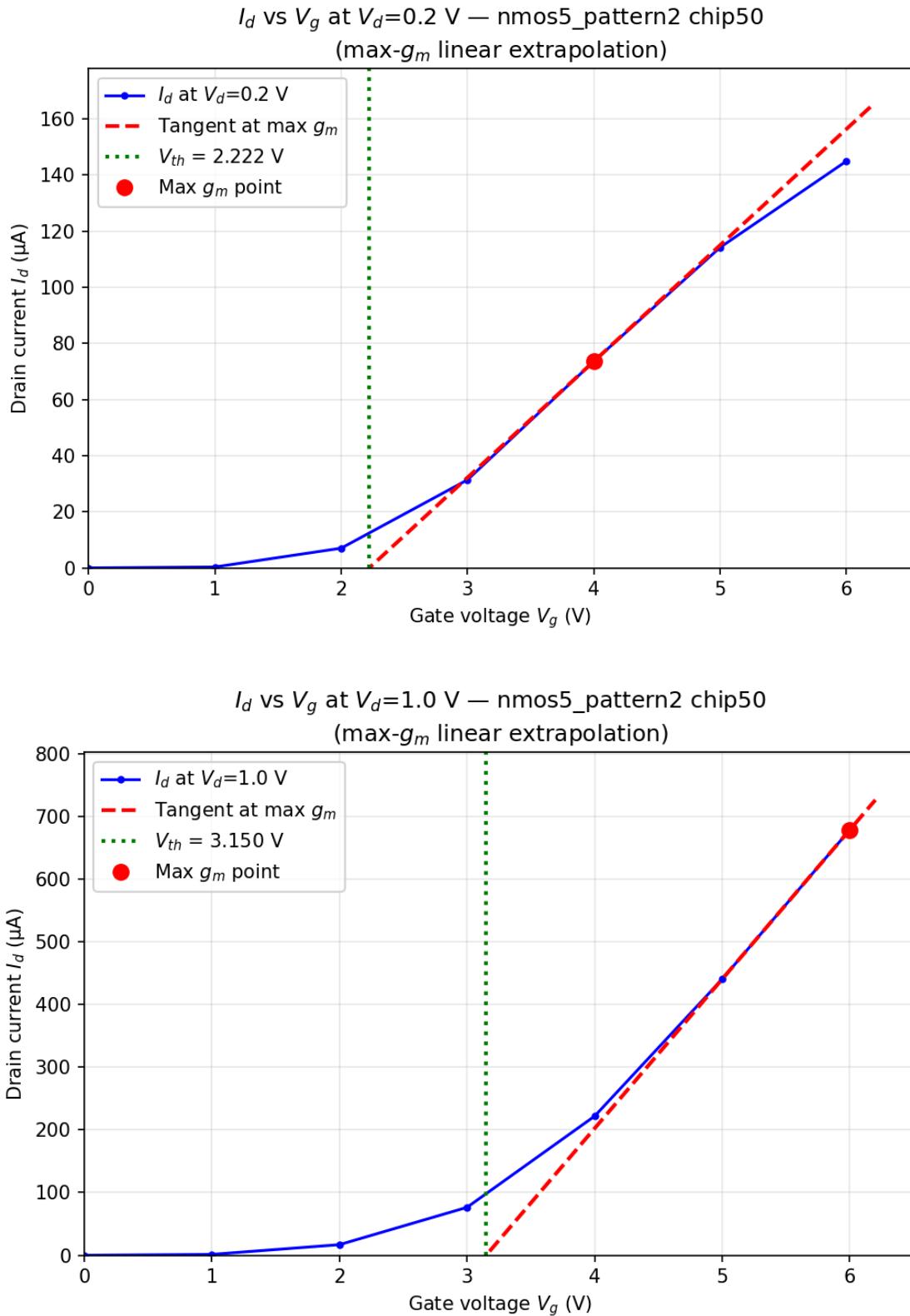
Something to do with overdrive voltage (V_{gs} - V_{th}). Leaving this here for future research.

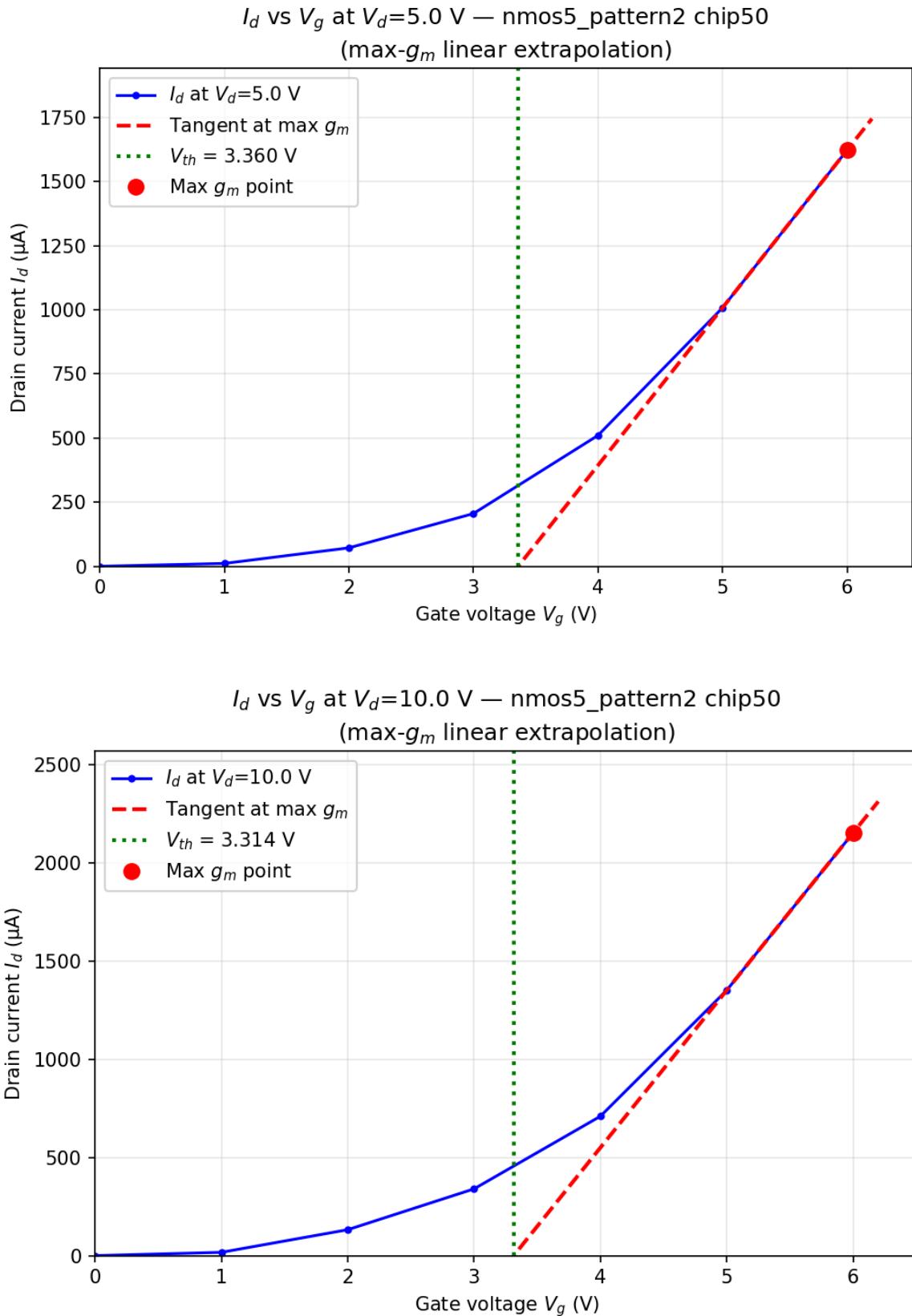
8.3 Why Chip 50 Has Lower I_{off} and Better I_{on}/I_{off}

Chip 50's photoresist dielectric suppresses off-state leakage far more effectively than Chip 19's spin-on glass. I don't really get the reasoning behind this as well so I will have to look more into this for the upcoming checkpoint.

The titles of the graphs below explain what the graph shows. I have created this set of graphs for all 94 transistors. You can find them in Section 11.







9. FET Size-Dependent Analysis

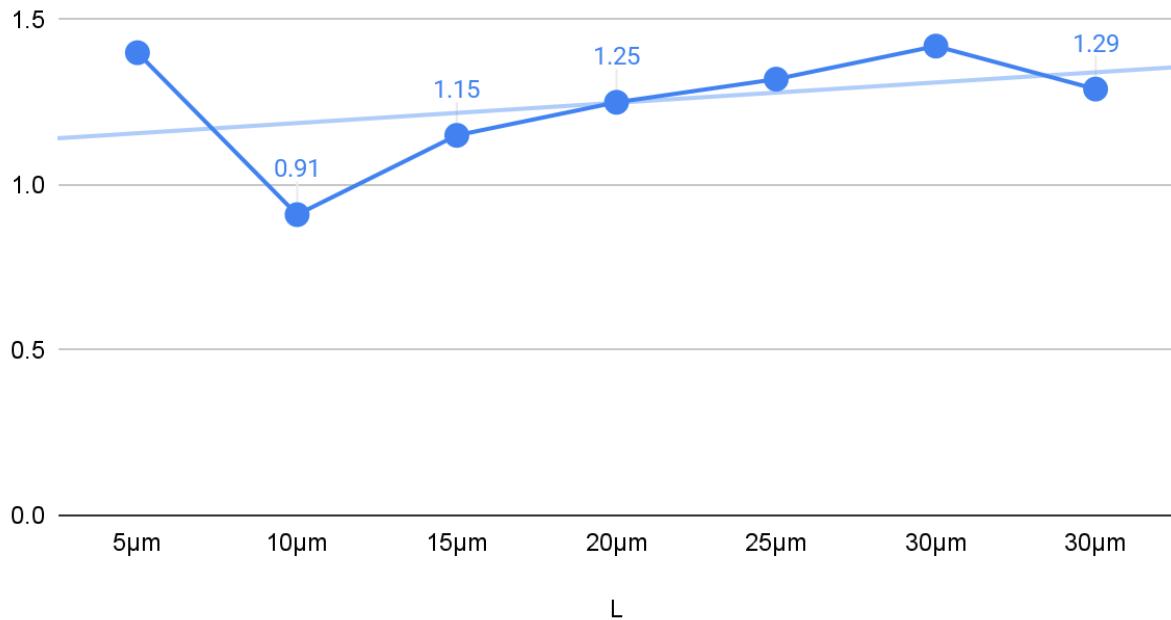
Seven NMOS transistor sizes were fabricated, with gate lengths from 5 μm (NMOS 1) to 30 μm (NMOS 6 and 7). The tables below show mean \pm std for each parameter, broken out separately for each chip so the within-chip size trends are not obscured by the chip-to-chip dielectric difference.

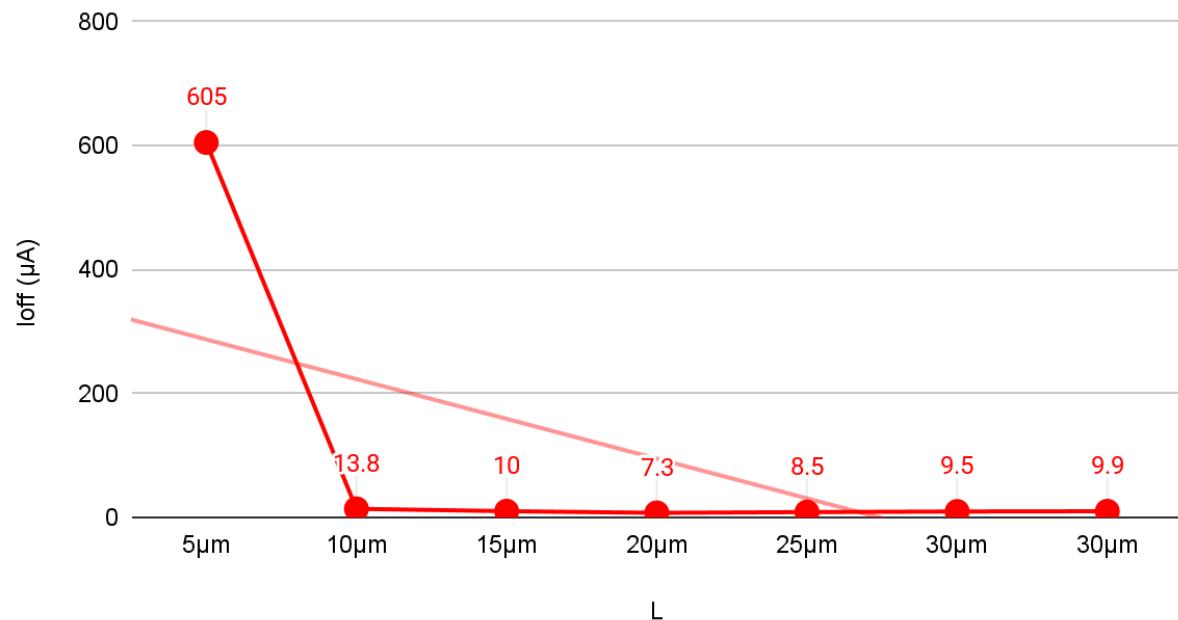
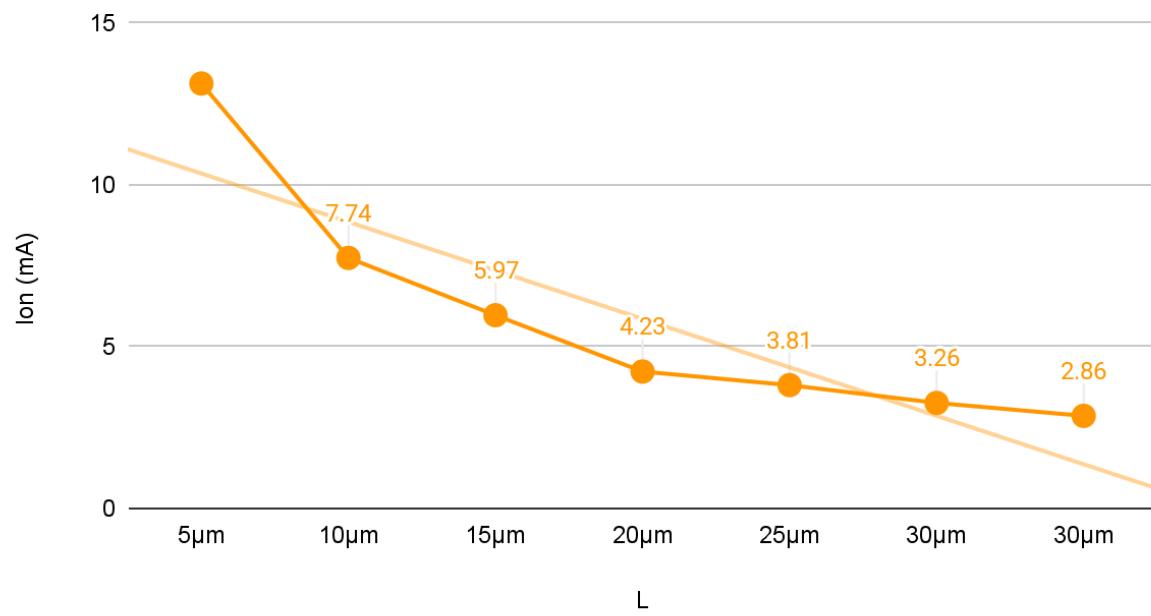
IMAGE

9.1 Chip 19: Per FET Size (700B Spin-On Glass Dielectric)

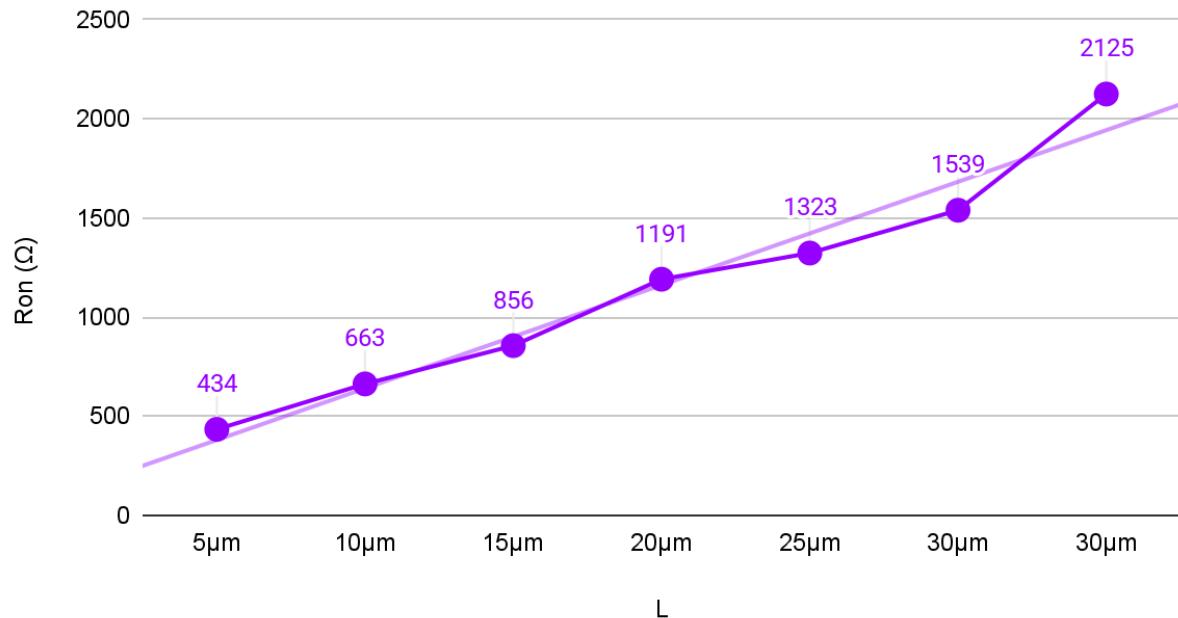
NMOS	L	Quantity	$V_{th} \pm \sigma$ (V)	$I_{on} \pm \sigma$ (mA)	$I_{off} \pm \sigma$ (μA)	$R_{on} \pm \sigma$ (Ω)
1	5 μm	5	1.40 ± 0.64	13.13 ± 4.41	605 ± 1271	434 ± 206
2	10 μm	6	0.91 ± 0.26	7.74 ± 1.28	13.8 ± 5.5	663 ± 127
3	15 μm	7	1.15 ± 0.35	5.97 ± 0.91	10.0 ± 4.0	856 ± 146
4	20 μm	7	1.25 ± 0.16	4.23 ± 0.41	7.3 ± 3.5	$1,191 \pm 124$
5	25 μm	8	1.32 ± 0.13	3.81 ± 0.35	8.5 ± 5.8	$1,323 \pm 139$
6	30 μm	8	1.42 ± 0.18	3.26 ± 0.20	9.5 ± 8.8	$1,539 \pm 97$
7	30 μm	7	1.29 ± 0.16	2.86 ± 0.91	9.9 ± 13.3	$2,125 \pm 1,416$

V_{th} (V) vs. L



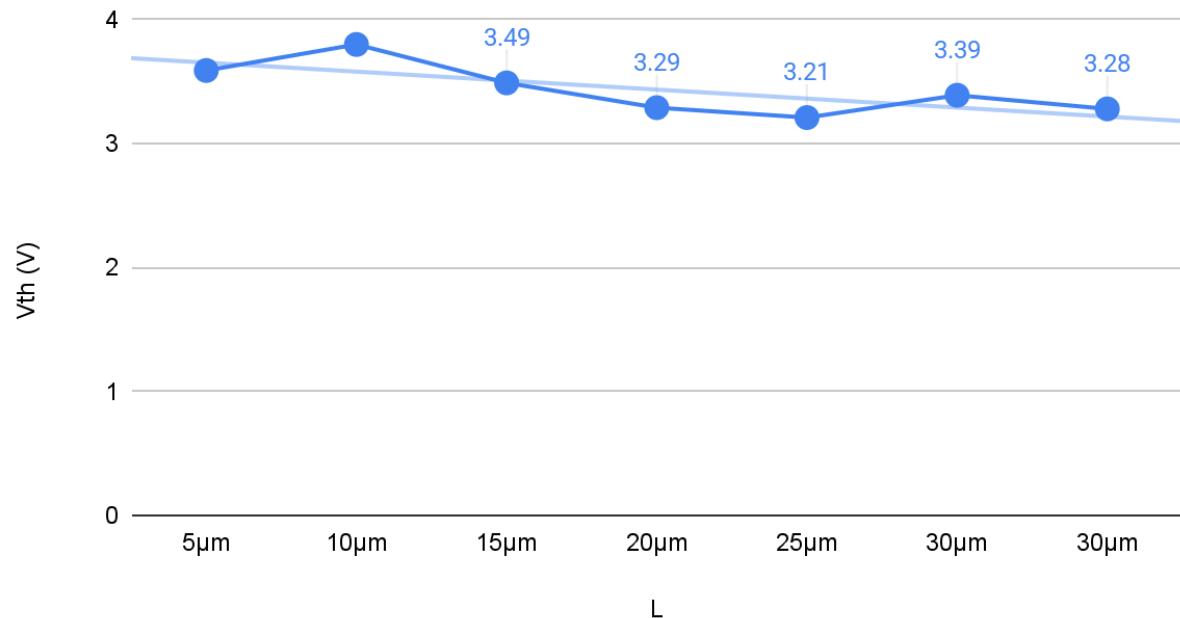
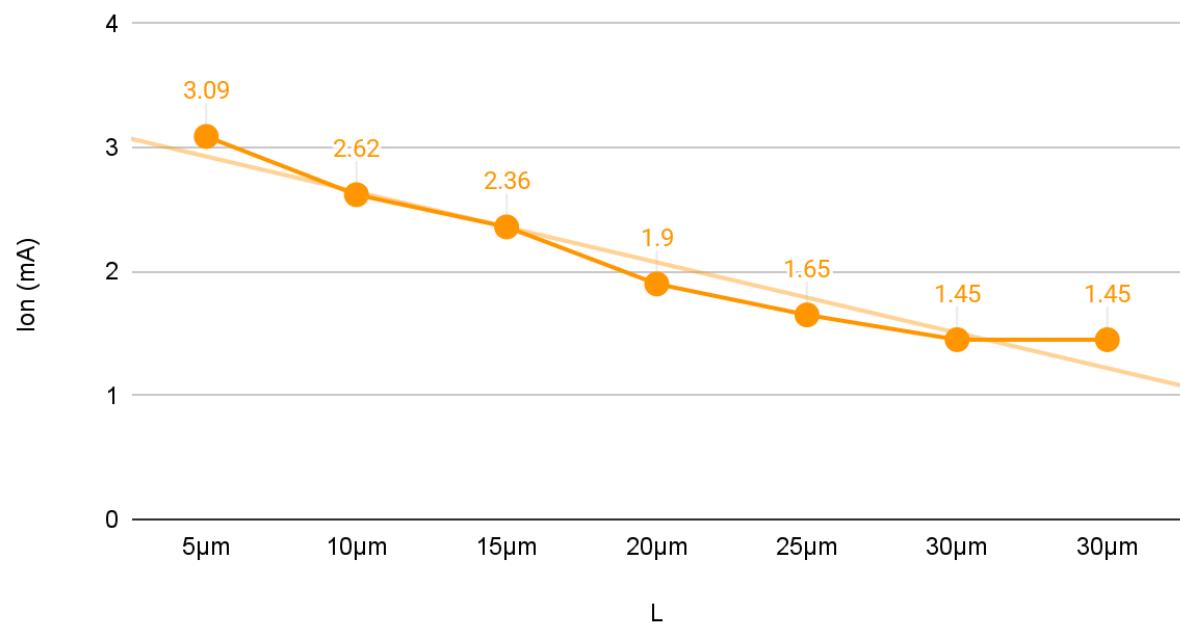
I_{off} (μ A) vs. L**I_{on} (mA) vs. L**

Ron (Ω) vs. L

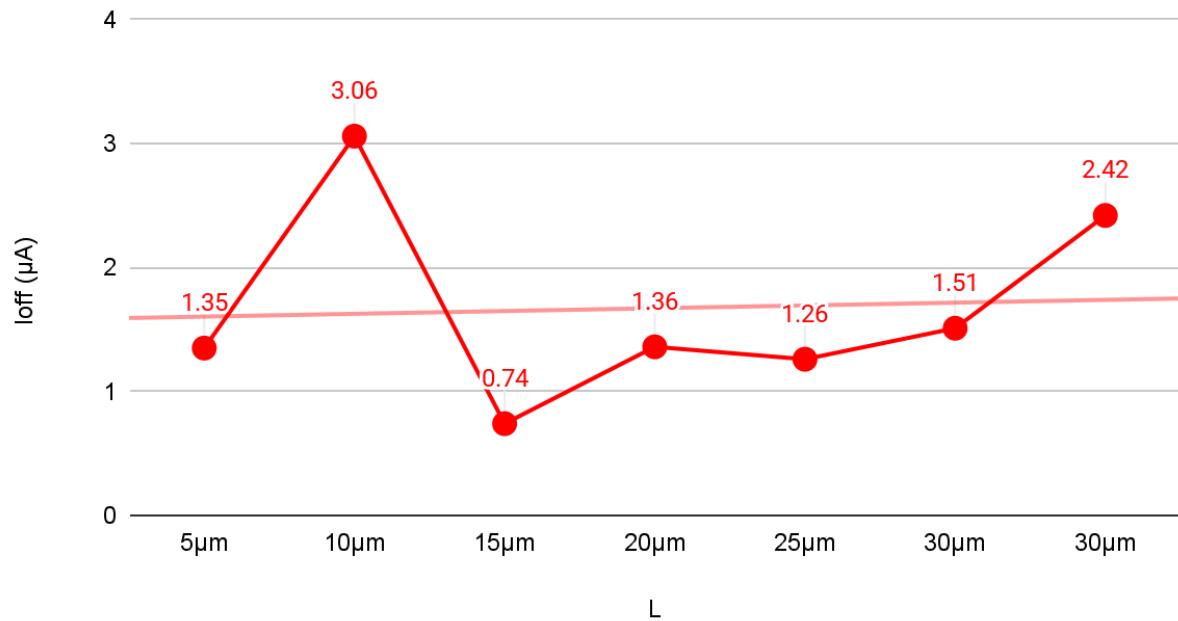


9.2 Chip 50: Per FET Size (Baked AZ Photoresist Dielectric)

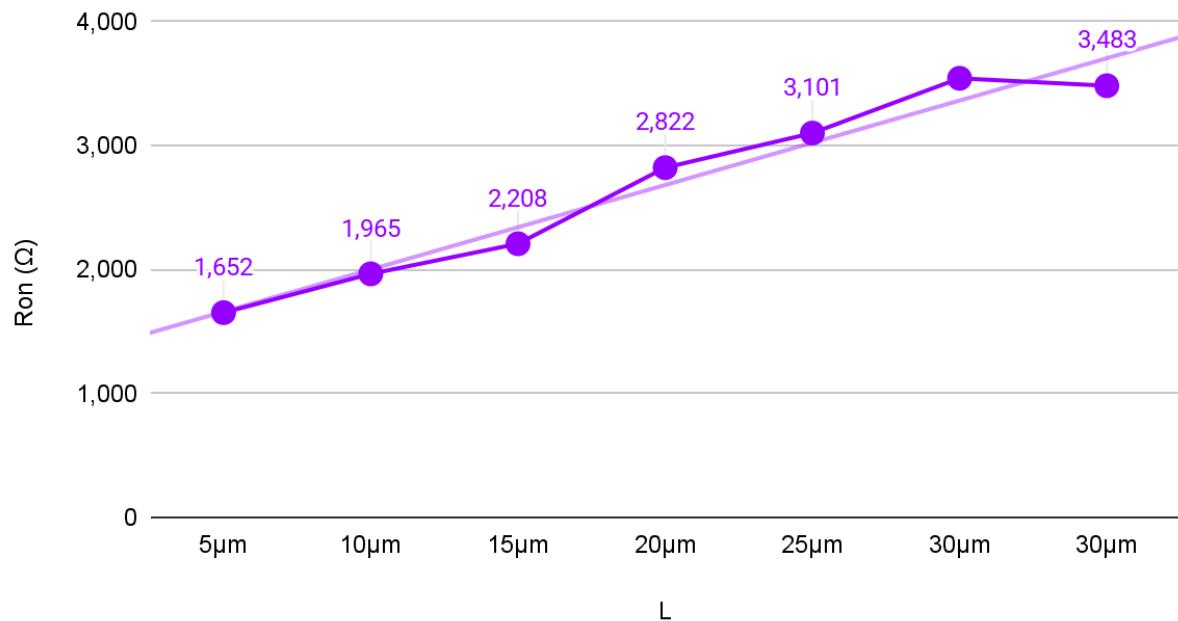
NMOS	L	Quantity	V _{th} $\pm \sigma$ (V)	I _{on} $\pm \sigma$ (mA)	I _{off} $\pm \sigma$ (μA)	Ron $\pm \sigma$ (Ω)
1	5 μm	6	3.59 \pm 0.44	3.09 \pm 0.46	1.35 \pm 2.20	1,652 \pm 255
2	10 μm	7	3.80 \pm 0.38	2.62 \pm 0.51	3.06 \pm 6.06	1,965 \pm 355
3	15 μm	6	3.49 \pm 0.33	2.36 \pm 0.53	0.74 \pm 0.81	2,208 \pm 501
4	20 μm	7	3.29 \pm 0.43	1.90 \pm 0.51	1.36 \pm 2.07	2,822 \pm 894
5	25 μm	7	3.21 \pm 0.43	1.65 \pm 0.28	1.26 \pm 2.03	3,101 \pm 457
6	30 μm	6	3.39 \pm 0.30	1.45 \pm 0.24	1.51 \pm 1.17	3,543 \pm 734
7	30 μm	7	3.28 \pm 0.24	1.45 \pm 0.12	2.42 \pm 1.45	3,483 \pm 309

V_{th} (V) vs. LI_{on} (mA) vs. L

I_{off} (μ A) vs. L



R_{on} (Ω) vs. L



9.3 Trends and Interpretation

I_{on} decreases with increasing gate length. On Chip 19, NMOS 1 ($5\mu m$) averages 13.13 mA vs. 2.86 mA for NMOS 7 ($30\mu m$), a $4.6x$ difference. On Chip 50, NMOS 1 averages 3.09 mA vs. 1.45 mA for NMOS 7, a $2.1x$ difference. The standard is I_{on} proportional to W/L (longer length less I_{on}), so this trend is expected.

R_{on} increases monotonically with gate length, consistent with the decreasing I_{on} trend since $R_{on} = V_{ds}/I_{on}$. On Chip 19: 434Ω (NMOS 1) $\rightarrow 2,125\Omega$ (NMOS 7). On Chip 50: $1,652\Omega$ (NMOS 1) $\rightarrow 3,483\Omega$ (NMOS 7). Chip 50 R_{on} values are consistently $\sim 3\text{-}4x$ higher than Chip 19 at every size, directly a consequence of the lower I_{on} from the higher- V_{th} photoresist dielectric.

V_{th} is very consistent across all 7 sizes within each chip. Chip 19 V_{th} ranges from 0.91 V (NMOS 2) to 1.42 V (NMOS 6), a spread of only 0.51 V across 7 sizes. Chip 50 ranges from 3.21 V (NMOS 5) to 3.80 V (NMOS 2), a spread of 0.59 V . This confirms that V_{th} is set by the dielectric and doping properties, not the gate length.

I_{off} shows no strong size trend on either chip, which is expected. The high I_{off} std values (especially on Chip 19) reflect device-to-device variation in sub-threshold leakage, likely driven by doping non-uniformity and probe contact variability.

10. Discussion and Conclusion

For digital switching applications, Chip 50's characteristics are more useful. Though its V_{th} of 3.43 V is high for most standard supply voltages, and would need to be reduced through process optimization (thinner or higher- k dielectric).

Within each chip, the variability in extracted parameters is substantial. Standard deviations for I_{on} are 63% of the mean for Chip 19 and 34% for Chip 50. This reflects the non-optimized nature of the fabrication process, particularly the inconsistency of probe contact resistance, alignment variability in lithography, and non-uniform doping across the chip. Critically, minor repositioning of probe needles was observed to dramatically change measured I-V characteristics, suggesting that some reported variability is extrinsic (probe-related) rather than intrinsic to the devices.

The size-dependent trend of decreasing I_{on} with increasing gate length is expected for standard MOSFET theory.

Overall electrical yield was 94%, indicating that the fabrication process, while variable, is capable of reliably producing functional NMOS transistors. Continued refinement of lithography alignment, doping uniformity, and probing technique are the highest-priority next steps for improving both yield and parameter consistency.

11. Links

1. [Images of chip going through fabrication process](#)
2. [Processed data nmos_summary_per_gate_voltage.csv](#)
3. [Processed data nmos_summary.csv](#)
4. [All graphs \(564 in total each of 94 transistors have 6 graphs associated\)](#)