CO262 - Computer Organization and Architecture

A3 - Design the RISC-V Datapath in Verilog

- Objective: Integrate all the modules built so far into a working RISC-V datapath.
- **Deadline:** 9AM, January, 21, 2019.
- **Submission guidelines:** Team assignment. Team size <= 2. Pack code, screenshots, testcases, etc. in an archive. Mail to co262.nitk@gmail.com.

1. Design a Combinational Control Unit for the RISC-V Processor (ALU Control + Main Control Unit). Use the subset of instructions defined in Fig. 4.12 (Page 252) of the textbook. You may follow the Control Unit design presented in the Section 4.4 and in the Appendix C.
2. Integrate all the required modules from A1 and A2 and the Control Unit to create a working RISC-V datapth. A random list of instructions tasking every part of the datapath can be stored inside the IM by the testbench. On reset, the datapath of the processor should fetch, decode, execute, memory access and write back the first instruction. This sequence should repeat indefinitely or until an exit instruction is encountered (define your own, if necessary). Assume any other info required to get the datapath working. The datapath should implement the subset discussed in the class (and shown in the Textbook in Section 4.3). The Block diagram of the final Datapath + Control Unit is in Fig. 4.17 (Page 257) of the textbook.