

1. Consider the 5-stage MIPS pipeline. Write both versions of the pipeline timing diagram (shown in the class) for the following code sequence. What is the CPI? For CPI, ignore the startup period (the first cycle is when the first commit happens).

sub \$2, \$1, \$3
and \$12, \$2, \$5
or \$13, \$6, \$2
add \$14, \$2, \$2
sw \$15, 100(\$2)

2. Consider the 5-stage MIPS pipeline. a. Write the pipeline timing diagram for the following 3rd iteration of the following loop. Show all instructions that are in the pipeline during these cycles (not just those from the 3rd iteration). Assume that, when required, the pipeline stalls in the ID stage to read the latest value of an input operand. b. What is the CPI of the instructions sequence from this iteration?

Loop: LD R1, 0(R2)
ADDI R1, R1, 1
SW R1, 0(R2)
ADDI R2, R2, 4
SUB R3, R3, 1
BNEZ R3, LOOP

Rough Work