1. Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. Th e following data constitutes a stream of virtual addresses as seen on a system. Assume 4 KiB pages, a 4-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

4669, 2227, 13916, 34587, 48870, 12608, 49225

a. Given the address stream shown, and the initial TLB and page table states provided above, show the fi nal state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault.

TLB

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

Page table

Valid	**Physical Page or in Disk**
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

b. Repeat 1.a using 16 KiB pages instead of 4 KiB pages. What would be some of the advantages of having a larger page size? What are some of the disadvantages?

c. Show the final contents of the TLB if it is 2-way set associative. There are several parameters that impact the overall size of the page table. Listed are key page table parameters.

Virtual Address Size	Page Size	Page Table Entry Size
32 bits	8 KiB	4 bytes

d. Given the parameters shown above, calculate the total page table size for a system running 5 applications that utilize half of the memory available.

Rough Work