CO262. Tutorial 3.	16 – Feb – 2018
1. Consider a 128KB DM cache with 64B cache lines using a 32b address. In the address: 0xDEADBE binary values of the Tag, Index and Block offset fields?	AD, what are the

2. Assume a fully associative write-back cache with many cache entries that starts empty. Below is a sequence of five memory operations (the address is in square brackets): What are the number of hits and misses when using no-write allocate versus write allocate?

Write Allocate		Write No-Allocate	Write No-Allocate	
Memory Ops	Hit/Miss (H/M)	Memory Ops	Hit/Miss (H/M)	
Write Mem[100] Write Mem[100]; Read Mem[200]; Write Mem[200]; Write Mem[100];		Write Mem[100] Write Mem[100]; Read Mem[200]; Write Mem[200]; Write Mem[100];		

3. The adjoining code is running on systems with the following configurations:

C1: 32KB, 32B block, 2-way SA cache.

C2: 32KB, 64B block, DM cache.

Starting addresses of A, and B are 0xA000, and 0xB000 respectively.

a. List the data memory references.

b. What are the hit rates on both the configurations? Suggest ways to improve hit rates on both of them.

double A[2048], B[2048], sum=0.0; for (i=0; i<2048, i++) sum = sum +A[i] \* B[i];



Rough Work