CO262 - System Programming (3:0:0) 3

Dec 2017 – May 2018

Course Objectives

1. Define concepts in Architecture and Organization that build on the fundamental design principles.
2. Demonstrate the interactions between the processor pipeline and functional correctness of the executing code, and the use of various current and future memory technologies.
3. Introduce the concept of parallelism, the hardware support required to execute parallel programs, various flavours of parallelism that exist in today's computing machines.
4. Illustrate the various design parameters of small and large Interconnection networks in today's computing systems.

Course Outcomes (What the learner knows and is able to do as a result of learning this course)

1. Identify dependences in the code, possible hazards in the pipeline, and solutions in the processor pipeline to overcome them.
2. Compare and contrast various memory technologies, understand the tradeoffs involved in their usage.
3. Understand the ISA support for synchronization primitives in modern processors, write shared memory parallel, and message passing parallel programs. Write vectorized programs.
4. Understand the architecture of cloud systems and its interaction with client systems and the architectural tradeoffs.

Table: Course Coverage

Module Title	Module Contents
M1 - Processor	Pipelining, Hazards, Forwarding, Branch Prediction.
	PH5e. Sections 4.5 - 4.11
M2 - Memory Systems	Memory hierarchy, SRAM, Cache Blocking, Cache coherence, DRAM, Virtual Machines, Virtual Memory, Non-Volatile Memory, RAID, Persistent NVMs
	PH5e. Chapter 5. Published literature.
M3 – Input Output	Connecting and interfacing I/O devices. Memory mapped I/O, Interrupt driven I/O. DMA. Secondary storage.
	PH4e: Sections 6.1 – 6.9.
M4 – Parallelism	Concept of Parallelism, ISA support for synchronization, Flynn's Classification, Vector Processing, Multithreading, Shared Memory and Message passing multiprocessors, Heterogeneous Computing, Clusters, Warehouse computing.
	PH5e. Sections 2.11, 6.1 – 6.7.
M5 - Interconnection Networks	Topologies – architecturs and properties, Router Architecture, Flow control, Link design, Simulation.
	PH5e. Section 6.8, Published literature.

Reference Texts

1. **[PH5e/PH6e] David A Patterson and John L Hennessy. Computer Organization and Design – The Hardware/Software Interface. Elsevier.(5e, 2014 – MIPS edition or the 6e, 2017 RISC-V edition).**

2. [PH5e] David A Patterson and John L Hennessy. Computer Organization and Design – The Hardware/Software Interface. 5e. Elsevier. 2014. (This is the MIPS edition book).
3. [PH4e] David A Patterson and John L Hennessy. Computer Organization and Design – The Hardware/Software Interface. 4e. Elsevier. 2012. (The ARM edition is available in the Library).
4. M. Morris Mano. Computer System Architecture. 3e. Pearson. 2007.

Related NPTEL Courses (http://www.nptel.ac.in):

- Matthew Jacob – High Performance Computing
- Bhaskaran Raman – Computer Organisation and Architecture
- S. Raman – Computer Organization
- Jatindra Kumar Deka – Computer Organisation and Architecture.

Course Evaluation (Tentative): Tutorials and Assignments – 30%, Quizzes – 10%, Midterm – 20%, Endsem – 40%.