CO262. Tutorial 6. 5 – April – 2018

1. Consider an SMP with 3 CPUs : A, B, and C with a write back, write invalidate MSI Cache coherence protocol Cache. For each of the events, write the sharing state of cache blocks X and Y. Note: The caches are Direct Mapped and X and Y map to the same cache block.

Event	State in A	State in B	State in C
A: Rd X			
B: Rd X			
C: Rd X			
A: Wr X			
A: Wr X			
C: Wr X			
B: Rd X			
A: Rd X			
A: Rd Y			
B: Wr X			
B: Rd Y			
B: Wr X			
B: Wr Y			

2. Consider a 3 node Distributed Shared Memory Multiprocessor system with a MSI Directory based cache coherence protocol. What are the steps and the corresponding Directory states for the following events involving location X. Assume that X resides in node A's local memory.
Initial State: Entry for X in D_A: S: A, B

(P.T.O.)

Event 1. A: Write X

Event 2. C: Write X

Event 3. B. Read X

Event 4. A. Write X

Rough Work