CO262. Tutorial 5. 23 – March – 2018

1. Assume that for a given program 70% of the executed instructions are arithmetic, 10% are load/store, and 20% are branch.
a. Given this instruction mix and the assumption that an arithmetic instruction requires 2 cycles, a load/store instruction takes 6 cycles, and a branch instruction takes 3 cycles, fi nd the average CPI.

b. For a 25% improvement in performance, how many cycles, on average, may an arithmetic instruction take if load/store and branch instructions are not improved at all?

c. For a 50% improvement in performance, how many cycles, on average, may an arithmetic instruction take if load/store and branch instructions are not improved at all?

2. Answer questions related to the SSE2 code shown below.

```
1. #include <x86intrin.h>
2. void dgemm (int n, double* A, double* B, double* C)
3. {
4.  for ( int i = 0; i < n; i+=4 )
5.  for ( int j = 0; j < n; j++ ) {
6.    __m256d c0 = _mm256_load_pd(C+i+j*n);
7.  for( int k = 0; k < n; k++ )
8.   c0 = _mm256_add_pd(c0, /*c0+= A[i][k]*B[k][j]*/
9.   _mm256_mul_pd(_mm256_load_pd(A+i+k*n),
10.  _mm256_broadcast_sd(B+k+j*n)));
11.  _mm256_store_pd(C+i+j*n, c0); /* C[i][j] = c0 */
12. }
13.}
```

a. Size of the SSE2 SIMD register in bytes is: _____. What is the datatype?

b. What are the inputs and return values of the SSE2 API used in the code?

Function call	Input parameters	Return value
`_mm256_load_pd`		
`_mm256_load_pd`		
`_mm256_broadcast_sd`		
`_mm256_store_pd`		

c. Which elements from the input arrays (A and B) and the output arrays (C) are being accessed/modified/ in the second iteration of the outermost loop (i loop). Show the full set of operations in simple arithmetic form. You may use $A_{1,1}$ or A[1][1] notations to represent the corresponding elements from the arrays.

Rough Work