Voltage controlled low barrier nanomagnets for probabilistic bits

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by

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Certificate

This is to certify that the thesis titled **Voltage controlled low barrier nanomagnets for probabilistic bits** being submitted by **Abhinav Reddy Oruganti** for the award of **Bachelor of Technology** in **Electrical Engineering** is a record of bona fide work carried out by him under my guidance and supervision at the **Department of Electrical Engineering**. The work presented in this thesis has not been submitted elsewhere either in part or full, for the award of any other degree or diploma.

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Abstract

Low energy barrier nanomagnets (LBMs) are tiny magnetic structures that have recently garnered significant attention for their potential to perform computational tasks more efficiently than conventional bits. Despite their inherent instability, researchers have explored ways to use these unstable nano-magnets as probabilistic bits (p-bits), similar to conventional digital bits. It is demonstrated that current can be used to switch the magnetization of the nanomagnet by 180^o, but due to energy losses, voltage is proposed to be used instead. The variation in the VCMA strategy is being observed and the importance of pulse-width and voltage is being discussed. As the aspect ratio increases, the critical rise-time decreases for both the CoFeB and PMN-PT structures. The energy consumption of these structures is noted to be different, with varying trends. Analogous to CMOS circuitry, the rise time variation with other factors, such as Aspect Ratio and Magnetoresistance, is also being discussed. The analogy to CMOS circuitry is particularly noteworthy, as it highlights the potential of LBMs to be integrated into traditional computing architectures, opening up a new avenue for high-performance computing.

Acknowledgments

We take this opportunity to express our gratitude to our mentor and advisor **Professor Dhiman Mallick**, whose support and guidance have been invaluable to us during this whole project. His suggestions have helped us think of creative and different approaches towards the problems we faced during our research and come up with various ways to solve those problems. Furthermore, we are grateful to **Mr. Pankaj Pathak, PhD Scholar**, for providing us with the right direction and assistance throughout the project. We also would like to thank the Electrical Engineering Department of IIT Delhi to give us the opportunity to do this research work in the incredible field of Nanomagnetic Devices.

Abhinav Reddy Oruganti

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Chapter 1

Introduction

1.1 Motivation

In traditional semiconductor-based logic and nanomagnet-based memory devices, stable and predictable units, such as standard MOS transistors or nanomagnets with energy barriers greater than approximately 40-60 kT, are utilized. Low energy barrier nanomagnets(LBMs), also referred to as p-bits, are comparable to memory cells employed in traditional memory technologies[2]. The potential utility of p-bits in diverse applications inspires us to investigate their properties. They provide a highly energy-efficient solution to probabilistic computing by storing information in the magnetization states of LBMs. These p-bits can be used to address some of the problems that require quantum computing. Furthermore, they can be utilized as binary stochastic neurons in stochastic machine learning, and in arrays to generate random numbers. P-bits are highly energy-efficient and have demonstrated superior performance for specific tasks such as combinatorial optimization, invertible logic, and integer factorization. In the present research, voltage sources are utilized to operate unstable nanomagnets instead of current sources, which were previously found to result in energy loss. In this project, we discuss LBMs of various structures, including CoFeB and PMN-PT, which are used in modeling of LBMs.

1.2 Roadmap

In Chapter 2 of our project, we discuss necessary contextual information and models that are using in the work. In Chapter 3-4 we discuss the modelling and various characterises of the unstable nanomagnets and VCMA(Voltage Controlled Magnetic Anisotropy). In Chapter 5, we conclude the thesis with summary and future work.

Chapter 2

Literature Review

2.1 Introduction

In this chapter, the model of the nanomagnetic structure is being discussed, the equations it follows are being explained, and its working is being described.

2.2 The Model

Simulations have been implemented on unstable nano-magnets in our research. The thickness of these nano-magnets is less than the critical thickness of 2nm-6nm, as noted in [3].

Since unstable nanomagnets, such as p-bits, have a tendency to oscillate between the two states representing 0 and 1, it can be difficult to maintain their stability.The magnetization states of LBMs at room temperature when spin-polarized current is injected perpendicular to the plane of the LBM are studied using stochastic Landau-Lifshitz-Gilbert equation (sLLG). The sLLG equation is employed due to the random fluctuations between 0 and 1 exhibited by p-bits.

The magnetization of a circular nanomagnet when subjected to a field $\vec{H_i}$ is $\hat{m_i}$ is obtained from the stochastic Landau-Lifshitz-Gilbert equation:

$$\frac{d\vec{m}(t)}{dt} = -\gamma\vec{m}(t)\vec{H}_{total} + \alpha\left(\vec{m}(t)\frac{d\vec{m}(t)}{dt}\right) + a\vec{m}(t)\times\left(\frac{\eta\bar{I_s}(t)\mu B}{qM_s\Omega}\times\vec{m}(t)\right) + b\frac{\eta\bar{I_s}(t)\mu_B}{qM_s\Omega}\times\vec{m}(t) \tag{2.1}$$

$$\hat{m}(t) = m_x(t)\hat{x} + m_y(t)\hat{y} + m_z(t)\hat{z}\ [m_x^2 + m_y^2 + m_z^2 + = 1] \tag{2.2}$$

$$\vec{H}_{total} = \vec{H}_{demag} + \vec{H}_{thermal} \tag{2.3}$$

$$\vec{H}_{demag} = -M_sN_{d-xx}m_x(t)\hat{x} - M_sN_{d-yy}m_y(t)\hat{y} - M_sN_{d-zz}m_z(t)\hat{z} \tag{2.4}$$

$$\vec{H}_{thermal} = \sqrt{\frac{2\alpha kT}{\gamma(1+\alpha^2)\mu_0 M_s \Omega(\Delta t)}} \left[G^x(0,1)(t)\hat{x} + G^y_{(0,1)}(t)\hat{y} + G^z_{(0,1)}(t)\hat{z}\right]$$

(2.5)

An elliptical nanomagnet (PMN-PT structure) with default dimensions of a=100nm and b=80nm is being considered, and simulations are being conducted to incorporate the sLLG equations in the models used to record the magnetization state.

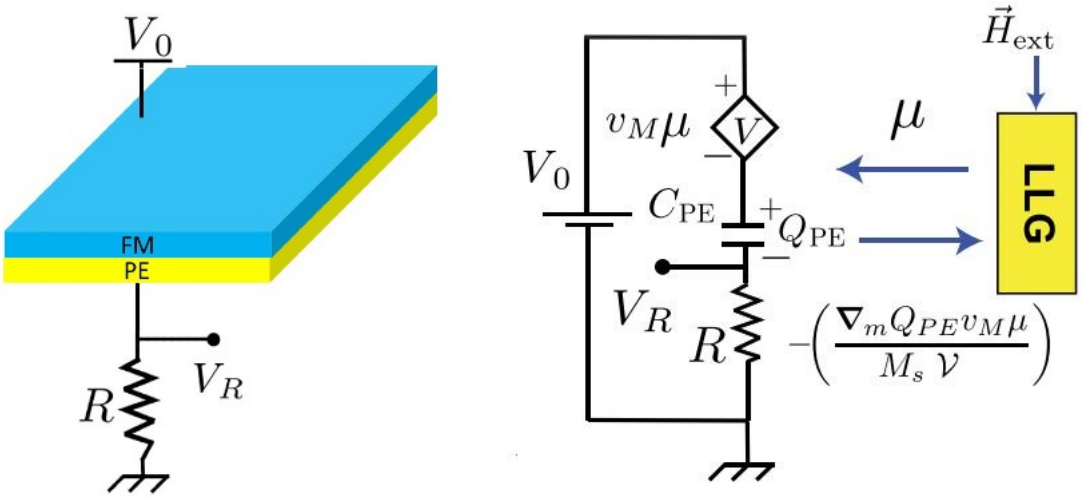


Figure 2.1: Equivalent circuit for ME read and write operations.

$$V_{in} = \frac{Q}{C} + R\frac{dQ}{dt} + \frac{\partial E_m}{\partial Q} \tag{2.6}$$

The above PMN-PT structure was used from the [5]. In the following way, the equivalent circuit model is explained. An assumption is made that a charge is flowing at t=0 and the capacitor is instantaneously charged. Then, the sLLG equations are solved at that instant and the magnetization state is returned in terms of the voltage-controlled voltage source. The simulation runs for a specific period of time (in nanoseconds) and records the magnetization state or plot.

2.3 Conclusion

In this chapter, the importance of employing p-bits as memory devices and the models inscribed in the paper are being discussed. The sLLG equations are being solved concurrently to produce the magnetization state at that time. In the following chapter, the models that were previously discussed will be employed to record the magnetization state when subjected to various characteristics, like variable pulse-widtn and voltage of a square-pulse.

Chapter 3

Voltage Controlled Magnetic Anisotropy

3.1 Introduction

The significance of the input pulse voltage and width of the nanomagnetic device when using VCMA strategy with Spin-Hall effect is being discussed in this chapter. Additionally, the initial model of the structure with PMN-PT (lead magnesium niobate-lead titanate) and its corresponding results are being presented.

3.2 PMN-PT structure

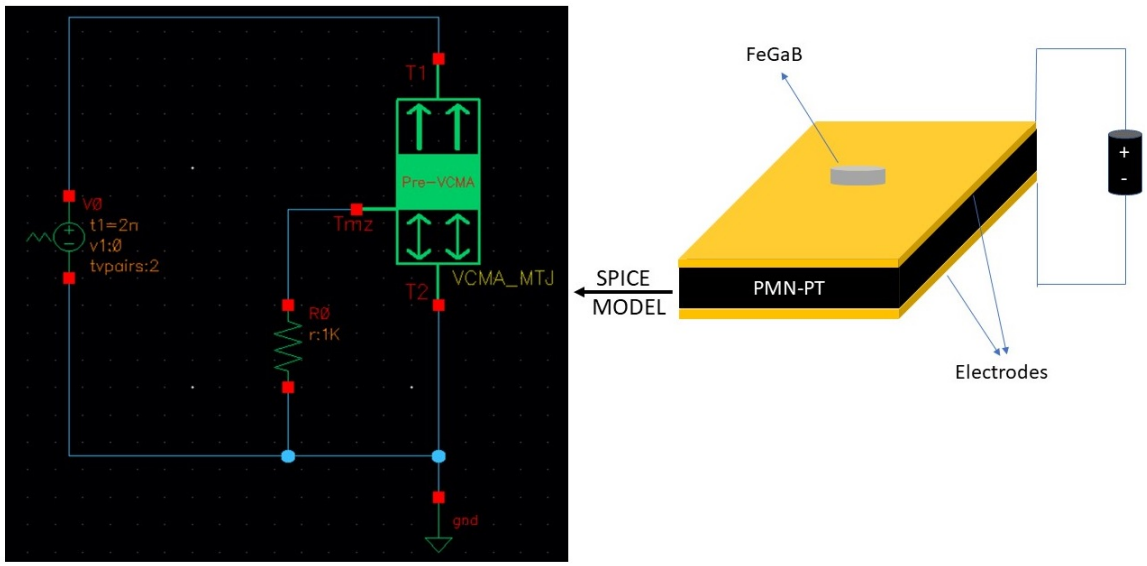


Figure 3.1: It is recognized that the structure requires a 3rd terminal to save the magnetization state (m_z). It has been proposed to use the SPICE Model from [1] and to vary the appropriate environments.

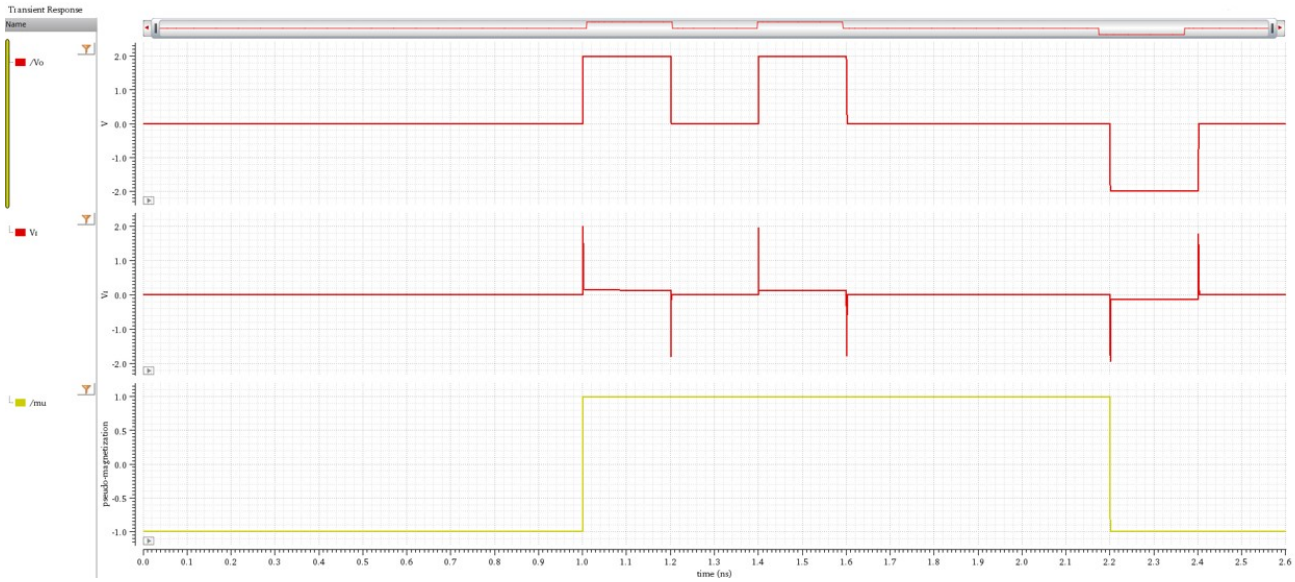


Figure 3.2: In our experiments, voltage pulses were applied as the input to the aforementioned structure. And the appropriate voltage across the resistor V_r, and magnetization state of the unstable-nanomagnet

It was observed that the pseudo-magnetization remains the same when a positive pulse is applied twice, since it is already present in the state. Additionally, the voltage across resistance (V_r) shows a sudden change to the maximum input voltage of 2V during the second input pulse. As expected, a magnetization switch from -1 to 1 was observed during the first positive voltage pulse, and a reverse switch from 1 to -1 occurred during the negative voltage pulse.

Incorporating SHE (Spin-Hall Effect) in the above schematic is proposed. The spin Hall effect is expected to offer a more localized and controllable approach for modifying the magnetic anisotropy energy, which in turn can potentially reduce the voltage required to switch the magnetization state of the magnetic layer.

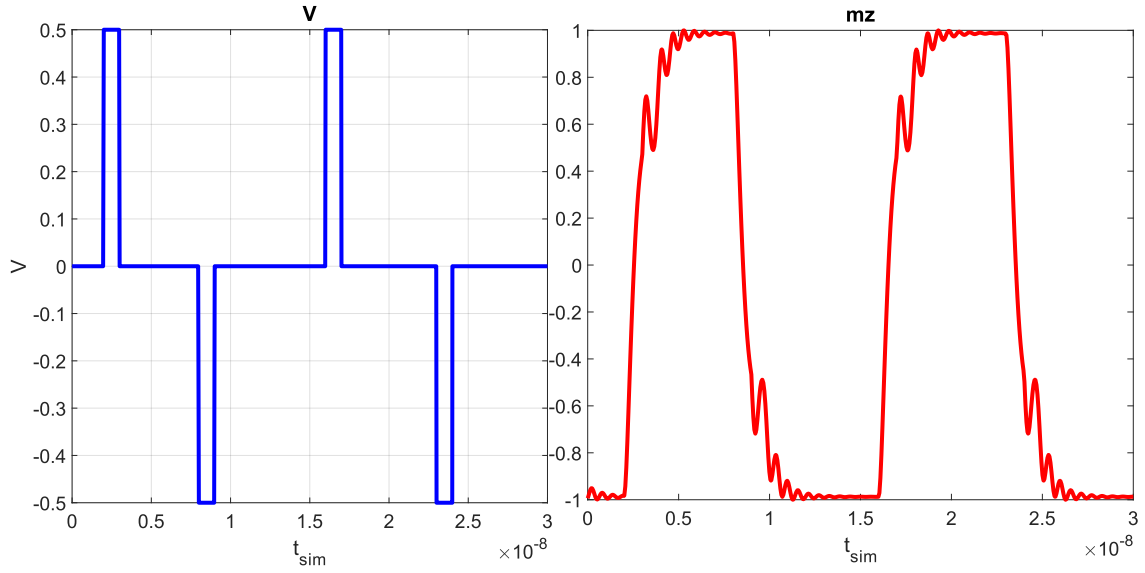


Figure 3.3: After incorporating SHE, the expected magnetization switching behavior in the previous structure is observed. SHE is added to study the behavior of the structure under different voltage pulse widths and magnitudes.

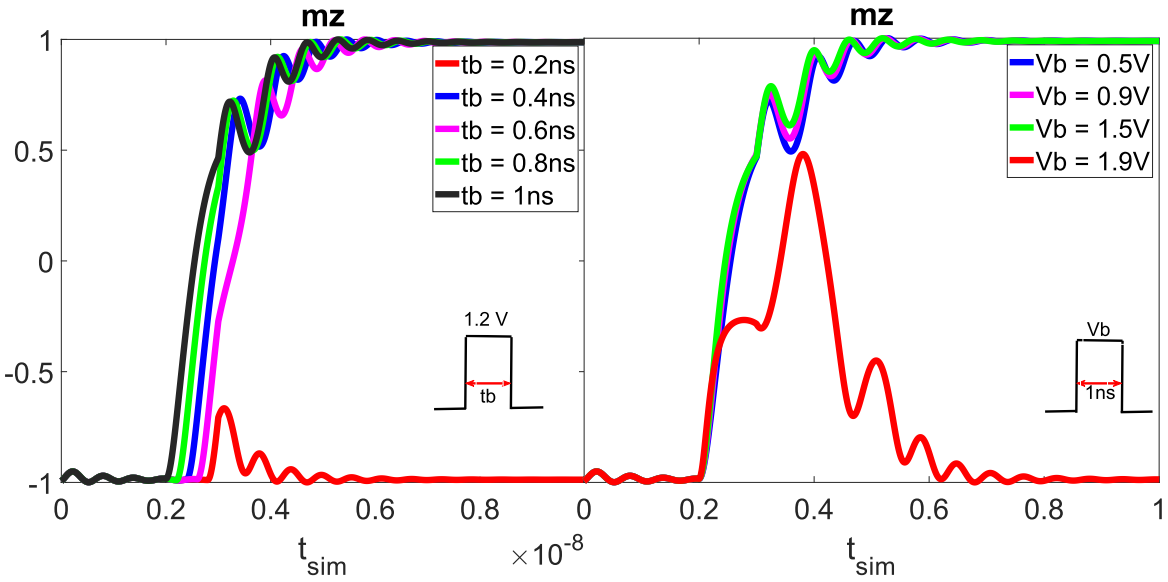


Figure 3.4: It is observed that, for the aspect ratio of 100:80, the critical voltage for magnetization switching is reached as the voltage is varied for a fixed pulse width. Similarly, for a fixed voltage, the critical width is reached as the pulse width is varied.

Upon observation, we find that decreasing the voltage width to a certain point for the chosen aspect ratio leads to an inability to switch the magnetization. In Fig 3.4(a), we observe that at tb = 0.2ns, the switching is not feasible. Hence, we conclude that a critical pulse width is required for a fixed voltage, indicating that the voltage must be applied across the device for a sufficient period to enable switching. Similarly, by maintaining a constant pulse width, as voltage is altered, there is a maximum voltage beyond which switching is not achievable. The previous explanation of requiring the voltage for a fixed period can also be applied here. It is observed that a critical pulse width is required to induce magnetization change. Additionally, it is deduced that the technique becomes ineffective after surpassing a critical voltage for a given width.

3.3 Conclusion

In this chapter, we discuss voltage switching when the polarity of the pulse is changed from positive to negative. We also had discussed the importance of proper selection of voltage pulse amplitude and duration for successful implementation of the VCMA strategy. The next chapter delves into the significance of rise-time and fall time in the provided voltage.

Chapter 4

Results

4.1 Introduction

In this Chapter, we discuss the importance of rise-time in CMOS circuitary and investigate the effect of critical rise-time(the minimum rise-time required for switching) varying the parameters of the nanomagnetic device.

The investigation of the rise time necessary for simulations when applying voltages or electric fields is proposed. Although this is of high significance in the CMOS circuitry that is widely used for memory devices, it is expected to also be an extremely important aspect in nanomagnetic devices.

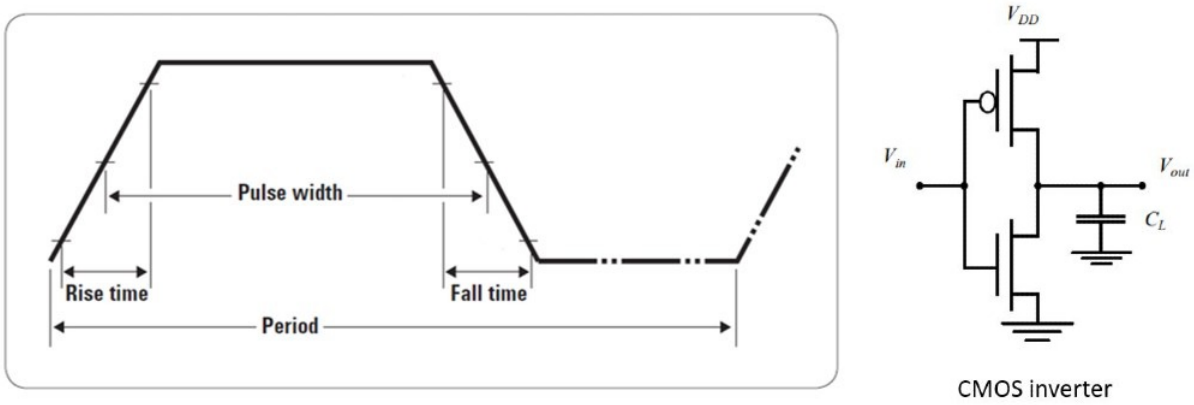


Figure 4.1: a) Rise time refers to the amount of time it takes for a signal to transition from a low voltage level to a high voltage level. Fall time refers to the amount of time it takes for a signal to transition from a high voltage level to a low voltage level. b) Every technology, that is used in circuitry has a critical rise time. For example, in CMOS inverter driving a C_L load capacitor the critical rise time is defined as $t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}}$

As the rise time component plays a crucial role in the memory cells of CMOS devices, it is equally significant in the nanomagnetic structures being used. The dependence of the **critical rise-time** is discussed in this chapter.

4.2 Impact of rise-time on aspect ratios

In the figure presented below, it is observed that an increase in aspect ratio from 1:1 to 1:1.8 results in faster switching, with the exception of the 1:1 circular structure that has four easy axes. Additionally, based on the simulations, we propose a new theory that the bit state reaches 1 when the magnetization reaches 0.8. Further observations suggest that an increase in aspect ratio leads to faster switching.

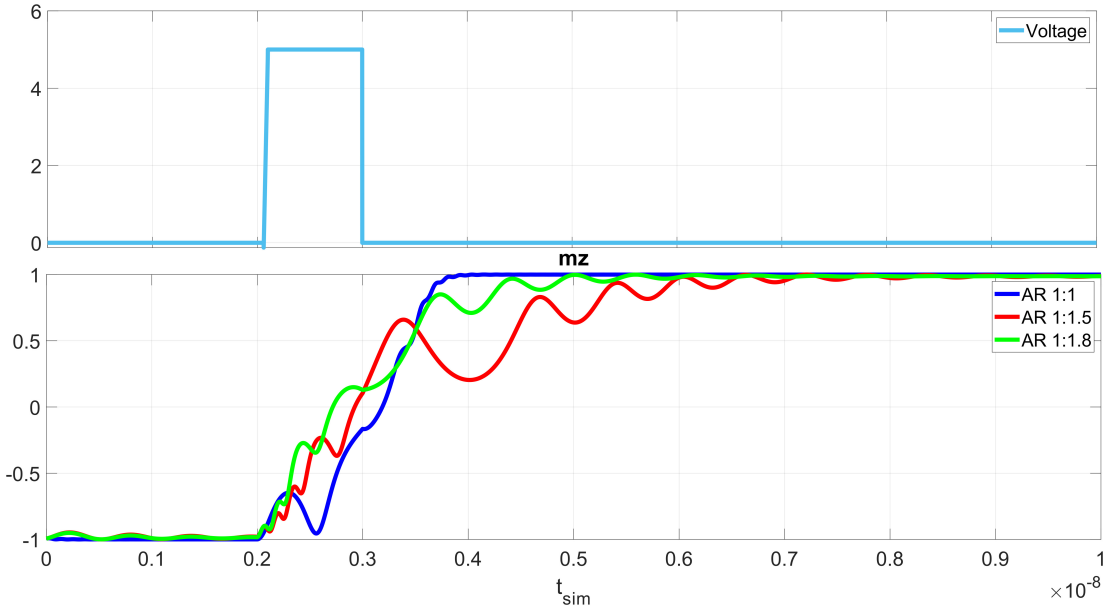


Figure 4.2: The magnetization states of different aspect ratios are being studied for a voltage of 5V, with a rise-time of 100ps. It is observed that for an aspect ratio of 1:1.2, the magnetization switches from -1 to 1 after 0.2ns, and for an aspect ratio of 1:1.4, it switches at 0.16ns. Similarly, for aspect ratios of 1:1.6 and 1:1.8, the switching times are 0.14ns and 0.12ns, respectively. It can be concluded that as the aspect ratio increases, the switching time decreases, indicating faster switching for larger aspect ratios.

It is also observed that with the decrease in the size of the magnetic system, the net magnetic anisotropic energy density increases, leading to higher energy barriers, which can result in slower switching probabilities. On the other hand, larger aspect ratios tend to exhibit faster switching probabilities due to their decreased energy barriers.

$$E_b = (K_{anis} - K_{demag}) = K_{eff} v; \tag{4.1}$$

where v is volume of the nanomagnet K_{anis} and K_{demag} are net anisotropy energy and demagnetization energy respectively [3].

The experimental results agree with the theoretical predictions conducted previously. [**?**]

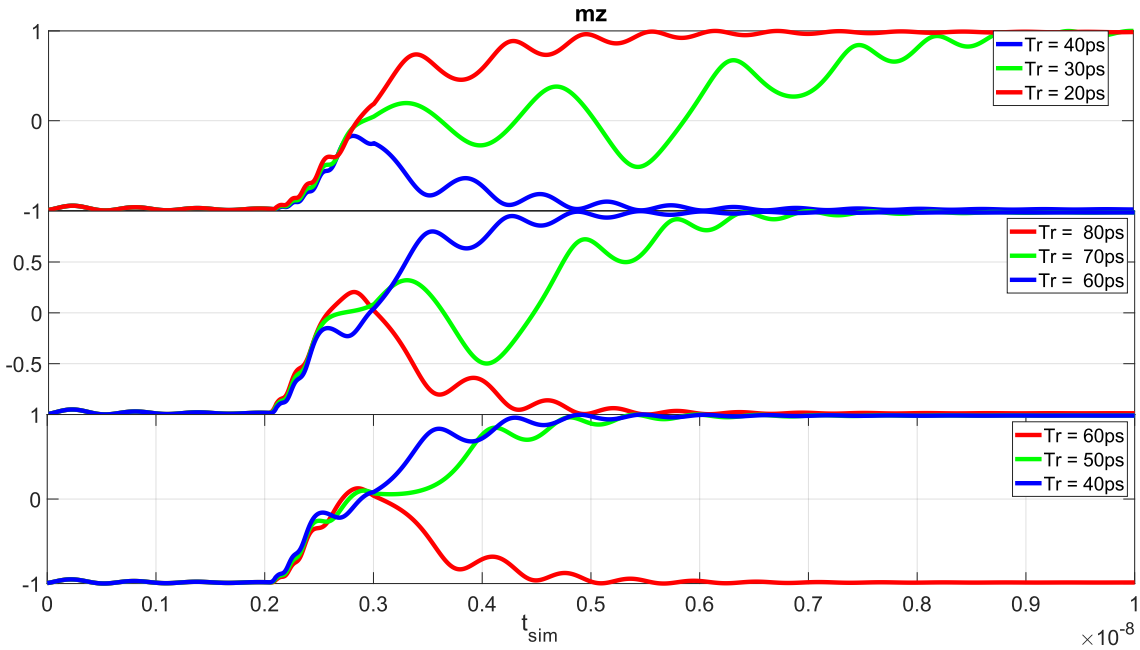
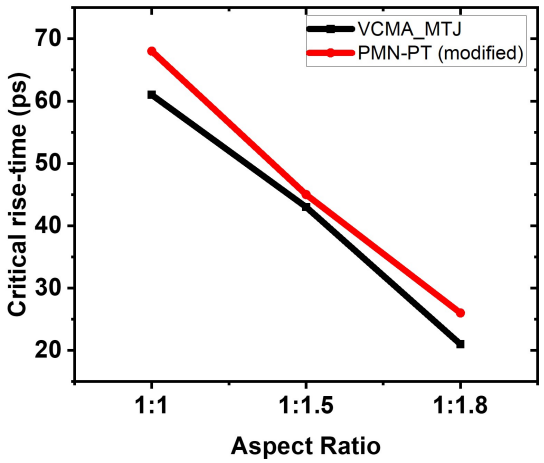
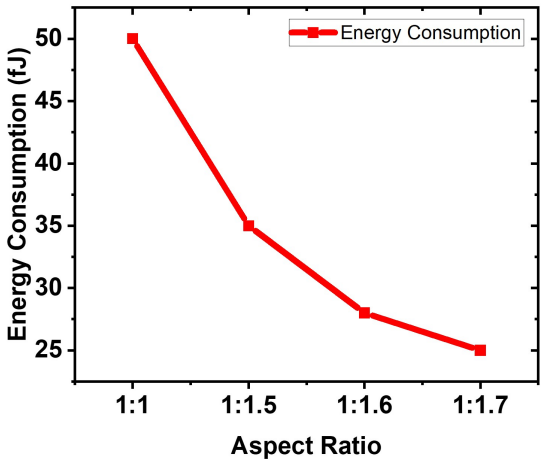


Figure 4.3: For different aspect ratios, we observe that the critical rise-time varies and increasing the rise-time beyond a certain point leads to failure in switching.Similar to the CMOS circuitry, low rise-time is preferred in the nanomagnetic devices as well to minimize power consumption. High rise-time results in greater energy dissipation, which can potentially damage the device. Therefore, it is crucial to optimize the rise-time for efficient operation of the device.

It has been observed from our simulations that the critical rise time of nanomagnets is influenced by their aspect ratios, which is consistent with our theoretical predictions. Our findings reveal that the critical rise time decreases as the aspect ratio increases. We are currently exploring the impact of other parameters on the rise time, with the objective of creating a formula that can predict the rise time for unstable nanomagnets.

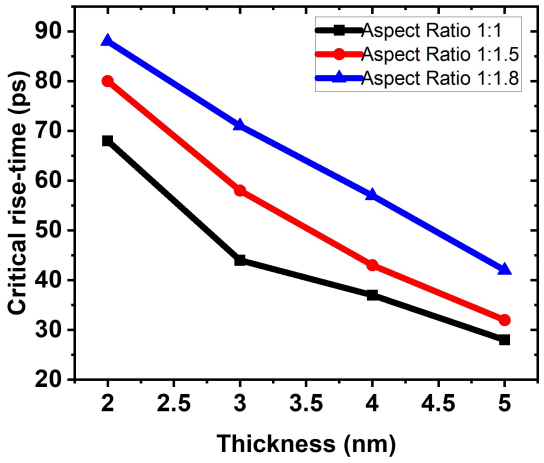
A similar trend is observed, in the below figure, as the aspect ratio is increased for the different structures, and it is found that the trend remains almost the same. Hence, we propose to normalize that for different structures, as the aspect ratio is increased, the critical rise-time decreases.

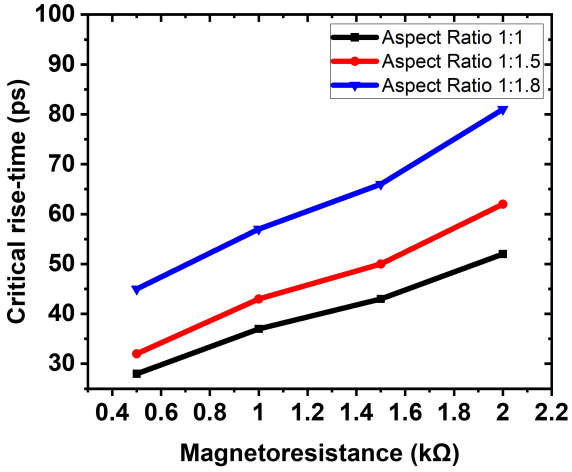




(a) Critical rise-time variation for two different structures(b) Varitaion of Energy Consumption with differnt Aspect
VCMA-MTJ(CoFeB structure) and PMN-PT(Lead Mag-Ratios
nesium Niobate-Lead Titanate).

Figure 4.4: In Fig 4.4 a), it is observed that the trend of critical-rise time with aspect ratios is similar for various structures. 4.4b) The energy consumption decreases with an increase in aspect ratio.





(a) Critical rise-time variation for different thicknesses (b) Critical rise-time variation for different Magnetoresistance.

Figure 4.5: The dependence of critical rise-time on Magnetoresistance and Thickness is illustrated in figures a) and b). It is observed that the critical rise-time decreases as the thickness is increased for a given aspect ratio. This trend is observed for other aspect ratios as well. Additionally, as the Magnetoresistance is increased, the critical rise-time also increases.

A similarity to the CMOS model that was discussed in the beginning of this chapter is observed. It was found that for a CMOS inverter, the typical rise-time is proportional to C_L, and a similar trend is observed in this particular Magnetoresistance as well.This point is noted as extremely important, and further investigations on potential similarities are being conducted.

4.3 Conclusion

In this chapter, the importance of rise-time and its similarity to CMOS circuitry is being discussed. It is observed that the rise time is directly proportional to the magnetoresistance in the structure used, similar to that of CMOS inverter where it feeds a of C_L the rise time is proportional to C_L. The variation of critical rise-time with different aspect ratios is also discussed and normalized for various structures. The next chapter concludes the topics covered in this paper and discusses the scope for future work. The wording is in present tense and it is about the subject matter.

Parameters	Values
Saturation magnetization (M_s)	$0.978 \cdot 10^6$
Gilbert damping α)	0.07
Temperature (T)	300K
Major axis (a1)	100 nm
Minor axis (a2)	80 nm
Thickness (a3)	2nm, 3nm, 4nm and 5nm

Table 4.1: Parameters used in the simulations

Chapter 5

Conclusions

Simulations have been performed on unstable nanomagnets with a thickness below the critical thickness, with the goal of developing p-bits for energy-efficient devices. The choice of elliptical devices over circular devices was made due to the presence of two easy axes in circular devices, compared to the single easy axis in elliptical devices, which can be designated as 0 or 1. The focus was shifted from current to voltage due to the energy losses incurred [4].

The research has provided insight into the key factors that must be considered when using the VCMA strategy on unstable nanomagnets. Specifically, the critical pulse width and voltage for each aspect ratio have been identified as essential parameters. Furthermore, the importance of rise-time and fall-time has been emphasized, and their analogous nature has led to interesting results. As a result, future device models must take these factors into account to ensure optimal performance. Overall, this research is expected to inform and benefit future studies in the field.

5.1 Scope for Future Work:

For future work, various voltage sources that are more efficient than applying voltage or electric field can be explored. One can also attempt to emulate newer sources and optimize them to observe the behavior of the nano-magnet more clearly and identify corner cases where it fails to work. A comparison of similarities to CMOS memory cells must be made at all times to ensure that we are moving in the right direction of research. The theoretical work presented in this project indicates that the proposed novel ME memory device is feasible and can be integrated into future energy-efficient devices. There is still much more research to be done on this interesting phenomenon, and it will continue to be a topic of interest in the future.

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