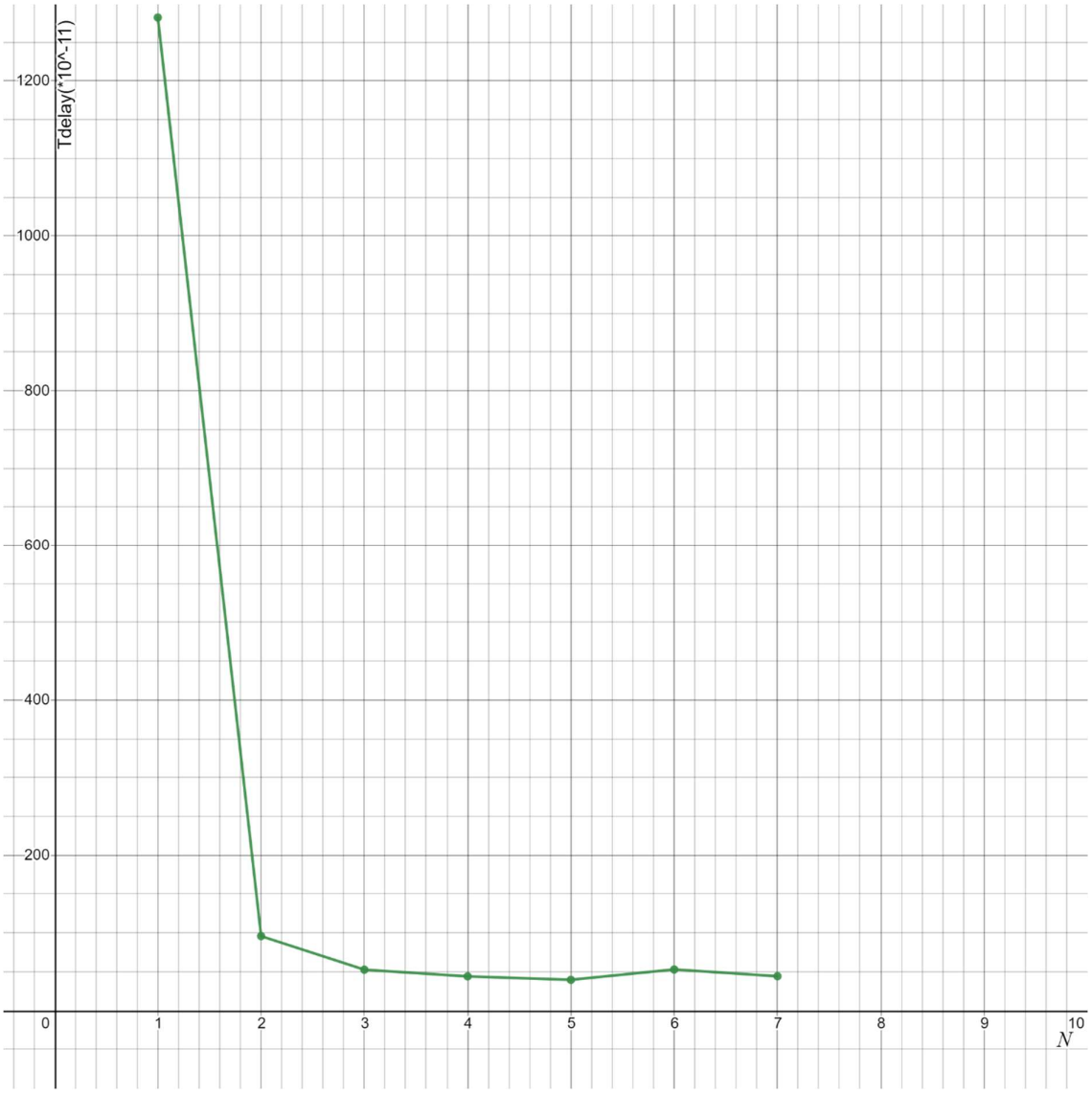
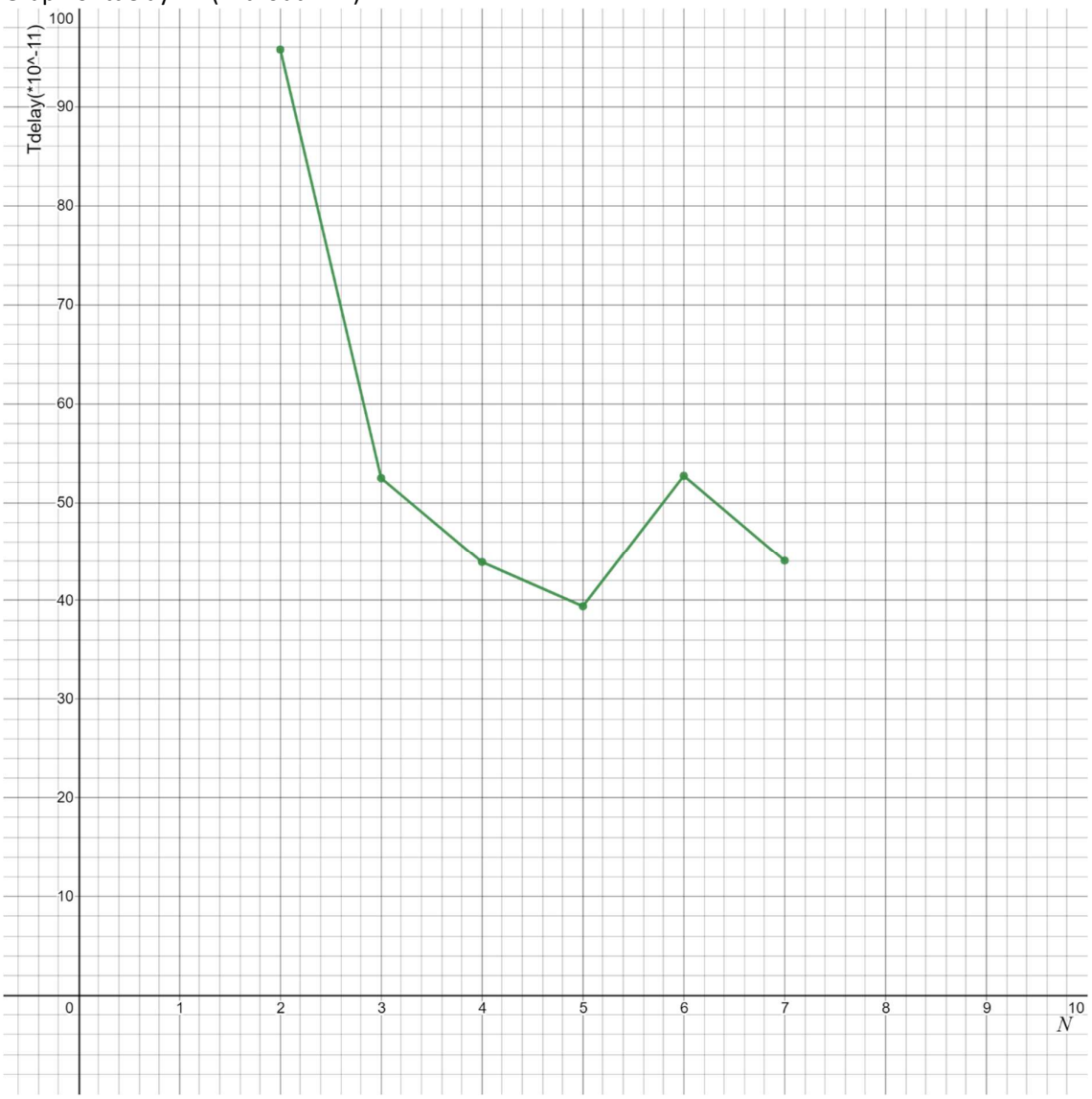
N=1	Tdelay = 1281.97005e-11
N=2	Tdelay = 95.787e-11
N=3	Tdelay = 52.47417e-11
N=4	Tdelay = 43.907485e-11
N=5	Tdelay = 39.41269e-11
N=6	Tdelay = 52.699935e-11
N=7	Tdelay = 44.05574e-11

Graph of tdelay vs N



Graph of tdelay v N(without N=1)



We can see that for N=5(5 inverters) the delay is minimum, which is optimum.

Appendix

*----------

ngSpice Netlist code

N=1

* CMOS Chain Inverter simulation

```
.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends

*N=1
x1 1 2 vdd 0 cinv  m=1
x2 2 3 vdd 0 cinv m=1024



vdd VDD 0 1.8
vin 1 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(1) val=0.9 rise=1 targ v(2) val=0.9 fall=1
meas tran tfall trig v(1) val=0.9 fall=1 targ v(2) val=0.9 rise=1
let tp = 0.5*(trise+tfall)

.endc
*--------------------------------------------------------------------------------------------------------------------------------
N=2

* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
```

```
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends

*N=2
x3 4 5 vdd 0 cinv  m=1
x4 5 6  vdd 0 cinv m=32
x5 6 7 vdd 0 cinv m=1024



vdd VDD 0 1.8
vin 4 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(4) val=0.9 rise=1 targ v(6) val=0.9 rise=1
meas tran tfall trig v(4) val=0.9 fall=1 targ v(6) val=0.9 fall=1
let tp = 0.5*(trise+tfall)

.endc
*--------------------------------------------------------------------------------------------------------------------------------
N=3
* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends
```

```
*N=3
x6 8 9 vdd 0 cinv  m=1
x7 9 10 vdd 0 cinv m=10.0793684
x8 10 11 vdd 0 cinv m=101.5936673
x9 11 12 vdd 0 cinv m=1024

vdd VDD 0 1.8
vin 8 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(8) val=0.9 rise=1 targ v(11) val=0.9 fall=1
meas tran tfall trig v(9) val=0.9 fall=1 targ v(11) val=0.9 rise=1
let tp = 0.5*(trise+tfall)

.endc

*--------------------------------------------------------------------------------------------------------------------------
N=4

* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends
```

```
*N=4
x10 13 14 vdd 0 cinv  m=1
x11 14 15 vdd 0 cinv m=5.656854249
x12 15 16 vdd 0 cinv m=32
x13 16 17 vdd 0 cinv m=181.019336
x14 17 18 vdd 0 cinv m=1024

vdd VDD 0 1.8
vin 13 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(13) val=0.9 rise=1 targ v(17) val=0.9 rise=1
meas tran tfall trig v(13) val=0.9 fall=1 targ v(17) val=0.9 fall=1
let tp = 0.5*(trise+tfall)

.endc
*--------------------------------------------------------------------------------------------------------------------------------
N=5

* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends

*N=5
```

```
x15 19 20 vdd 0 cinv m=1
x16 20 21 vdd 0 cinv  m=4
x17 21 22 vdd 0 cinv m=16
x18 22 23 vdd 0 cinv m=64
x19 23 24 vdd 0 cinv m=256
x20 24 25 vdd 0 cinv m=1024

vdd VDD 0 1.8
vin 19 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(19) val=0.9 rise=1 targ v(24) val=0.9 fall=1
meas tran tfall trig v(19) val=0.9 fall=1 targ v(24) val=0.9 rise=1
let tp = 0.5*(trise+tfall)

.endc
*--------------------------------------------------------------------------------------------------------------------------
N=6

* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends

*N=6
```

```
x21 26 27 vdd 0 cinv  m=1
x22 27 28 vdd 0 cinv m= 3.174802104
x23 28 29 vdd 0 cinv m= 32
x24 29 30 vdd 0 cinv m= 10.0793684
x25 30 31 vdd 0 cinv m=101.5936673
x26 31 32 vdd 0 cinv m=322.5397888
x27 32 33 vdd 0 cinv m=1024

vdd VDD 0 1.8
vin 26 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(26) val=0.9 rise=1 targ v(32) val=0.9 rise=1
meas tran tfall trig v(26) val=0.9 fall=1 targ v(32) val=0.9 fall=1
let tp = 0.5*(trise+tfall)

.endc
*--------------------------------------------------------------------------------------------------------------------
N=7

* CMOS Chain Inverter simulation

.include tsmc018.txt

.subckt cinv IN OUT VDD GND
mn1 OUT IN GND GND CMOSN W=0.2u L=0.18u PD=0.7u AD=0.06p PS=0.7u AS=0.06p
mp1 OUT IN VDD VDD CMOSP W=0.6u L=0.18u PD=1.5u AD=0.09p PS=1.5u AS=0.09p
.ends
```

```
*N=7
x28 34 35 vdd 0 cinv  m=1
x29 35 36 vdd 0 cinv m= 2.691800385
x30 36 37 vdd 0 cinv m= 7.245789314
x31 37 38 vdd 0 cinv m= 19.50421847
x32 38 39 vdd 0 cinv m= 52.50146278
x33 39 40 vdd 0 cinv m= 141.3234578
x34 40 41 vdd 0 cinv m= 380.414538
x35 41 42 vdd 0 cinv m=1024

vdd VDD 0 1.8
vin 34 0 pulse(0 1.8 1n 1p 1p 500n 1u)
.control
op
tran 1n 1u

meas tran trise trig v(34) val=0.9 rise=1 targ v(41) val=0.9 fall=1
meas tran tfall trig v(34) val=0.9 fall=1 targ v(41) val=0.9 rise=1
let tp = 0.5*(trise+tfall)

.endc
```