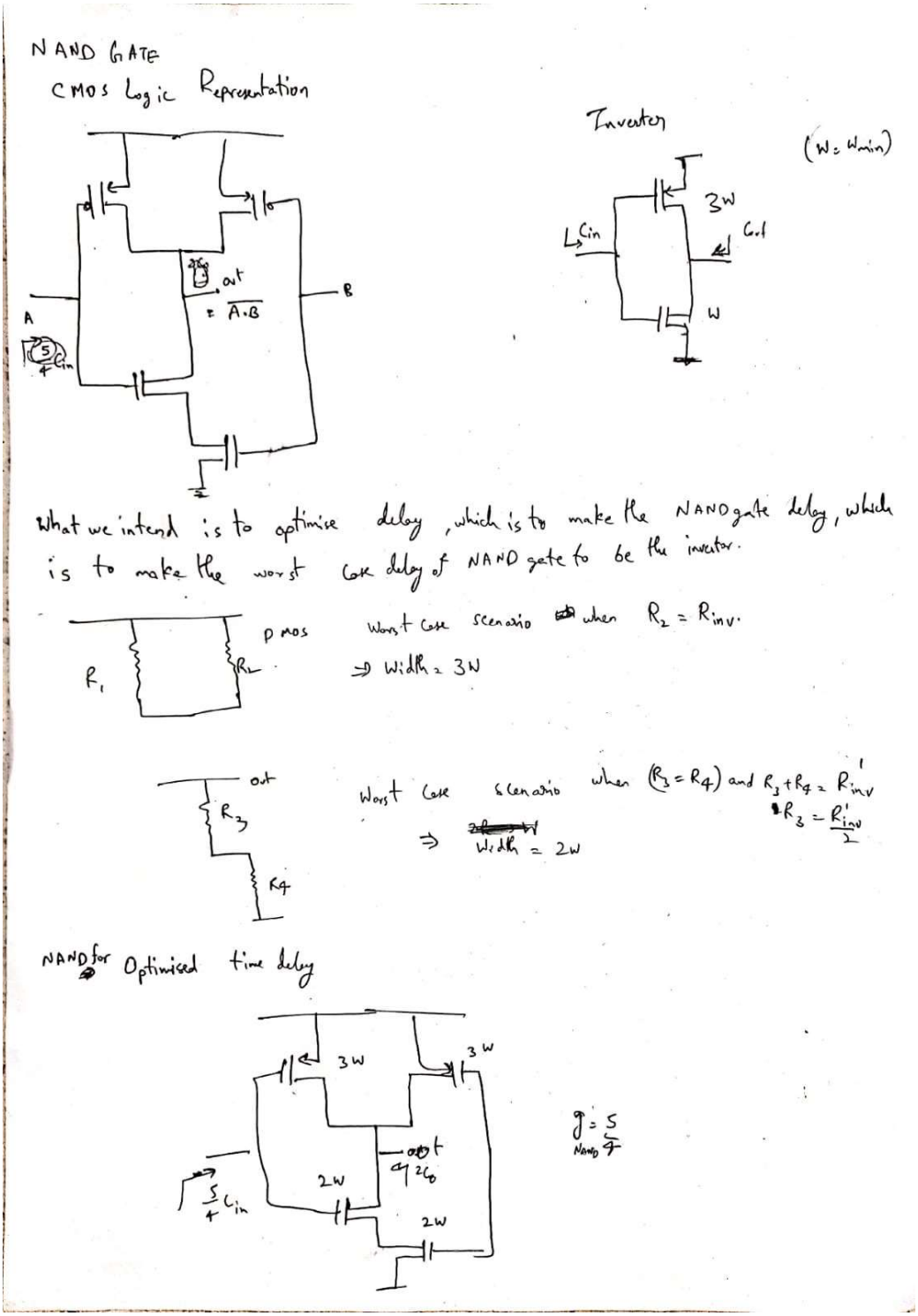
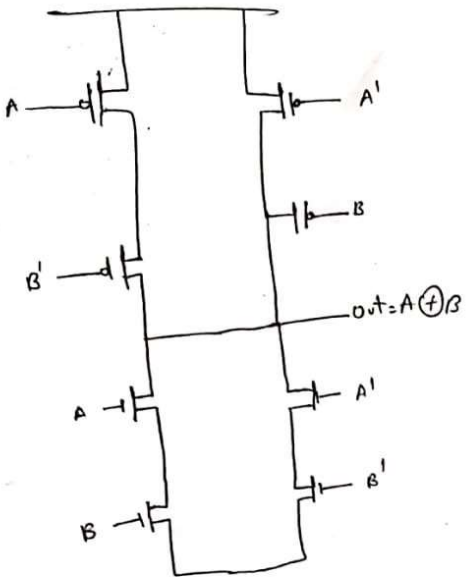
Assignment on logic sizing optimization

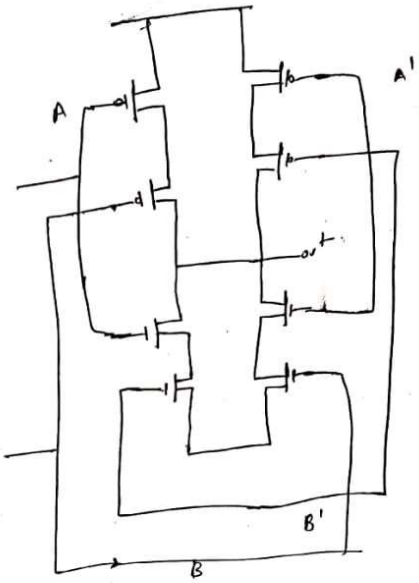
$$\overline{Y} = (\overline{C} + \overline{B})(\overline{A}B + A\overline{B})$$

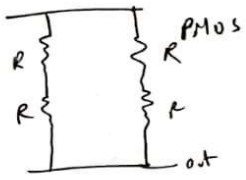
We have to design gates such that delay is minimum. The circuit is used to drive a unit sized inverter.



XOR Gate





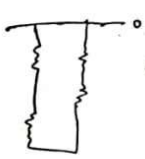


Worst case

$2R_2 R_{inv}$

$R = \frac{R_{inv}}{2}$

$\Rightarrow Width_2 = 3W \cdot 2 = 6W$

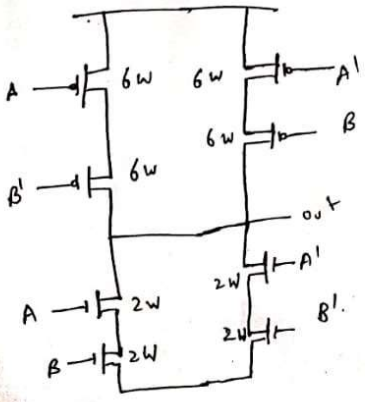


Worst Case

$2R_2 R_{inv}$

$R = \frac{R_{inv}}{1}$

$\Rightarrow Width_2 = 2W$ (B' and A' are generated by inverters).



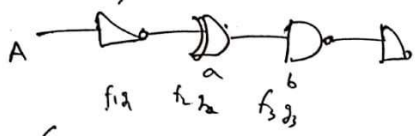
$g_{eff} = \frac{6+6_2}{3+1} = \frac{2}{1}$ (A and A')

$g_{eff} = \frac{6+2}{3+1} = 2$ (B and B')

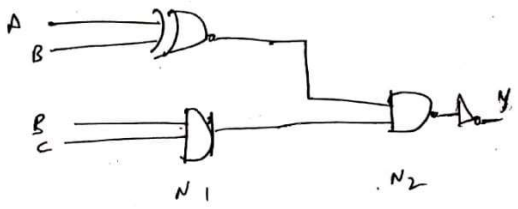
Delay = gf+p

In the above XOR gate to generate A' we also need an inverter

inv, xor, nand, inv path



$F = \frac{C_L}{C_{g_1}} = 1$



$G = g_1 g_2 g_3 = 1 \cdot 2 \cdot \frac{5}{4} \cdot 1 = \frac{5}{2}$ $\quad g_1 = 1,\ g_2 = 2,\ g_3 = \frac{5}{4}$

$H = FG = 1 \cdot \frac{5}{2}$, $h = \sqrt[3]{H} = 1.3572$

$f_1 = \frac{h}{g_1} = 1.3572$, $f_2 = \frac{h}{g_2} = \frac{1.3572}{2} = 0.678$

$f_3 = \frac{h}{g_3} = 1.0857$

$a = f_1/g_2 = 0.678$ $\quad b = \frac{f_1 f_2}{g_3} = 0.736$

As a and b are less than 1 which cannot be generated by foundry.

So, sizing should be $a = 1$, $b = 1$

Similarly if we choose nand nand inv path

Nand ① path should also be sized to 1.

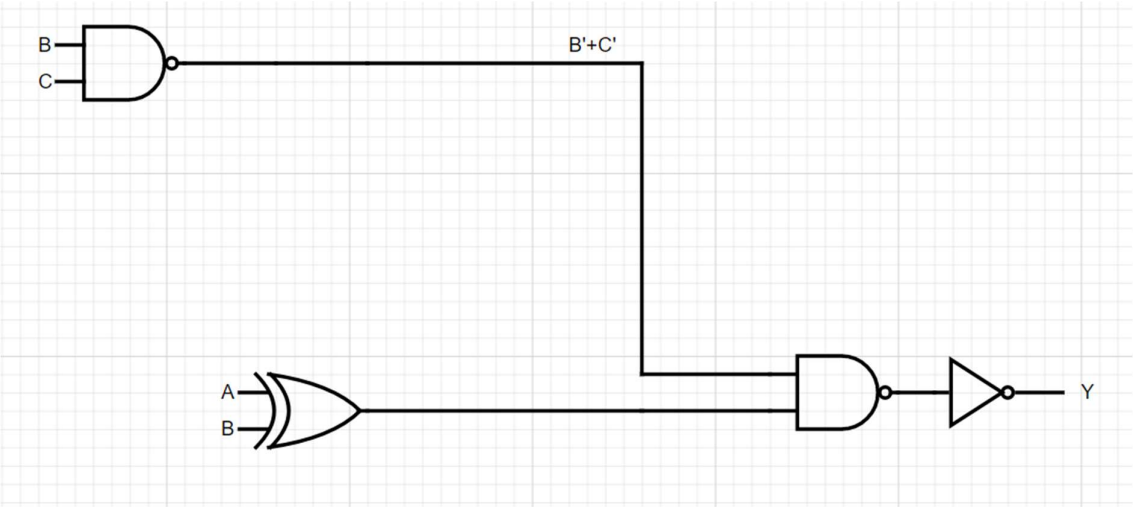
$t_{delay} = \sum t_{p0}\left(p_i + \frac{f_i g_i}{\gamma}\right)$

$= t_{p0}\left(1 + \frac{1.1}{\gamma}\right) + t_{p0}\left(2 + \frac{2.1}{\gamma}\right) + t_{p0}\left(2 + \frac{\frac{5}{4}.1}{\gamma}\right)$ ← (This is higher than below path)

(inv)

$= t_{p0}\left(5 + \frac{17}{4\gamma}\right) = 10\ p\ (9.25) = 9.25 \times 10^{-11}$

Logic Diagram of the circuit



We had written the netlist code and the delay is 7.064078e-11